HEWLETT PACKARD

Technical Information Package

13037 disc controller

Printed: AUG 1980

Copyright © 1980 by HEWLETT-PACKARD COMPANY

NOTICE

The information contained in this document is subject to change without notice.

This document has been prepared for use as a training supplement to facilitate the understanding of theory of operation to the component level. It is not the intent of this document, expressed or implied, to provide information that will enable repair to any level other than that which is specified in the Hewlett-Packard service manual.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

This document contains proprietary information which is protected by copyright. All rights are reserved. No part of this document may be photocopied or reproduced without the prior written consent of Hewlett-Packard Company.

Part No. 13037-90902

HEWLETT-PACKARD COMPANY
P.O. BOX 39, BOISE, IDAHO 83707, U.S.A.

Printed in U.S.A.

CONTENTS

	Page
Introduction	1-1
General Description	2-1
Microprocessor PCA	3-1
Microprocessor Characteristics	3-1
Microprocessor Description	3-1
Functional Description	3-9
ALU	3-14
Instruction Decoding	3-17
Device Controller PCA	4-1
Device Controller Characteristics	4-1
Hardware Description	4-3
Appendix I: Disc Drive Interface	4-23
Appendix II: Computer Interface	4-31
Error Correction PCA	5-1
General Description	5-1
Block Diagram and Functional Description	5-1
Expanded Description	5-11
21XX Interface PCA	6-1
Bus Interface and Decode Logic	6-1
First-In First-Out (FIFO) Buffer	6-3
CPU Flag Logic	6-6
Appendix I: 2100 Interface Logic and Programming	6-9
Power Regulator PCA	7-1
+5 Volt Regulator	7-1
Power Amplifier	7-2
Frequency Response and Loop Stability	7-3
Over Current Protection	7-4
Overvoltage Protection	7-4
Thermal Design Data	7-5
+12 Volt Unregulated Supply	7-5
−20 Volt Unregulated Supply	7-5
+20 Volt Unregulated Supply	7-6
−12 Volt Unregulated Supply	7-6
−5 Volt Regulator	7-6
Power-On Circuit	7-6
Appendix I: Output Specifications	7-7
Appendix II: Troubleshooting Aids at Turn-On	7-6
Firmware	8-1
Appendix I: Microassembler Instruction Description	8-47
Appendix II: Label Call Addresses	8-51

CONTENTS (Continued)

Page

Major 13037 Disc Controller Features 9-1
- Introduction 9-1
- Multiple CPU Disc Drive Operation 9-1
- The File Mask 9-3
- Spare Tracks and the 13037 9-6
- Automatic Head and/or Track Switching 9-12
- Some Routine Overviews 9-14

Programming Information 10-1
- Command Words 10-1
- Control Commands 10-3
- Sense Commands 10-10
- Read Commands 10-20
- Write Commands 10-26

12745 HP-IB Adapter Kit 11-1

INTRODUCTION

Information contained in this engineering supplement is intended to provide the customer with an in-depth knowledge as to the function and operation of the 13037 Disc Controller. All information contained in this document is proprietary and is protected by copyright. No part of this document may be photocopied or reproduced without the prior written consent of the Hewlett-Packard Company.

This document describes the 13037 Disc Controller as it is currently being shipped at the time of this printing. Information contained herein is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

GENERAL DESCRIPTION

The 13037 Disc Controller is comprised of a discrete 16-bit microprocessor with externally addressable hardware functions physically located on the ECC/ROM and device controller boards. Although such functions are under the control of the microprocessor, some of these functions run asynchronously with respect to the microprocessor clock. For such hardware, the microprocessor will monitor various flags describing the condition of the circuitry, and at the appropriate times will update respective control signal latches to govern the desired processes (examples include reading information from the disc or decoding ECC patterns).

The device controller board is responsible for controller communications with the CPU (interface) and the disc drive. Additionally, the device controller hardware contains the circuitry needed to encode and precompensate data prior to its being written onto the disc (via the formatter), as well as to decode the data during subsequent reads.

The ECC/ROM board is comprised of two distinct sections: the ROM hardware (containing the microcoded instructions to be processed by the microprocessor) and the ECC hardware (error correction circuitry enabling the 13037 to correct up to a 32-bit burst of erroneous data read from the disc).

Internal communications of the 13037 microprocessor with the other controller hardware is provided by the microprocessor input/output (MIO) bus. This 16-bit bus is bidirectional, and concurrently connects the microprocessor board with the ECC/ROM and device controller PCA's. When the microprocesor wants to communicate with a particular hardware function of these other boards, the microprocessor sends the representative address over the five-bit external address bus. Function decoders on the ECC/ROM and device controller boards will respond by decoding this address and enabling the appropriate circuitry.

Figure 1 illustrates the relationship of each board to the bus lines previously described.

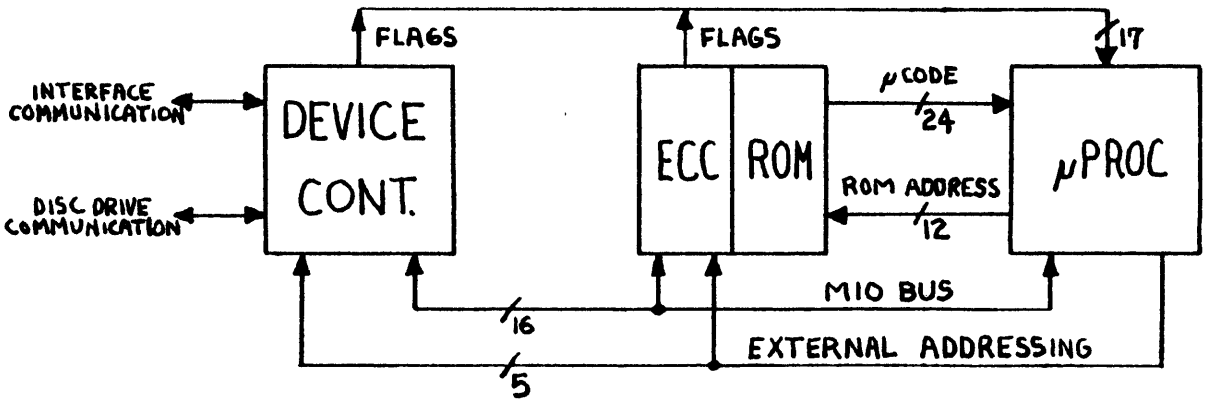


Figure 1

Figure 2 diagramatically relates each of the boards with specific hardware functions internal to these boards. Each of the boards is described below to the level represented by this block diagram. Component level discussions will follow.

The microprocessor board does not physcially contain the ROM hardware, but because it is essential for microprocessor operation, it is included in this section of the block diagram. The addressed microcoded instruction is made available by the ROM to the ROM output register (ROR) for subsequent latching at the beginning of the current instruction. At the same time, the ROM address register (RAR) is incremented to address the next instruction. In this way, the ROM can be setting up for this next instruction while the ROR holds the current instruction for subsequent command decoding.

The command decoding hardware interprets the current instruction as to type, then generates the appropriate control signals for proper execution of that command. One aspect of this decoding includes the determination of any appropriate branching. The branch select logic, in conjunction with the address gating, decides if the intended branch is to take place (by testing the condition code bit), and what address is to be used when branching. This address comes from one of four sources, as selected by the address gating hardware: 1) the three-level subroutine stack (during "return" operations from subroutines); 2) test inputs used in factory testing only; 3) a computed address from the arithmetic portion of the microprocessor (indirect branching; or 4) an immediate address taken directly from the lower twelve bits of the ROR (corresponding to a direct branch). Note that the subroutine stack functions during subroutine calls by buffering the corresponding return address for the "return" operations discussed above.

Other command decoding functions include the selection of a desired condition (either internal to the microprocessor board or one of the external flags previously described) to be latched into the condition code latch during a test instruction. This condition code bit (CCB) is tested by the branch select logic during branch instructions to decide if the intended branch is to be allowed (including subroutine calls and returns).

The arithmetic portion of the microprocessor board can process data from two sources: an eight-bit immediate operand (provided by the lower eight bits of the ROR), or register data (stored in the internal A and B registers). The arithmetic logic can function in byte (upper or lower) or full word modes. Byte modes must by used during immediate operand instructions, and though the immediate operand replaces any A register (A REG) source, a B register (B REG) must be used concurrently for any operation other than PASS or COMPLEMENT. For normal operations, A and/or B register sources are used and either byte or full word modes can be specified.

The registers are organized as two sets of four 16-bit registers (i.e., four A registers and four B registers). They receive data from the MIO bus for storage and source data to the arithmetic logic unit (ALU) for processing. The ALU will accept data as previously described and operate on these data as prescribed by the current instruction. The resulting computation is stored in a temporary register (T register) for later use, and subsequently passed to the shifter for any swap, shift, or rotate operation prior to its driving the MIO bus. If the resulting data is to be stored in one of the internal registers, it is now available on the MIO bus for writing into that register.

The process status register (PSR) monitors salient characteristics of the current arithmetic operation and latches that information for later review. This data can be individually sampled by the condition select logic in setting the condition code latch. In this way, branching can occur based on a former arithmetic result.

The external address bus is driven from the appropriate bits of the ROR. This data is used as previously described to allow the microprocessor to enable external communication paths over the MIO bus.

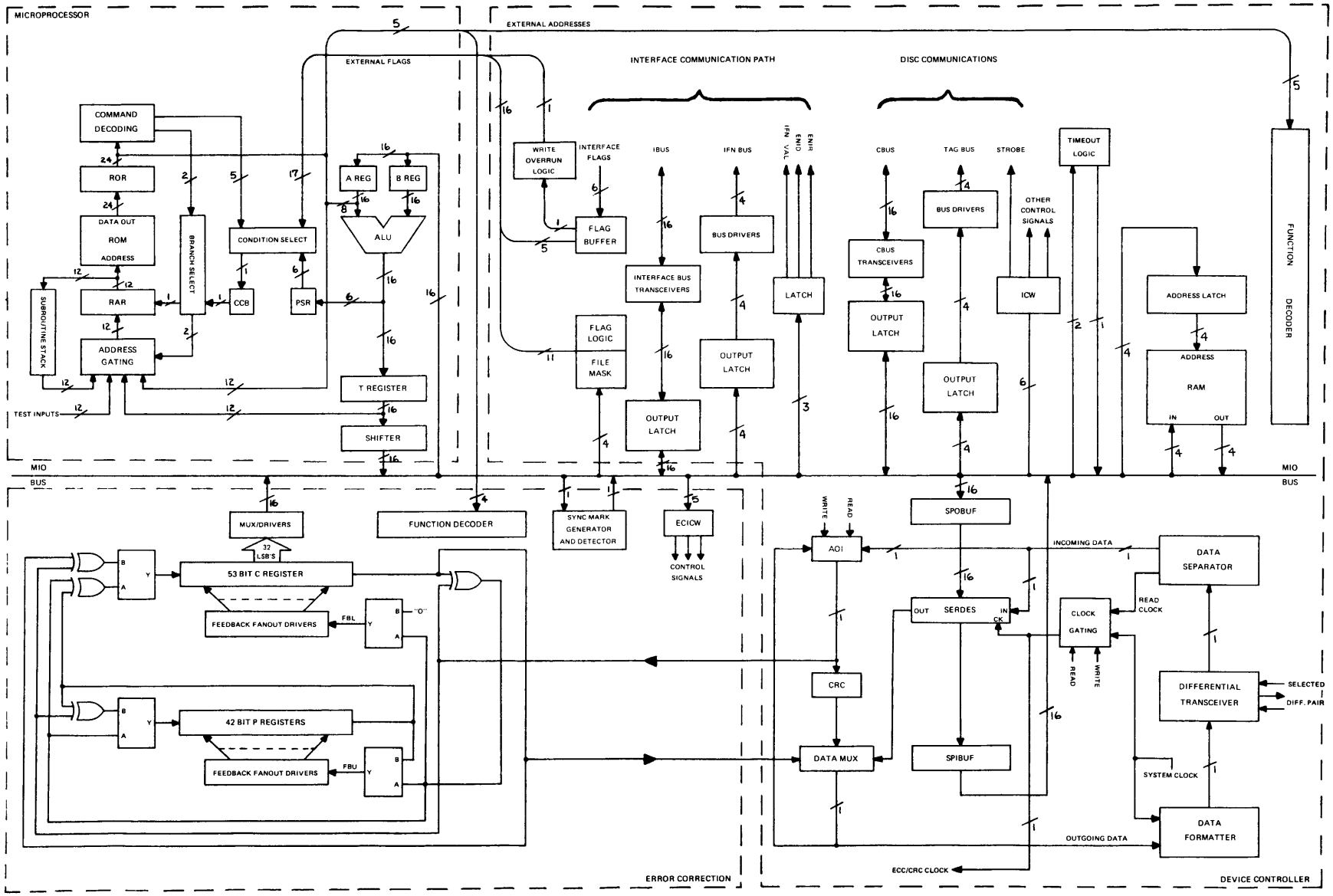

MICROPROCESSOR
EXTERNAL ADDRESSES
EXTERNAL FLAGS
INTERFACE COMMUNICATION PATH
DISC COMMUNICATIONS
COMMAND DECODING
ROR
DATA OUT ROM ADDRESS
RAR
ADDRESS GATING
SUBROUTINE STACK
BRANCH SELECT
CONDITION SELECT
CCB
PSR
A REG
B REG
ALU
T REGISTER
SHIFTER
TEST INPUTS
WRITE OVERRUN LOGIC
INTERFACE FLAGS
FLAG BUFFER
FLAG LOGIC
FILE MASK
IBUS
IFN BUS
IFN VAL
END
ENIR
INTERFACE BUS TRANSCEIVERS
BUS DRIVERS
OUTPUT LATCH
LATCH
CBUS
TAG BUS
STROBE
CBUS TRANSCEIVERS
OUTPUT LATCH
BUS DRIVERS
OUTPUT LATCH
OTHER CONTROL SIGNALS
ICW
TIMEOUT LOGIC
ADDRESS LATCH
ADDRESS
RAM
IN
OUT
FUNCTION DECODER
MIO BUS
MUX/DRIVERS
32 LSB'S
53 BIT C REGISTER
FEEDBACK FANOUT DRIVERS
FBL
42 BIT P REGISTERS
FEEDBACK FANOUT DRIVERS
FBU
FUNCTION DECODER
SYNC MARK GENERATOR AND DETECTOR
ECIOW
CONTROL SIGNALS
ERROR CORRECTION
WRITE
READ
AOI
CRC
DATA MUX
SPOBUF
SERDES
SPIBUF
INCOMING DATA
DATA SEPARATOR
READ CLOCK
CLOCK GATING
DIFFERENTIAL TRANSCEIVER
SELECTED
DIFF. PAIR
SYSTEM CLOCK
DATA FORMATTER
OUTGOING DATA
ECC/CRC CLOCK
DEVICE CONTROLLER

Figure 2

The device controller board performs two major functions: communications with the CPU interface and disc drive, and the conditioning of data during disc reading and writing. These major functions are illustrated in the upper and lower portions of figure 2, respectively.

The function decoder monitors the external address bus to decide which function is being enabled by the microprocessor; in this way conflicts over use of the MIO bus are eliminated. Additionally, the internal control word (ICW) latch is updated by the microprocessor board to contain control signals relating to the particular function being performed (i.e., read, write, disc drive function bus validation, etc.). These control signals are used primarily by the data encoding and decoding hardware to establish the current modes of operation.

The RAM and its address latch are used to store 16 four-bit words of data for later use by the controller. This information includes disc drive to CPU mapping, a retry counter (used in recovering valid address information from a defective track), polling information, and other such quantities.

The timeout logic is a 1.8-second hardware timer used whenever the device controller has to wait for the CPU or disc drive to complete an intended function. Examples of such functions include waiting for the CPU interface to send or receive data, or waiting for the disc drive to complete an incremental (or decremental) seek during multiple track transfers. If the intended function does not complete within the 1.8-second period, the controller will enter a power on/timeout processor routine to disconnect from the malfunctioning device.

The file mask logic of the device controller is a series of one bit latches that retain information concerning sparing operations (sparing enabled) and multiple track transfers (direction of seek, cylinder or surface mode, etc.). This information is updated only by a power-on (or timeout) or by a CPU "Set File Mask" command to the controller. These one-bit data can be individually sampled as external flags by the microprocessor.

Additional external flags from the CPU interface are buffered by the flag buffer hardware. One flag, the overrun signal, is further qualified by the write overrun logic to detect any overruns internal to the device controller board during write operations.

The communications paths between the controller and the disc drive and CPU interface are organized in a basically identical manner. Each communication path has a four-bit function bus to describe the operation expected of the CPU interface or disc drive. These commands are transmitted over the interface function bus (IFN BUS) or the disc drive TAG BUS. These busses are unidirectional and are driven by the device controller board. Each bus has an output latch that (when enabled by the function decoder) stores the current MIO bus contents for subsequent transmission through the bus drivers. In this way the latched function remains constant independent of any changes on the MIO bus (until, of course, being updated as selected by the function decoder).

These functions must be validated by a control signal before the interface or disc drive will respond to them (in this way spurious noise will fail to initiate false operations). The interface function valid (IFN VAL) signal, one of three latched values, enables the interface to respond to the associated IFN BUS command. Additionally, the two other latched values are sent to the interface: the ENIR (enable interface receiver) signal enables the interface to accept information over the 16-bit interface bus (IBUS), a bidirectional data bus used to transfer additional data pertinent to the particular interface function being executed (i.e., a READ function would send read data to the CPU over the IBUS); the ENID (enable interface driver) signal allows the interface to send information over the IBUS (i.e., data words to be written onto the disc).

Validation of disc drive TAG BUS functions occurs with a true STROBE signal. This signal is updated with the ICW previously discussed. The disc drive control bus (CBUS), a 16-bit, bidirectional counterpart to the interface IBUS, has no equivalent ENIR or ENID signals. Instead, the most significant bit of the TAG BUS is used to establish direction of data transfer over the CBUS.

As with the function busses, the IBUS and CBUS require output latches to retain MIO bus information being outputted by the controller. When inputting information from these busses, the output latches are bypassed (information is passed directly over the IBUS and written into a microprocessor register).

Actual serial data transfer to or from the disc drive is handled asynchronously to the microprocessor by the lower half of the figure 2. At the heart of the transfer operation is the serializer-deserializer (SERDES), a 16-bit shift register with parallel loading capabilities.

In the write mode, the SERDES parallel output buffer (SPOBUF) gets updated with MIO bus data to be written as the next word onto the disc. Every sixteenth clock pulse, SERDES parallel loads the latched SPOBUF quantity and subsequently serially shifts it to the drive. The microprocessor then updates SPOBUF (via the function decoder) with the next word to be written.

In the read mode, SERDES serially inputs data as it is read from the disc. With every sixteenth bit the SERDES parallel input buffer (SPIBUF) latches the current word read from the disc. Before the next sixteenth bit, the function decoder will enable SPIBUF to put that word on the MIO bus for subsequent transmission to the interface.

It should be noted that in both the read and write modes previously described, a bit counter increments with every clock of SERDES. At every word boundary (every sixteenth bit) an EOW flag is set telling the microprocessor that a word has been read (SPIBUF has been updated), or a word is being written (SERDES has parallel loaded the SPOBUF quantity). In this way the microprocessor can synchronize itself with the somewhat asynchronous read/ write logic.

(The fact that microprocessor instructions are executed at a 5 MHz rate while data is transferred to/from the disc at a nominal 468.75k word/second rate reflects the asynchronous nature of the two operations.)

Prior to being written onto the disc, the serial data from SERDES is encoded to allow denser information packing onto the media. Additionally, a separate clock from the disc is not required as the MFM encoding technique is used (MFM combines the clock and data into one waveform and can be subsequently decoded into the original clock and data streams). The data formatter hardware takes SERDES serial data, encodes it, and precompensates it (to prevent disc media pulse crowding effects) before sending it to the differential transceiver. It should be noted that encoding of data is done with the system clock (divided down to the desired bit transfer rate).

Each of the eight data ports of the device controller is driven by a differential transceiver. These transceivers are connected in parallel, with possible conflicts eliminated by the fact that only the selected drive will enable its respective differential transceiver (only one drive is ever selected at any given time).

Besides sourcing formatted data to the drive during write operations, the differential transceiver receives read data from the drive and channels it to the data separator hardware. This hardware phase locks to the incoming waveform and derives from it the decoded data. Additionally, a clock is generated coincident with this decoded data that will track with any fluctuation in the return rate of that data. This read clock is gated through the clock gating hardware to clock SERDES in time with the incoming read data (during the write mode, formatted data is generated synchronous to the system clock, and thus the gating logic passes the system clock to SERDES).

As a supplemental means of determining the integrity of a read transfer, cyclic redundancy circuitry (CRC) is incorporated. This hardware uses data being written onto the disc (prior to its being formatted) to generate a characteristic CRC word. This word is subsequently ap-

pended to the written data field. During read operations, separated data is concurrently fed to SERDES and the CRC logic. A new CRC word is subsequently generated that will, if no errors were enountered, match the previously written CRC field. Absence of this match will cause a data error signal generation.

Because of the two possible sources of CRC input (separated data during read operations and outgoing data during write operations), and-or-invert (AOI) hardware is provided to establish the proper data path to the CRC.

In addition to CRC error detection, an error detection and correction technique is additionally provided to help correct misread or miswritten data. This error correction circuitry (ECC) monitors the same data as the CRC and hence is fed from the output of the AOI logic. As with CRC, during write operations a characteristic ECC pattern is generated and appended to the CRC field of the sector. This outgoing data requires a third write data path to the disc (i.e., data field path from the interface, CRC field path from the CRC hardware, and ECC field path from the ECC/ROM board); the DATA MUX must be included to appropriately select these data paths at the respective time that the corresponding fields are to be written onto the disc. It is the data mux output that is then sent to the data formatter for appropriate encoding.

The error correction circuitry (ECC) is comprised of one 53-bit shift register and one 42-bit shift register. In the encoding mode (i.e., during write operations when data sent to the disc is used to generate the characteristic ECC pattern), these two registers are joined in series and given appropriate feedback to create a 95-bit encoding register. In the decoding mode (i.e., during read operations when separated data is monitored in an attempt to detect errors), each register is simultaneously fed the separated read data. After the sector is clocked through, both registers will be identically zero if no error occurs. If any are non-zero, an error was detected by the respective non-zero register. Only when both registers are non-zero (i.e., both have detected an error) can error correction be attempted (both registers will be compared to see if they agree on the detected error).

Because of the varying configuration of the ECC hardware in the decoding and encoding mode, mux'es are included to attain the proper configuration for the respective operation. These mux'es affect not only the relationship of the registers, but the type of feedback as well. The control signals necessary to esablish these conditions are generated by the error correction internal control word (ECICW). This latch is updated by the MIO bus when enabled by the function decoder hardware (this hardware monitors the microprocessor generated external address lines, and performs the same type of function as the function decoder on the device controller board).

Once an error has been detected and the correction pattern generated, the correction data must be sent to the CPU. At this time the function decoder will enable the mux/drivers to select the appropriate word and send it across the MIO bus for subsequent transmission to the interface.

The sync mark generator and detector hardware is included to establish during write operations that a valid ECC field is being written (i.e., a 100376 sync word will be written as opposed to a 100377 sync word), and determine during read operations that a valid ECC field is present (found by monitoring the least significant bit of the sync word). This hardware was included because the initial controllers were to have error correction as an option, but it was later decided to be included as standard equipment.

This concludes the general description of the 13037 Disc Controller. Detailed circuit theory is found elsewhere in this document.

CONTENTS

		Page
1.0	MICROPROCESSOR CHARACTERISTICS	3-1
2.0	MICROPROCESSOR DESCRIPTION	3-1
2.1	Block Diagram	3-1
2.2	Module Descriptions	3-3
2.2.1	Processor Hardware Description	3-3
2.2.2	Instruction Description	3-4
3.0	FUNCTIONAL DESCRIPTION	3-9
3.1	Clock	3-9
3.2	ROM	3-9
3.3	Instruction Flow	3-9
3.3.1	Timing	3-9
3.3.2	RAR Addess Gating	3-13
3.3.3	Condition Code	3-13
3.3.4	Subroutine Stack	3-14
4.0	ALU	3-14
4.1	Immediate Operands	3-15
4.2	Registers	3-15
4.2.1	Write	3-15
4.2.2	Read	3-15
4.3	T-Register	3-15
4.4	Processor Status Register	3-16
4.5	Shifter	3-16
4.6	Signal Polarity	3-17
5.0	INSTRUCTION DECODING	3-17
5.1	U101	3-17
5.2	I/O Decoding	3-17
5.3	Byte Selection	3-18

MICROPROCESSOR PCA

1.0 MICROPROCESSOR CHARACTERISTICS

This document describes the microprocessor PCA of the 13037 Disc Controller. The function of the disc controller is to translate high-level commands from a 21XX or 3000 series computer into commands recognized by controller-compatible disc drives. Examples of such high-level commands are READ, WRITE, SEEK, and REQUEST STATUS.

The disc controller is a microprogrammed processing unit. The microprogram, or firmware, is stored in a read only memory. The microprocessor fetches instructions from the ROM, decodes them, manipulates and stores data, and creates the control signals which sequence the disc controller hardware.

Microprogramming has several advantages over the alternative method of implementing a disc controller by using a hardware sequenced state machine. Microprogramming allows a straightforward, orderly hardware design which is largely independent of specific controller characteristics. Complex algorithms in a microprogrammed machine do not require complex hardware, only appropriate firmware. Controller modification becomes a matter of changing firmware, which is much easier than modifying hardware.

The disc controller microprocessor resides on a single 3000-size printed circuit board. It communicates with the other disc controller modules via a central data (MIO) bus and clock, strobe, and addressing lines. Its current load is 5 amps.

2.0 MICROPROCESSOR DESCRIPTION

2.1 BLOCK DIAGRAM

Figure 1 is a block diagram of the microprocessor. The left half of figure 1 is instruction sequencing logic; the right half shows the registers, and arithmetic and logic modules.

Instructions are contained in the ROM. The command decoding block uses the current instruction to create control signals which operate the arithmetic/logic section. The ROM address register contains the address in ROM of the next instruction. This address is one greater than the previous address if a branch is not being executed. If a branch is being executed, the address gating network selects the proper branch address from one of four possible sources: the subroutine stack, an external address, the T register, or the immediate field of a branch instruction.

The condition select block tests a flag and sets the condition control bit (CCB). The branch select logic looks at the CCB to decide if the branch is to succeed or fail. It also determines what type of branch is to occur.

The right part of figure 1 shows the four A and four B registers which may act as inputs for the ALU. Note that an immediate operand may replace an A register in some instructions. The ALU output is temporarily held in the T register. Following this, the shifter rotates, shifts, or swaps bytes, putting the result on the MIO bus. This result is then directed either to an A or B register, or to an external destination.

The PSR block represents the processor status register, which latches six ALU conditions and makes them available to the conditional branch test circuitry.

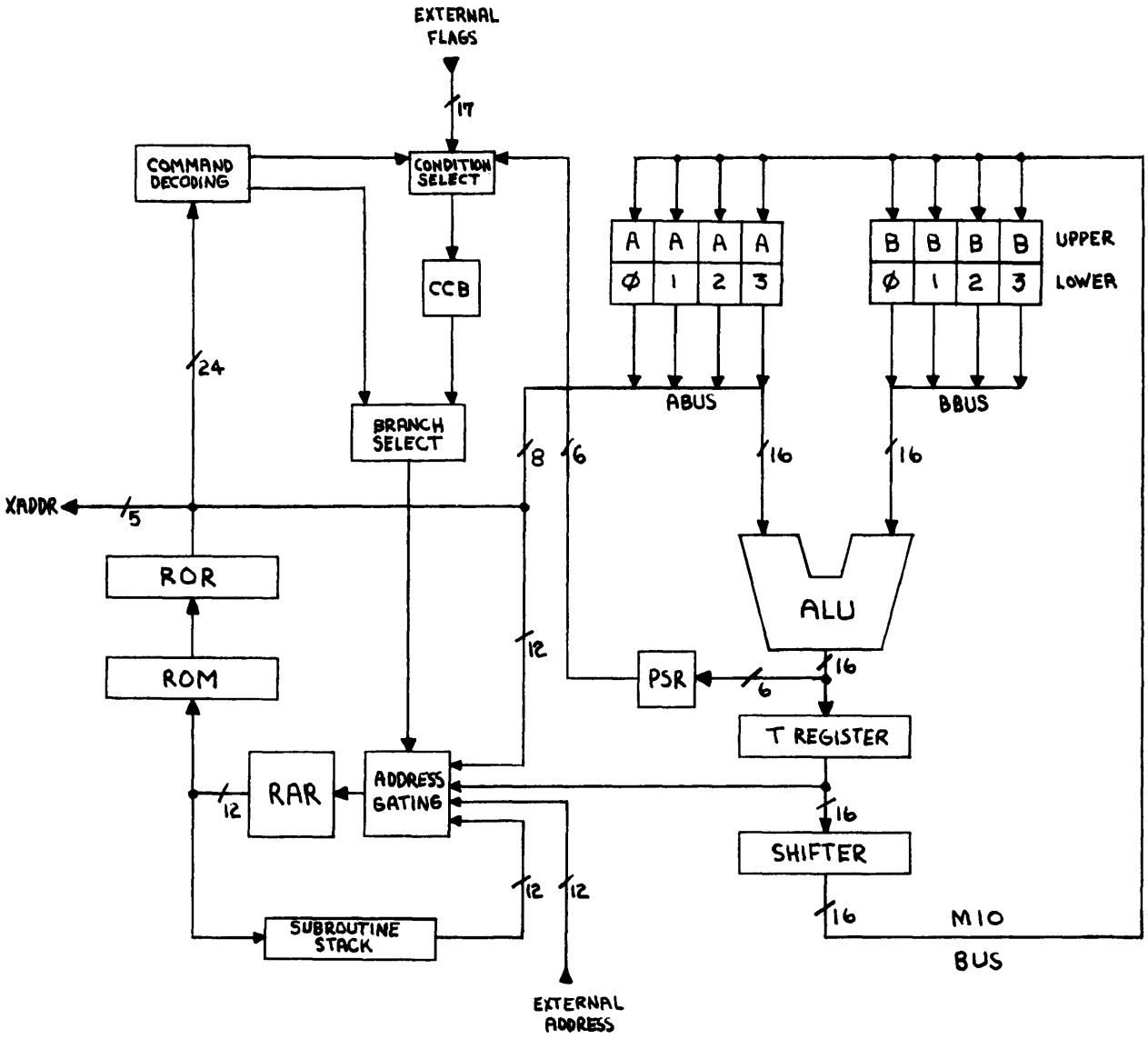


Figure 1. Microprocessor Block Diagram

2.2 MODULE DESCRIPTIONS

Microprocessor Module

This module contains all of the major decision-making logic contained in the controller. It can execute arithmetic/logical, input/output, and branch instructions. Each instruction will be executed in 200 ns. It controls and communicates with all other controller modules on the central MIO bus.

2.2.1. Processor Hardware Description

ALU

The ALU performs all of the functions listed below. ROM bits 16 - 20 and 14 in arithmetic and I/O instructions specify which operation is to be performed. All operations may be performed on a 16-bit (full word) or 8-bit (byte) basis. ALU status is available after each arithmetic instruction and is held in the Processor Status Register (PSR). Listed below are the operations incorporated by the 13037B firmware.

PLUS	INCREMENT	COMPLEMENT
MINUS	EXCLUSIVE OR	LOGICAL AND
PASS	INCLUSIVE OR	DECREMENT

BUSES

The ALU is driven by the "A" and "B" buses, each of which connects to four 16-bit registers, to be described later. The "A" bus also connects to the Immediate Operand field of the ROM instruction. (Note, therefore, that all two parameter immediate operations are with B registers.) All information on these buses is ground true.

The MIO bus is a 3-state bus which connects the output of the ALU-shift unit to the registers, as well as other modules. Information may be strobed out on this bus from a register or Immediate Operand, or it may be strobed into a register from the outside world or from the shift unit. Information on this bus is ground true.

REGISTERS

Eight 16-bit registers are implemented. Four of them drive the "A" bus (A0 – A3) and the other four (B0 – B3) drive the "B" bus. All are fed from the MIO bus.

Instructions may affect only the upper or the lower byte of these registers, or, in some cases, the entire 16 bits.

CONDITIONS

Seventeen external flags and six processor status indicators are available for use in conditional branches. They are all positive true. The external flags connect to the outside world via the MIO connector. Processor status is recorded during each arithmetic instruction in the Processor Status Register (PSR) and is available until the next arithmetic instruction. These conditions are: EQUAL, signifying that the contents of the A and B registers selected are equal; UOVER, signifying overflow (carry) out of the ALU upper byte; LOVER, indicating carry out of the lower byte of the ALU; TNZRO, meaning that the contents of the T-register are not zero; TMSB, the sign bit of the T-register; and TLSB, the LSB of the T-register. In addition, a condition which is always FALSE is provided for unconditional branches.

An SCC (set condition code) instruction should be executed before a branch to clock the selected condition into the condition code bit (CCB). A following branch will depend on the value set in the CCB by the last SCC instruction.

S-REGISTER

The S-register is a three-level LIFO (last-in-first-out), or push-down, stack. This allows for three-level subroutine jumps. When a CALL is executed, the current address plus 1 is pushed onto the stack; when a RTN is executed, the value on the top of the stack is put into the P-register and the stack is popped.

Care should be taken in programming not to exceed three levels of subroutine nesting, as only the last three return addresses are remembered; previous information is lost. Also, if more than three returns are made in succession, then the address which was at the bottom of the stack will be repeatedly jumped to.

T-REGISTER

The T-register holds the result from the ALU, again in ground true form. An indirect branch will load the contents of the T-register into the P-register, so care must be taken that the data in the T-register at that point has been complemented and is the correct sense.

SHIFTER

The shifter can: swap bytes; pass; and rotate, shift left, or shift right by one bit. Rotates and swaps are meaningless for byte instructions.

CLOCKS

The microprocessor runs on a 30 MHz clock in six phases, labeled T0 through T5. Timing is shown in figure 3 (next section). Each instruction is executed in 200 ns.

P-REGISTER AND ADDRESS GATING

The P-register is a 12-bit counter register which addresses the ROM. Normally the next instruction is in the current address plus one, so P is incremented during each instruction. In a branch, however, one of four different address sources (depending on the ROM instruction and the CCB) is loaded into the P-register.

This address may come from the BRANCH ADDRESS field of the ROM, the S-register, the T-register, or an external source. Which branch is taken is discussed in the description of the instructions.

ROM

A bipolar ROM with maximum access time of 130 ns is used to store the control program. The instruction word width is 24 bits. Up to 4K of control storage is addressable.

2.2.2 INSTRUCTION DESCRIPTION (Refer to figure 2)

OTI — Output Immediate Operand

The immediate operand contained in ROM bits 0 – 7 is passed through the ALU and shifter to the MIO bus. Information on the MIO bus is ground true. The external destination contained in ROM bits 8 – 12 is put on the external address bus and is positive true. External select is true for the entire instruction time. At T4 the UB or LB strobe (depending on ROM bit 13) is transmitted. The strobe occurs for 1.5 CPU clock periods (allowing for attenuation prior to reaching the device controller board) and is positive true. No shift is performed.

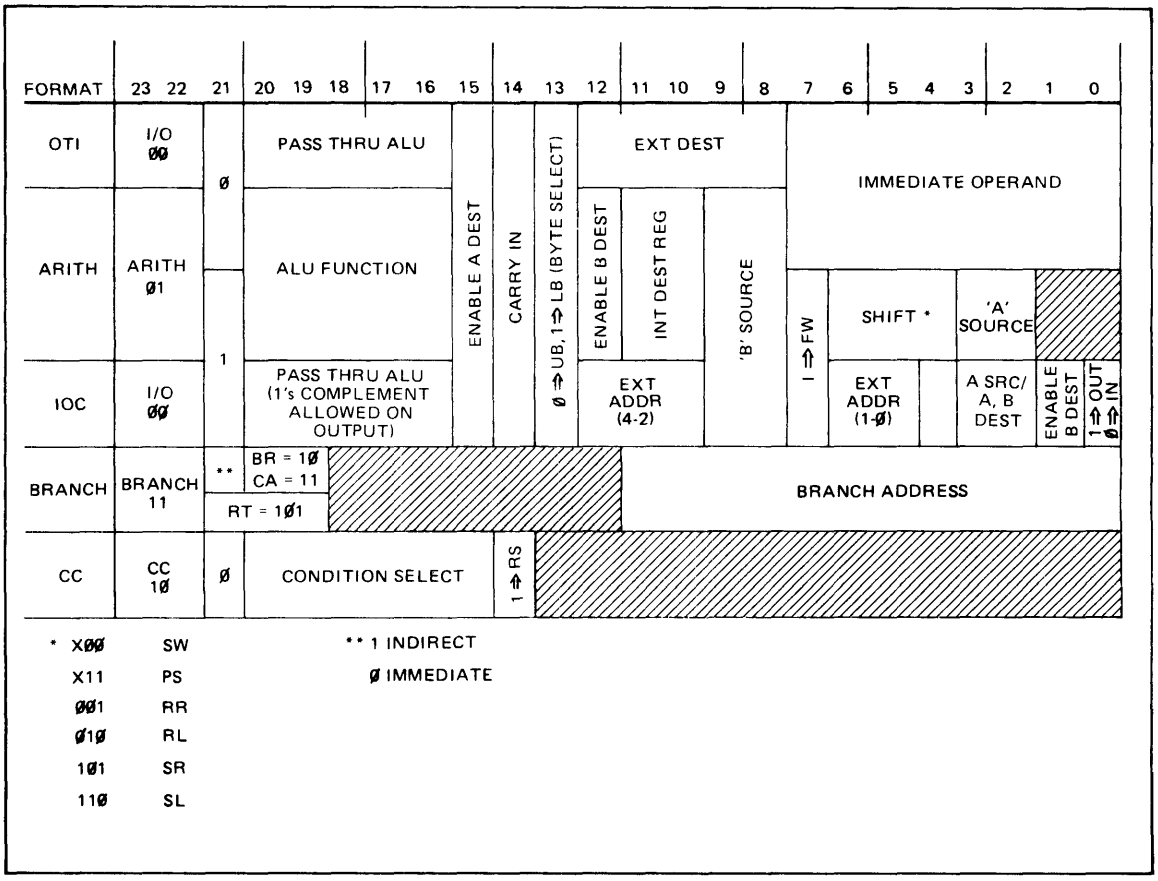


Figure 2. Instruction Format

U/L Field (ROM Bit 13)	If 0, immediate operand is put on the upper byte of the MIO bus; if 1, it is put on the lower byte.
EXT DEST Field (ROM Bits 8 – 12)	A five-bit field containing the address of the external destination of the immediate operand.
IMMEDIATE OPERAND Field (ROM Bits 0 – 7)	An eight-bit field containing binary information to be output to the address contained in the EXT DEST field.

ARITH — Arithmetic

A. With Immediate Operand (ROM Bit 21 = 0)

The ALU performs the operation specified by ROM bit 14 and ROM bits 16 – 20. It takes as inputs the immediate operand (ROM bits 0 – 7) from the A bus, and a B register specified by ROM bits 8 – 9. ROM bits 10 – 11 specify the number of the register into which the result is written, and ROM bits 15 and 12 specify whether an A register, a B register, both, or neither are written into. U/L (ROM bit 13) specifies which byte is affected. No shift is performed.

B. Without Immediate Operand (ROM Bit 21 = 1)

The ALU performs the operation specified by ROM bit 14 and ROM bits 16 – 20. It takes as inputs an A register specified by ROM bits 2 – 3 and a B register specified by ROM bits 8 – 9. A shift specified by ROM bits 4 – 6 is performed on the result. ROM bits 10 – 11 specify the number of the register into which the result is written, and ROM bits 15 and 12 specify whether an A register, a B register, both, or neither are written into. U/L (ROM bit 13) and FW (ROM bit 7) specify whether the upper byte, the lower byte, or both are affected.

ENABLE A DEST (ROM BIT 15) and
ENABLE B DEST (ROM BIT 12) FIELDS

Each bit, if set to 1, causes the result of the operation to be written into a register on the A or B bus, respectively. If both are set, an A and B register are paired and the effect is that of a single register available to both buses. If neither is set, the result is left in the T register until T3 of the next instruction. This allows computation of a final branch address without the need to write the information back into a register.

INT DEST REG FIELD (ROM BITS 10 – 11)

These bits contain the number of a register into which the result will be written. (ENABLE A DEST and ENABLE B DEST determine which group — A or B — that will be written into.)

A SOURCE (ROM BITS 2 – 3) and
B SOURCE (ROM BITS 8 – 9) FIELDS

Specify which register is put on each bus for an ALU operation.

IMMEDIATE OPERAND FIELD (ROM BITS 0 – 7)

This field represents an eight-bit number used in an ALU operation with a B register. Only one byte is affected (replaces A register).

U/L (ROM BIT 13) and
F/W (ROM BIT 7) FIELDS

These bits determine which byte(s) is (are) affected during an operation. If FW = 1, both bytes of the sources are used, and both bytes of the result are written in the destination. If only U or L is specified, only that byte of the operand and destination are affected. The other byte in both source and destination is left unaffected. (U/L = 0 specifies an upper byte; U/L = 1 specifies a lower byte.)

SHIFT FIELD (ROM BITS 4 – 6)

This three-bit field specifies what shift operation is to be done on the result from the ALU before the result is written into its destination:

ROM BIT			MNEMONIC	ACTION
6	**5**	**4**		
X	0	0	SW	Swap bytes (full word only)
X	1	1	PS	Pass no shift
0	0	1	RR	Rotate 1 bit right (full word only)
0	1	0	RL	Rotate 1 bit left (full word only)
1	0	1	SR	Shift 1 bit right
1	1	0	SL	Shift 1 bit left

IOC — Register I/O

A. Input to Register (ROM Bit 0 = 0)

Selects an external source and loads a selected register with the contents of that source. The external source address (ROM bits 5 – 6 and ROM bits 10 – 12) is put on the external address bus; external select (EX SEL) is true (high). An input strobe (INPUT) is sent out positive true. During T4, the data on the MIO bus (ground true) is written into the register(s) whose number is specified by ROM bits 2 – 3, and whose group is selected by ROM bits 15 and 1 (an A register, B register, both, or neither). If FW = 1 (ROM bit 7), the entire 16 bits of the MIO bus is recorded; if only U or L is true, then only the appropriate byte is recorded.

B. Output from Register (ROM Bit 0 = 1)

A selected register is output to a selected external destination. The source register is selected by ROM bits 2 – 3. Note that ROM bits 15 and 1 (enable A dest and enable B dest) are meaningless in this case. The assembler must know whether an A or B register is required, and insert PSA or PSB (Pass A or Pass B), or CMA or CMB (Complement A or Complement B) into the opcode field (ROM bit 14 and ROM bits 16 – 20). External select (EX SEL) is true during the entire instruction time (ground true). A shift specified by ROM bits 4 – 6 is performed on the output of the ALU. At time T4 UB OUT, LB OUT, or both (depending on U, L, and FW) is put out positive true.

ALU FUNCTION FIELD (ROM BIT 14 and ROM BITS 16 – 20)

The assembler must decide whether an A or B register is to be output, and insert PSA or PSB (or CMA or CMB) into this field; on input operations, this field is meaningless. For OTI, only Pass A may be used.

ENABLE A DEST (ROM BIT 15) and
ENABLE B DEST (ROM BIT 1) FIELDS

On input (ROM bit 0 = 0) conditions, the mode of operation is as described for the ARITH instruction; the fields are meaningless for output conditions (ROM bit 0 = 1).

U/L (ROM BIT 13) and
FW (ROM BIT 7) FIELDS

These are the same as described for ARITH instructions.

EXT ADDR FIELD (ROM BITS 0 – 4)

For output conditions (ROM bit 0 = 1), the field is as described for OTI. On input conditions (ROM bit 0 = 0), this field represents a five-bit address of an external source whose contents are to be stored in a processor register.

A/B SRC/DEST REG FIELD (ROM BITS 2 – 3)

On output conditions (ROM bit 0 = 1), this field contains the number address of the register to be output; it is used in conjunction with the ALU FUNCTION field in determining the specific register to be accessed. On input conditions (ROM bit 0 = 0), this field is used in conjunction with the ENABLE A DEST and ENABLE B DEST fields to specify the register(s) into which information is to be written.

I/O FIELD (ROM BIT 0)

A one-bit field specifying whether a register is to be input to or output from (0 = input, 1 = output).

BRANCH

A. JUMP (ROM BIT 20 = 1, ROM BIT 19 = 0)

If the CCB is false, the branch is not taken and the next instruction is executed. If the CCB is true, and if the branch is specified by bit 21 to be indirect, the contents of the T-register (temporary ALU result register) replace the contents of the ROM address register (i.e., the T-register contains the address of the next instruction). If bit 21 specifies a direct branch, then the address contained in ROM bits 0 – 11 is used as the address of the next instruction. The CCB is set true at the end of the instruction.

B. CALL (ROM BIT 20 = ROM BIT 19 = 1)

Operates just like a branch except that before the branch is taken (if and only if the CCB is true) the contents of the ROM address register are pushed onto the subroutine stack. The CCB is set true at the end of the instruction.

C. RTN (ROM BIT 21 = ROM BIT 19 = 1, ROM BIT 20 = 0)

If the CCB is true, the address in the top of the subroutine's stack replaces the address in the ROM address register, and the subroutine stack is popped. If more than three pops are made, the first-in address will always be used. If the CCB is false, the ROM address register is incremented. The CCB is set true at the end of the instruction.

SCC — Set Condition Code

Samples the condition specified (see below) and sets its value into the condition code bit (CCB). RS (reverse sense) may be used to negate the condition. Subsequent branches will be affected by the condition of this bit.

CONDITION SELECT	
01 0000 thru 01 1111	External Flags 00B – 17B
10 0000	External Flag 20B
10 0001	LOVER — Lower byte ALU carry
10 0010	EQUAL (A = B)
10 0011	UOVER (ALU overflow)
10 0100	TNZRO (T register ≠ 0)
10 0101	TMSB (Sign of T register results)
10 0110	TLSB (LSB of T register)
10 0111	FALSE (Unconditional False)

3.0 FUNCTIONAL DESCRIPTION

3.1 CLOCK (Refer to Sheet 3 of the microprocessor schematics)

U37 and its associated circuitry form an ECL oscillator. A 10 MHz crystal and a third harmonic tank circuit provides the 30 MHz master clock frequency. C7 is adjustable for a 30 MHz waveform at test point X1. U31 and U35 select either this internal clock or an external clock and route it to the clock phase ring counter, which is made up of U13, U14, U16, and U56. The ring counter generates the 6-phase clock waveforms shown in figure 3. It can be thought of as a shift register, of which only one bit at a time is ever high. On the rising edge of every 30 MHz clock pulse, the bit shifts to the next higher stage. During T5, all the inputs to U56 are high, so the D input to U13 is high. Thus on the next rising edge of the 30 MHz clock, T0 goes high, and the clock phases start a new cycle. Because each phase of the clock is 33.3 nsec, an entire instruction will require 200 nsec for completion.

U67 divides the 30 MHz clock to 15 MHz before transferring it to the device controller board. This scheme was employed to reduce the electromagnetic interface (EMI) that introduces noise into the system.

3.2 ROM

The microprocessor control memory consists of twenty-four 256 × 4 bit read only memory chips located on the ECC/ROM PCA. These ROM's are organized as four banks (horizontal rows) of six ROM's per bank. This gives an instruction word length of 24 bits, and allows 1024 instructions to be stored in ROM. Since the ROM address field is 12 bits wide, the ROM size could easily be expanded to 4096 words.

Bank selection is done by U91 of the ECC/ROM board, which looks at the two most significant bits of the ROM address field (RAR 8 and RAR 9). The ROM's may be either 3-state or open collector. If open collector, four resistor pull-up packs must be loaded.

3.3 INSTRUCTION FLOW (Refer to Sheet 1 of the microprocessor schematics)

Figure 4 outlines the mechanism by which the ROM is accessed. The ROM address register (U33, U53, and U73) contains the address of the next instruction in ROM. The ROM output register (U61, U71, U81, U91, and U155) latches the 24-bit instruction while it is being executed and a new instruction is being accessed in ROM.

3.3.1 TIMING

If the RAR is clocked when PE (parallel enable) is low, the RAR loads; i.e., each output (0_0, 0_1, 0_2, 0_3, on each 74161 IC) assumes the value of the input (P_0, P_1, P_2, P_3). If it is clocked (by a rising edge on CP) when PE is high, the output is incremented and no loading takes place. Incrementing the RAR causes access to the next sequential instruction in ROM; loading the RAR causes a branch, where the next instruction's address has no relation to the current instruction's address.

The RAR has been designed to increment on the rising edge of T0 of every instruction. Therefore we want PE on the RAR to be high as T0 rises. Similarly, we want PE to be low as T2 rises, because during a branch the RAR will be clocked at T2 in order to load it with the branch address. As shown in figure 5, flip-flop U55 satisifes these conditions, putting a square wave on PE which is high as T0 rises and low as T2 rises.

U75 creates the RAR clock: a rising edge on T0 always, and a rising edge on T2 during a successful branch instruction.

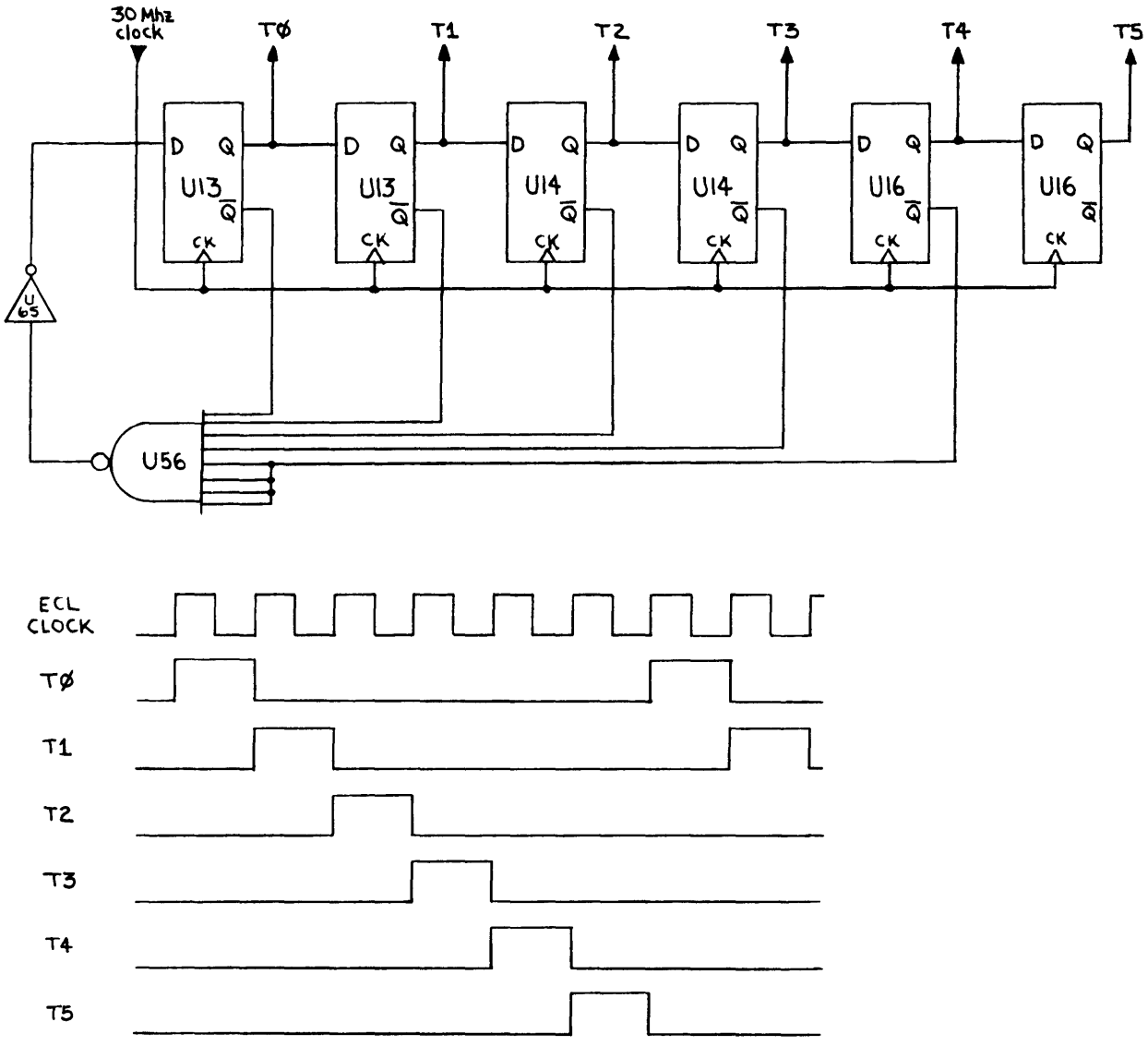


Figure 3. Clock Phase Generation

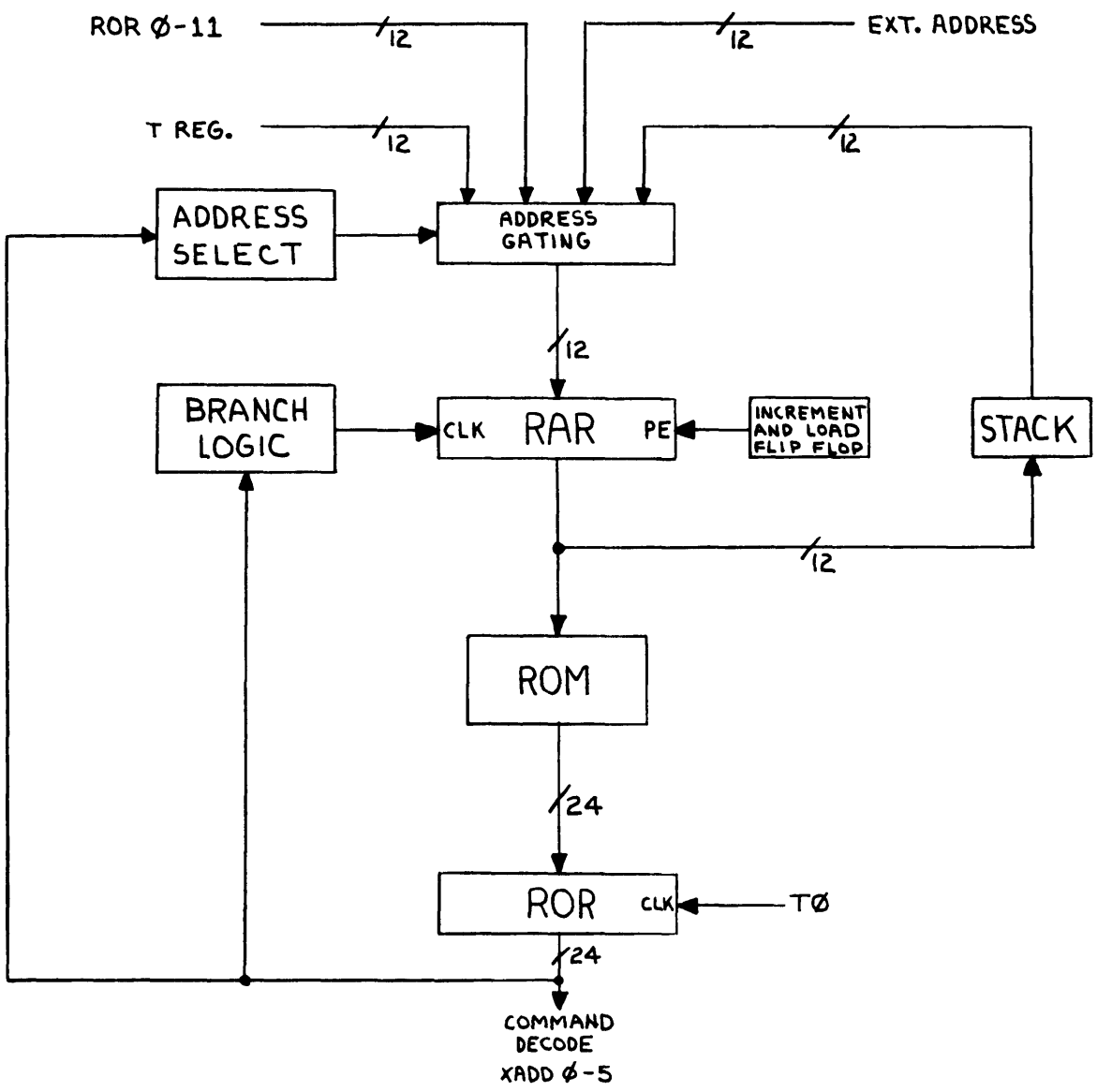


Figure 4. ROM Address Logic

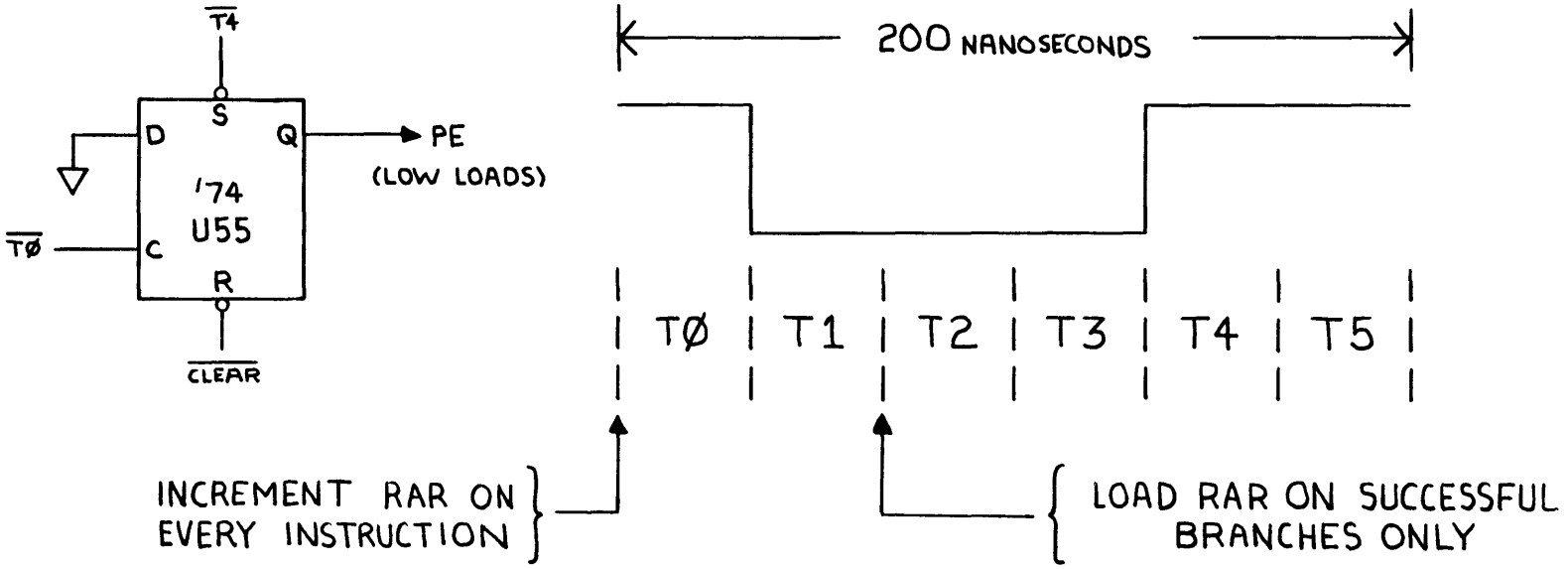


Figure 5. Increment/Load Flip-Flop and Timing

The ROR is always clocked on T0, so every instruction starts at T0. The ROM has completed its access; it is presenting the instruction word as the T0 clock rises and latches this word into the ROR. Recall that T0 is also the phase which increments the RAR. Thus we are strobing data out of the ROM on the same clock edge as we are changing the address to the ROM. No problem occurs since the ROM acess time is always greater than the ROR setup time. This scheme allows the ROM to be accessing for the full instruction time prior to the T0 edge which strobes its contents into the RAR. Two processes are thus occurring simultaneously: the instruction is being decoded and executed, and the next instruction is being looked up in ROM.

During a successful branch instruction, the RAR is loaded at T2 (refer again to figure 5).

3.3.2 RAR ADDRESS GATING

U22, U32, U42, U52, U62, and U72 are multiplexers which allow the RAR to be loaded with an address from one of four possible sources:

1. ROR bits 0 – 11 (corresponding to a direct branch); the destination address is the 12 least significant bits of the ROM instruction word.

2. an external address which has been keyed in from a service device attached to the controller; this feature allows an operator to start executing the microprogram at any desired address for diagnostic purposes.

3. the contents of the top level of the subroutine stack; this occurs when a return from a firmware subroutine is executed.

4. the contents of the T-register, which latches the output of the ALU on every instruction; this allows a microprogram to indirectly branch through a branch table in ROM, depending on the contents of the T-register.

Which of these four possible branches is taken depends on the levels on the 1Y and 2Y inputs (pins 2 and 14) of the RAR multiplexers. These levels are determined by U77 in accordance with the following table:

RAR Multiplexer

ROR 21	ROR 20	Selected
0	0	external address
0	1	direct branch
1	0	subroutine return
1	1	branch to T register contents

3.3.3 CONDITION CODE

Conditional branching in this microprocessor requires two instructions. The first instruction sets a condition code flip-flop (U55) depending on the state of an external flag or an internal condition. The second instruction is a branch instruction which succeeds when the condition code flip-flop is set, and fails when it is in the reset state. No loading of the RAR at T2 occurs on a branch that fails.

During a set condition code instruction, U121 or U131 selects an external flag (external to the microprocessor PCA) or a T-register condition, depending on bits 15 – 20 of the micro-instruction word. ROR 14 determines whether the selected condition is to be checked for true or false. It is exclusive-ORed with the output of U121 and U131 in U11 and fed to the condition code flip-flop U55. This data is clocked into the flip-flop only at T3 of a set condition code instruction. The preset input of this flip-flop goes low at T4 of a branch instruction, causing the flip-flop to set. This function was added so that if two branches are executed without an intervening SET CC instruction, the second branch will always succeed.

3.3.4 SUBROUTINE STACK

Subroutines are a useful feature of many programs because they allow a given section of code to be executed at many points within a program without the physical repetition of that code. When the programs are stored in a ROM, a means must be provided for storing the return addresses, so that the main program can resume at the correct place after the subroutine is complete. In this microprocessor, a 3-level, 12-bit subroutine stack provides this function. Composed of U23, U24, U34, U44, U54, U63, U64, and U74, it can store up to three return addresses, allowing three levels of subroutine nesting. These chips are wired so that during a CALL instruction, the contents of the RAR (which has been incremented to become the correct return address) is pushed onto the top of the stack (U34, U54, and U74). Also, the former contents of the top level of the stack are pushed onto level 2 (U24, U44, and U64), and the former contents of level 2 are pushed onto level 3 (U23 and U63). The contents of level 3 are lost during a CALL instruction. The opposite direction of data flow occurs during a RETURN instruction:

LEVEL 3 → LEVEL 3
LEVEL 3 → LEVEL 2
LEVEL 2 → LEVEL 1 (top)
LEVEL 1 → RAR

Every flip-flop in the stack is clocked at the rising edge of T2, on both a CALL and a RETURN instruction. The signal generated at pin 8 of U43 (STACKOP) supplies a positive-going edge at this time to clock U23 and U63. The other latches (U24, U34, U44, U54, U64, and U74) requires a negative edge to trigger, so U65 inverts STACKOP for them.

The WSEL (word select) input to the level 1 and level 2 flip-flops determines which set of inputs they read (and hence whether "popping" or "pushing" will take place). WSEL is high during a CALL and low during a RETURN.

4.0 ALU (Refer to Sheet 2 of the microprocessor schematics)

Arithmetic and logical operations are performed on two 16-bit words by the four ALU chips (U106, U126, U136, and U156). The function to be performed is determined by bits 16 through 20 of the arithmetic instruction word. These five bits are thus wired directly from the ROR to the M, S0, S1, S2, and S3 inputs of each of the ALU's. Full carry look-ahead is achieved by the 74S182 (U135). The ALU's always operate on two data words: one on the A bus, and one on the B bus (refer again to figure 1). No clocking is provided on the ALU chips. Rather, the data registers feeding the ALU's and the T-register following the ALU are clocked. Two sources exist for the data inputs to the ALU's: registers and immediate operands.

4.1 IMMEDIATE OPERANDS

Two types of instructions put immediate operands on the A bus: an immediate output, and an immediate arithmetic. U97 creates GIMOP (gate immediate operand) for these two instructions, which goes to one enable of U141 and U151 (the immediate operand drivers). The other enable of U151 goes to LB (lower byte), while the other enable of U141 goes to UB (upper byte). Immediate operands are only 8 bits long, and LB and UB determine whether they will be put onto the upper or lower byte of the A bus. Because the immediate operand replaces the A register during an immediate operand instruction, the A register outputs are not enabled so that there is no conflict.

4.2 REGISTERS

The four 16-bit A registers and four 16-bit B registers are implemented with eight 4 × 4 register files (U122, U123, U132, U133, U142, U143, U152, and U153). How these are assigned to upper and lower bytes of A and B registers is shown on sheet 2 of the microprocessor schematic. The data inputs to these registers (D_0, D_1, D_2, and D_3) are tied to the MIO bus. The data outputs go to the ALU inputs. The R_A and R_B control inputs specify the address (0, 1, 2, or 3) within each register file to be read out of. The W_A and W_B inputs specify one of four addresses to be written into. Two active low control enables, GW and GR, are also needed on each register file. They act as read and write clocks.

4.2.1 WRITE

When GW is low, data is written from the MIO bus into the register file. On sheet 2 of the microprocessor schematic, U124, U134, U144, and U154 combine $\overline{\text{AWEN}}$, $\overline{\text{BWEN}}$, $\overline{\text{LBG}}$, and $\overline{\text{UBG}}$ to lower the appropriate GW's during T4 of any instruction which requires writing into a register. Arithmetic instructions and I/O input instructions require writing into a register. The signal $\overline{\text{CLD}}$ (clock data) reflects this fact (it is the NOR of IOIN and ARITH on sheet 3 of the microprocessor schematic, and must be low to allow writing into a register).

$\overline{\text{LBG}}$ (lower byte gated) — same as LB except only goes low during T4.

$\overline{\text{UBG}}$ (upper byte gated) — same as UB except only goes low during T4.

$\overline{\text{AWEN}}$ — A register write enable.

$\overline{\text{BWEN}}$ — B register write enable.

4.2.2 READ

When GR is low, data is read out of the register file and onto the ALU input lines. $\overline{\text{LB}}$ is tied directly to GR of the B register lower byte, and $\overline{\text{UB}}$ goes directly to GR of the B register upper byte. Thus one byte or both bytes of the B register is always sent to the ALU inputs during an arithmetic or I/O instruction. U144, however, only allows $\overline{\text{LB}}$ or $\overline{\text{UB}}$ to drive GR low on the corresponding A register when GIMOP (gate immediate operand) is low. Thus the A inputs to the ALU are fed either by an immediate operand, or by the A register, but not both.

4.3 T-REGISTER

U94, U104, and U114 comprise a 16-bit register which latches the result of an ALU operation on the trailing edge of T2. U134 combines $\overline{\text{T2}}$ and $\overline{\text{ENSHIFT}}$ to clock this T-register. $\overline{\text{ENSHIFT}}$ is generated by U97 pin 8 to be low only when ROR 23 is low and IOIN (I/O INPUT) is low; i.e., during an ARITH, OTI, or I/O OUT instruction.

4.4 PROCESSOR STATUS REGISTER

During any instruction which clocks the T-register, the state of the T-register is latched in the 6-bit processor status register (U111). U95, U115, and U124 NAND together the 16 ALU outputs to produce TNZRO, which is high if any bit (or bits) of the ALU output is one. EQUAL goes high if the words on the A and B input busses to the ALU are the same. UOVER and LOVER go high if there is a carry out of the upper or lower bytes, respectively. MSB and LSB go high if the most significant bit or least significant bit, respectively, are ones.

The 6 outputs of the processor status register go to U121, where any one of them can be tested by a SET CC instruction.

4.5 SHIFTER

U82, U83, U92, U93, U102, U103, U112, and U113 form the shifter, which receives the output of the ALU, shifts it, and puts it onto the MIO bus. Allowable shifts are shift left, shift right, rotate left, rotate right, swap bytes, and pass. Except for bits 0 and 15, the shifter selects each bit from one of four possible sources. Bit i ($i \neq 0, 15$) comes from:

1. bit i of the T register (pass)
2. bit $i - 1$ of the T register (shift left, rotate left)
3. bit $i + 1$ of the T register (shift right, rotate right)
4. bit $i \pm 8$ of the T register (swap bytes)

This observation allows the shifter to be built from one-of-four data selectors, rather than a complex shift register. Each of the 8 shift chips contains two one-of-four data selectors. The inputs are wired to the T-register in accordance with the above table. The outputs of the shifter go directly to the MIO bus. U124 makes the distinction between shift and rotate for bits 1 and 15 in accordance with $\overline{\text{ROT}}$, which comes from ROR 6.

The select inputs to the shifter chips are functions of ROR 4, ROR 5 and PASS:

	ROR 6	**ROR 5**	**ROR 4**
Swap	X	0	0
Rotate right	0	0	1
Shift right	1	0	1
Rotate left	0	1	0
Shift left	1	1	0
Pass	X	1	1

From the above table, $\text{ROR 4} \cdot \overline{\text{ROR 5}}$ = rotate or shift right
$\overline{\text{ROR 4}} \cdot \text{ROR 5}$ = rotate or shift left
$\text{ROR 4} \cdot \text{ROR 5}$ = pass

PASS is GIMOP or I/O OUT (page 3 of the microprocessor schematics) since no shift should occur on instructions involving immediate operands or on I/O output instructions.

Pin 3 of U144 and pin 3 of U154 control the enables on the shifter chips. $\overline{\text{LB}}$ and $\overline{\text{UB}}$ determine whether the upper byte, the lower byte, or both bytes of the shifter output will be enabled onto the MIO bus. In addition, $\overline{\text{ENSHIFT}}$ must be low for the shifter to drive the MIO bus. This happens for ARITH, OTI, and I/O OUT instructions.

4.6 SIGNAL POLARITY

The MIO bus is ground true. A logical one is a zero volt signal and a logical zero is a 4.7 volt signal. The input bus to the ALU's is also ground true. The immediate operand drivers which drive this bus (U141 and U151) are inverters, since the immediate operand field of a micro-instruction comes out of the ROR (and ROM) plus true. The pull-up resistors on the 74170 register files ensure that when a file's output is not enabled, the line goes to +5.0 volts (which the input of the ALU regards as a logical zero). Thus when an ARITH instruction specifies operations on only one byte, the register files corresponding to the other byte are not enabled, and the ALU sees logical zeros on the inputs corresponding to the disabled byte.

5.0 INSTRUCTION DECODING

(Refer to Sheet 1 of the microprocessor schematics)

Besides the ROR and the clock circuitry, all of the chips on sheet 3 of the schematic perform instruction decoding. Based on the current instruction in the ROR, they generate the signals which operate the ALU. U86 decides which of the four basic types of instruction is being executed. It is a 2-line-to-4-line decoder which decodes bits 23 and 22 of the ROR into one of the following:

1. IOINST = $\overline{\text{ROR 23}} \cdot \overline{\text{ROR 22}}$ (also EX SEL to the device controller board)
2. ARITH = $\overline{\text{ROR 23}} \cdot \text{ROR 22}$
3. BRINST = $\text{ROR 23} \cdot \text{ROR 22}$
4. SET CC = $\text{ROR 23} \cdot \overline{\text{ROR 22}}$

5.1 U101

U101 is a quad 2-input data selector that selects XADD0 and XADD1 from one of two sources. During an OTI (output immediate) instruction, they come from ROR bits 8 and 9. During an IOC instruction, they come from ROR bits 8 and 9. During an IOC instruction, they come from ROR bits 5 and 6. In both cases, XADD0 and XADD1 go through the P2 connector to the device controller board, where they join XADD 2, 3, 4, and EX SEL in selecting an external register.

ID1 and ID2, which determine what word (0, 1, 2, or 3) of a register is written into, have two possible sources. During an ARITH instruction, they come from ROR bits 10 and 11. During an IOC instruction, ROR bits 2 and 3 are the sources.

5.2 I/O DECODING

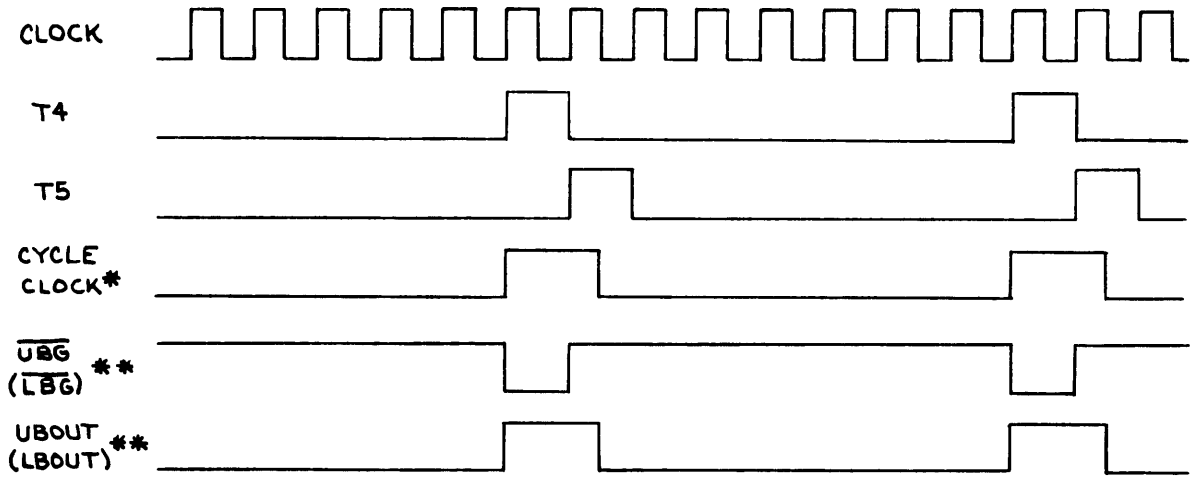
U96 (pins 11 and 12) separates all I/O instructions into either OTI (output immediate) or IOC (I/O control). U86 (pins 6 and 9) further divides IOC instructions into input (INPUT) or output (I/O OUT) types on the basis of ROR 0. I/O OUT is ORed with $\overline{\text{ROR 23}} \cdot \overline{\text{ROR 21}}$ to form PASS, which directs the shifter not to shift. INPUT is sent through P2 to the device controller board where it determines whether some of the registers drive or receive from the MIO bus.

The IOIN (as well as ARITH) command allows selection and subsequent writing into a register. The register group is selected by U145. The $\overline{\text{AWEN}}$ and $\overline{\text{BWEN}}$ signals are generated by ROR bit 15 and ROR bit 1, respectively (ROR bit 15 and ROR bit 12 for ARITH commands). As previously described, U101 provides gating for the number of the selected group (via ID1 and ID2) into which the information is written (i.e., A3 or B0, etc.).

5.3 BYTE SELECTION

U96 (pins 6 and 9) creates $\overline{LB}$ and $\overline{UB}$ based on ROR bit 13 (U/L field), ROR bit 7 (FW field), and ROR bits 21 and 23. $\overline{LB}$ specifies lower byte when it is low, and $\overline{UB}$ specifies upper byte. When both are low, a full word instruction is specified. U85 (pins 8 and 6) creates $\overline{LBG}$ $(\overline{LB \cdot T4})$ and $\overline{UBG}$ $(\overline{UB \cdot T4})$, which are used in the ALU section.

UBOUT and LBOUT are generated by U125 (pins 11 and 6) and sent to the device controller board. They are the same as UB and LB in that they become true at the beginning of T4, but they return false at the middle of T5 (instead of at the end of T4); this falling edge latches the contents of the MIO bus into the appropriate device controller register. The middle of T5 had to be chosen to ensure enough data propagation time, as attenution of the signal occurs before it reaches the device controller PCA. U57 creates this positive-going stretched pulse called CYCLE CLOCK, which remains high through the first half of T5 and which strobes LBOUT and UBOUT (see figure 6).



* ALWAYS PRESENT (GATED TO LBOUT AND UBOUT LOGIC THROUGH U57 BY AN OTI OR IOOUT INSTRUCTION).

** ONLY PRESENT WHEN ENABLED BY UB OR LB SELECTION (U/L FIELD OR FW FIELD).

Figure 6. Byte Selection Timing

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60001
13037-68001

DATE CODE : K-2301

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C1	0160-2055	CAP .01UF-20+80%
C10	0180-0374	CAP 10UF 10%
C11	0160-2207	CAP 300PF 5%
C12	0160-2055	CAP .01UF-20+80%
C13	0160-2055	CAP .01UF-20+80%
C14	0160-2055	CAP .01UF-20+80%
C15	0160-2055	CAP .01UF-20+80%
C16	0160-2055	CAP .01UF-20+80%
C17	0160-2055	CAP .01UF-20+80%
C18	0160-2055	CAP .01UF-20+80%
C19	0160-2055	CAP .01UF-20+80%
C2	0160-2055	CAP .01UF-20+80%
C20	0160-2055	CAP .01UF-20+80%
C21	0160-2055	CAP .01UF-20+80%
C22	0160-2055	CAP .01UF-20+80%
C23	0160-2055	CAP .01UF-20+80%
C24	0160-2055	CAP .01UF-20+80%
C25	0160-2055	CAP .01UF-20+80%
C26	0160-2055	CAP .01UF-20+80%
C27	0160-2055	CAP .01UF-20+80%
C28	0160-2055	CAP .01UF-20+80%
C29	0160-2055	CAP .01UF-20+80%
C3	0160-2055	CAP .01UF-20+80%
C30	0160-2055	CAP .01UF-20+80%
C31	0160-2055	CAP .01UF-20+80%
C32	0160-2055	CAP .01UF-20+80%
C33	0160-2055	CAP .01UF-20+80%
C34	0160-2055	CAP .01UF-20+80%
C35	0160-2055	CAP .01UF-20+80%
C36	0160-2055	CAP .01UF-20+80%
C37	0160-2055	CAP .01UF-20+80%
C38	0160-2055	CAP .01UF-20+80%
C39	0160-2055	CAP .01UF-20+80%
C4	0160-2055	CAP .01UF-20+80%
C40	0180-0374	CAP 10UF 10%
C5	0160-2055	CAP .01UF-20+80%
C6	0160-2055	CAP .01UF-20+80%
C7	0121-0046	CAP 9-35PF
C8	0160-2055	CAP .01UF-20+80%
C9	0160-2055	CAP .01UF-20+80%
CR1	1990-0327	DIODE-LIGHT EMIT
CR2	1990-0327	DIODE-LIGHT EMIT
E1	0360-0294	TERM-SOLDER STUD
E2	0360-0294	TERM-SOLDER STUD
E3	0360-0294	TERM-SOLDER STUD
E4	0360-0294	TERM-SOLDER STUD
E5	0360-0294	TERM-SOLDER STUD

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60001
13037-68001

DATE CODE : K-2301

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
E6	0360-0294	TERM-SOLDER STUD
L1	9100-2260	COIL FXD 1.8UH
MP10	0624-0077	SCR TAP 4-40X.31
MP11	5040-6009	EXTRACTOR PC
MP12	1480-0116	PIN GRV .062X.25
MP13	7120-4325	LABEL-INFO
MP14	5020-7318	SPACER
MP9	5040-6058	BRACE-PC BOARD
R1	1810-0030	RES NET 7X1K
R11	1810-0080	RES NET 7X500
R12	1810-0080	RES NET 7X500
R13	1810-0080	RES NET 7X500
R14	1810-0080	RES NET 7X500
R15	0683-1025	RES 1000 5% .25
R16	0757-0416	RES 511 1%.125
R17	0757-0416	RES 511 1%.125
R18	0757-0416	RES 511 1%.125
R19	0757-0416	RES 511 1%.125
R2	0757-0280	RES 1K 1%.125
R20	0757-0279	RES 3.16K 1%.125
R21	0757-0407	RES 200 1%.125
R22	0757-0407	RES 200 1%.125
R3	0683-2715	RES 270 5% .25
R4	0683-5615	RES 560 5% .25
R5	0683-2715	RES 270 5% .25
R6	0683-8205	RES 82 5% .25
R7	0683-1215	RES 120 5% .25
R8	0757-0280	RES 1K 1%.125
R9	0698-3429	RES 19.6 1%.125
U101	1820-0616	IC 9322PC
U102	1820-2287	SN745253
U103	1820-2287	SN745253
U104	1820-1191	IC SN74S175N
U105	1820-0683	IC SN74S04N
U106	1820-0999	IC SN74S181N
U11	1820-0694	IC SN74S86N
U111	1820-1076	IC SN74S174N
U112	1820-2287	SN745253
U113	1820-2287	SN745253
U114	1820-1076	IC SN74S174N
U115	1820-1323	IC SN74S30N
U12	1820-0683	IC SN74S04N
U121	1820-0622	IC SN74151N
U122	1820-0725	IC-MEMORY
U123	1820-0725	IC-MEMORY
U124	1820-1449	IC SN74S32N
U125	1820-0239	IC MC3002P

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60001
13037-68001

DATE CODE : K-2301

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U126	1820-0999	IC SN74S181N
U13	1820-0693	IC SN74S74N
U131	1820-0640	IC SN74150N
U132	1820-0725	IC-MEMORY
U133	1820-0725	IC-MEMORY
U134	1820-1449	IC SN74S32N
U135	1820-1305	IC SN74S182N
U136	1820-0999	IC SN74S181N
U14	1820-0693	IC SN74S74N
U141	1820-0760	IC HP106B
U142	1820-0725	IC-MEMORY
U143	1820-0725	IC-MEMORY
U144	1820-1449	IC SN74S32N
U145	1820-0063	IC SN7451N
U151	1820-0760	IC HP106B
U152	1820-0725	IC-MEMORY
U153	1820-0725	IC-MEMORY
U154	1820-1449	IC SN74S32N
U155	1820-1076	IC SN74S174N
U156	1820-0999	IC SN74S181N
U16	1820-0693	IC SN74S74N
U21	1820-0683	IC SN74S04N
U22	1820-0998	IC SN74S153N
U23	1820-0788	IC SN74174N
U24	1820-1100	IC SN74298N
U31	1820-0681	IC SN74S00N
U32	1820-0998	IC SN74S153N
U33	1820-0716	IC SN74161N
U34	1820-1100	IC SN74298N
U35	1820-0681	IC SN74S00N
U37	1820-0808	IC MC10111P
U42	1820-0998	IC SN74S153N
U43	1820-0069	IC SN7420N
U44	1820-1100	IC SN74298N
U52	1820-0998	IC SN74S153N
U53	1820-0716	IC SN74161N
U54	1820-1100	IC SN74298N
U55	1820-0693	IC SN74S74N
U56	1820-1323	IC SN74S30N
U57	1820-0681	IC SN74S00N
U61	1820-1076	IC SN74S174N
U62	1820-0998	IC SN74S153N
U63	1820-0788	IC SN74174N
U64	1820-1100	IC SN74298N
U65	1820-0683	IC SN74S04N
U67	1820-0693	IC SN74S74N
U71	1820-1076	IC SN74S174N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60001
13037-68001

DATE CODE : K-2301

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U72	1820-0998	IC SN74S153N
U73	1820-0716	IC SN74161N
U74	1820-1100	IC SN74298N
U75	1820-1158	IC SN74S51N
U76	1820-0681	IC SN74S00N
U77	1820-0681	IC SN74S00N
U81	1820-1076	IC SN74S174N
U82	1820-2287	SN745253
U83	1820-2287	SN745253
U84	1820-1449	IC SN74S32N
U85	1820-0681	IC SN74S00N
U86	1820-0843	IC MC4002P
U87	1820-0683	IC SN74S04N
U91	1820-1076	IC SN74S174N
U92	1820-2287	SN745253
U93	1820-2287	SN745253
U94	1820-1076	IC SN74S174N
U95	1820-1323	IC SN74S30N
U96	1820-0843	IC MC4002P
U97	1820-1449	IC SN74S32N
Y1	0410-0137	XTAL 30MHZ 3RD

END OF MATERIAL LIST.

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	DJW/GA	1-25-73
B	UPDATED FROM PILOT RUN NOW B-1440-22	DJW/GA	11-4-74
C	PC22-2503 ON SHT. 3 C11 WAS 100PF	GD/GA	3-18-75
D	PC22-3290-CIRCUIT CHG, DATE CODE C-1620	GD/MK	5-19-76
E	PC22-3647-CIRCUIT CHG, DATE CODE C-1640	GD/JR	11-12-76
F	U55 WAS 7474 PC48-0392.	K.LARSON	3-13-78
G	UPDATED SYMBOLS PC48-0452.	LO/EC.	4-21-78
H	CURRENT DATE CODE F-1808 PC48-3434 REV.B	[illegible]	9-4-81
J	CURRENT DATE CODE G-1808 PC48-3565	[illegible]	[illegible]
K	CURRENT DATE CODE H-1808 PC 48-3343	K.F./MSM	12.7.81
L	CURRENT DATE CODE J-3000 PC48-5433.	[illegible]	9-2-83
M	CURRENT DATE CODE K-2301 CD48-0480	[illegible]	1-5-83

13037-60001-51

+5V: P1 1-4
J1 7-10
GRND: P1 11-16
P1 19,20,29,30,42
43,47,50,54,55
P2 1,50
P3 1-49 ODD NO'S. ONLY
J1 1,2,49,50
J2 1,2,49,50

SPARE IC'S:

74500	U31B
74504	U65F, U105CD
7420	U43A
74532	U97B, U134A
74574	U67B
74586	U11BD
745174	U155F
745175	U26D

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005
SEE CORP. STD. 608

DRAWN BY: DATE: 1-25-73
ENGINEER: DATE: 11-1-74
RELEASE TO PROD.: DATE: 12/12/74
SUPERSEDES DWG.:

TITLE: CONTROLLER U-PROCESSOR SCHEMATIC
NEXT ASSEMBLY: 13037 A-B
FINISH: SCALE:

HEWLETT PACKARD
PART NUMBER: 13037-60001
D-13037-60001-51
SHEET OF

D-13037-60001-52

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		1-25-73
B	UPDATED FROM PILOT RUN B-11440-22		11-4-74
C	PC22-2503, SHT 3 CHWAS 100pf		3-12-75
D	PC22-2932, CIRCUIT CHG DATE CODE B1530-22	GD/MK	10-23-75
E	PC22-3290 CHG IC 3 NO. DATE CODE C-1620	GD/MK	5-20-76
F	CORRECTED ERRORS, PC48-0452.	L.O./EC	4-20-78
G	ADDED 745253. PC48-2113.	L.O./	12-26-78
H	CURRENT DATE CODE F-1808 PC 48-3436	K.F./MJM	9.4.81
J	CURRENT DATE CODE G-1808 PC48-3565		10.28.81
K	CURRENT DATE CODE H-1808 PC 48-3343	K.F./MJM	12.7.81
L	CURRENT DATE CODE J-3000 PC48-5433		9-2-83
M	CURRENT DATE CODE K-2301 C048-0480		1-5-85

ENGINEERING RESPONSIBILITY — SEPIA

0	1	2	3	4	5	6	7	8	9	10	11	12	14	15	
16	17		19		21	22	23	24	25	29	30	32	35	38	43
45	46	61	63						85						

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L PART NO.	MAT'L DWG. NO.	MAT'L SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY		12-14-73
ENGINEER		11-1-74
RELEASE TO PROD.		12/12/74
SUPERSEDES DWG.		

SCHEMATIC CONTROLLER U-PROCESSOR ARITH. SECTION

SEE KARDEX

FINISH — SCALE

HEWLETT PACKARD

13037-60001

PART NUMBER D-13037-60001-52

SHEET 1 OF 1

D-13037-60001-53

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15 16 17 18 19 20 21 22 23 41 42 43	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		1-27-73
B	UPDATED FROM PILOT RUN (NOW B-1000-22)		11-4-74
C	PCO-22-3703 W/USE3 CH WAS 1808E		3-18-75
D	PCO-22-3732, CHG. CIRCUIT DASH # FROM 15 B-1520	GB/	10/24/75
E	PCO-22-3390, CIRCUIT AND I.C'S CHG, DATE CODE IS C-1620	GB/	5/4/76
F	PCO-22-3617, CIRCUIT CHG, DATECODE IS B-1660	GB/	11/12/76
G	CORRECTED CONNECTIONS TO U114-2 AND 5 WAS MISSED ON PCO-22-3617	GB/	3/17/77
H	UPDATED SYMBOLS PC48-0452	EG 4-28-78	
J	ADDED NOTE 1 PC48-2965 REV B	5-12-81	
K	CURRENT DATE F-1808 PCO 48-3436 REV. B	9.4.81	
L	CURRENT DATE CODE G-1808 PC48-3565	12.26.81	
M	CURRENT DATE H-1808 PCO 48-3343	12.7.81	
N	CURRENT DATE CODE J-3000 PC 48-5433	9-2-83	
P	CURRENT DATE CODE J-2301 CO 48-0480	1-5-83	

NOTE:
1. SQUARE POLARITY PAD ON LED'S INDICATE ANODE CONNECTION. THIS BOARD ONLY.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED.
DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY — DATE 2-26-73
ENGINEER — DATE 11-1-74
RELEASE TO PROD. — DATE 3/11/74
SUPERSEDES DWG.

SCHEMATIC
CONTROLLER µ-PROCESSOR
TITLE

NEXT ASSEMBLY 13037A/B
FINISH
SCALE

HEWLETT PACKARD

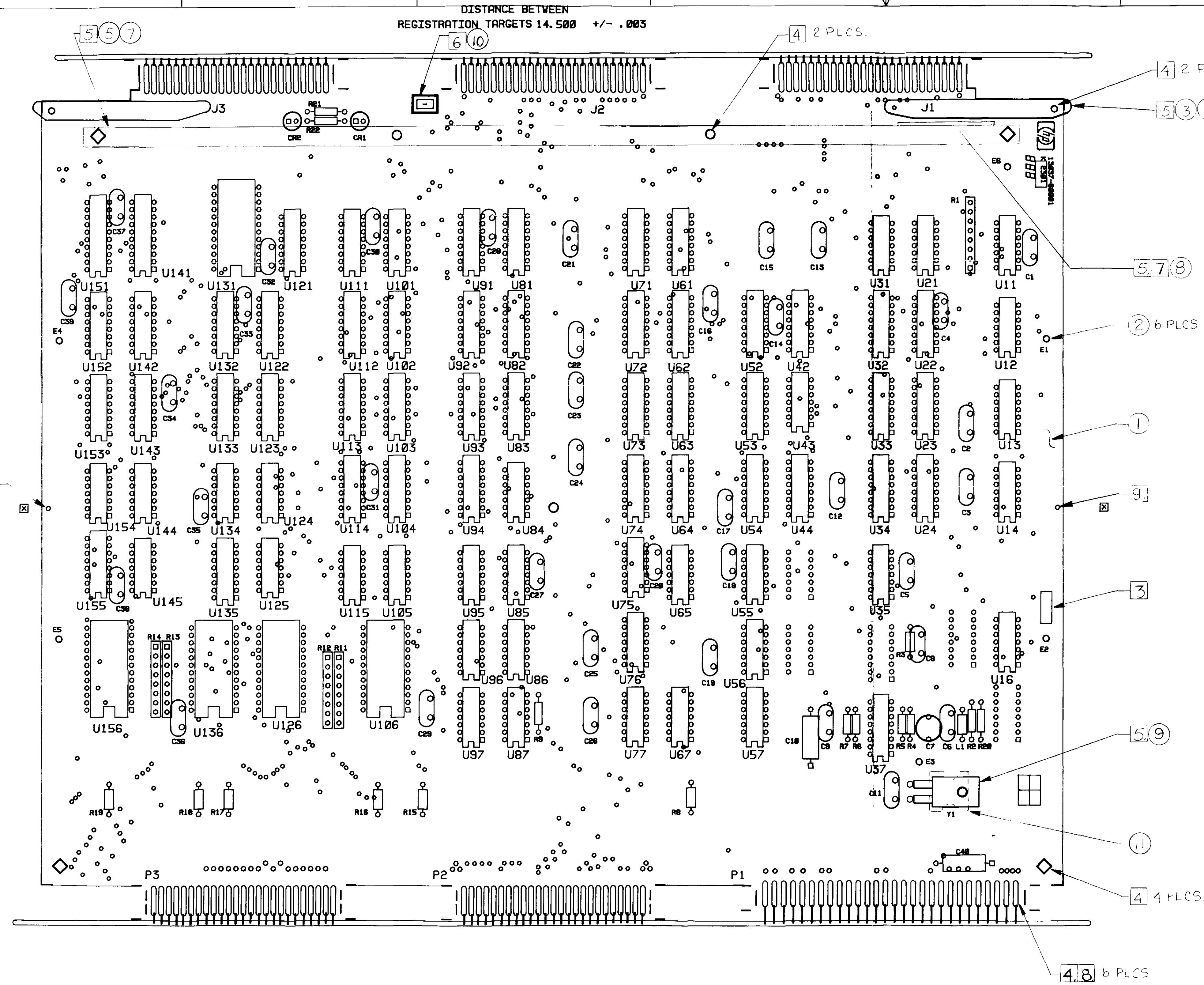
PART NUMBER D-13037-60001-53

SHEET 1 1

ENGINEERING RESPONSIBILITY	SEPIA	AP/C A

D-13037-60001-6

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-5433/A		
B	CURRENT DATE CODE K-2301 C048-0480	NW PJP	12-20-83



REFERENCE DRAWINGS:
SCHEMATIC D-13037-60001-51, 52, 53.

NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE IN OHMS.
   ALL RESISTORS 1/4 W 5%.
   ALL RESISTOR NETWORKS 1810-0080.
   ALL CAPACITANCE IN MICRO FARADS.
   ALL CAPACITORS .01 CERMAIC DISC.
   ALL IC'S ARE 1820-
2. ARTWORK DATE 12-27-83 .
3. PC PRODUCTION: MARK ASSEMBLY WORK ORDER NUMBER: COMPONENT SIDE ONLY.
4. MASK PRIOR TO LOADING.
5. TOUCH UP, INSTALL (3) THROUGH (9)
6. INSTALL (10) AFTER LINE TEST.
7. ITEM (8) MUST BE 1 INCH FROM RIGHT EDGE OF BRACE.
8. CLEAN FINGERS IN TOUCH UP.
9. BOARD ERROR CORRECTION HOLES.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
11	1	SOCKET XTAL	1200-0546		
10	1	INFO LABEL	7120-6830		
9	1	CRYSTAL	0410-0137		
8	1	INFO. LABEL	7120-4325		
7	1	BRACE, PC BOARD	5040-6058		
6	1	SPACER	5020-7318		
5	5	SCREW	0624-0077		
4	2	EXTRACTOR	5040-6009		
3	2	PIN	1480-0116		
2	6	TERMINAL E1-E6	0360-0294		
1	1	BOARD ETCHED	13037-80001		

DRAWN BY	DATE 12-27-83	TITLE BOARD ASSEMBLY, MICRO PROCESSOR	HEWLETT PACKARD
ENGINEER		NEXT ASSEMBLY SEE WHERE USED	PART NUMBER 13037-60001
RELEASE TO PROD.			
SUPERSEDES DWG.		FINISH —— SCALE 2:1	D-13037-60001-6

SHEET 1 OF 1

CONTENTS

Page

1.0 DEVICE CONTROLLER CHARACTERISTICS 4-1
2.0 HARDWARE DESCRIPTION 4-3
2.1 Formatter/Separator Clock 4-3
2.2 Data Formatter 4-4
2.3 Data Separator 4-6
2.3.1 Separator Control and Clock Select Logic 4-6
2.3.2 Phase Comparator and VCO 4-7
2.3.3 Final Decoding Logic 4-12
2.4 SERDES, EOW, and $\overline{\text{SYNC}}$ 4-13
2.5 CRCC 4-16
2.6 Timeout Circuitry 4-16
2.7 RAM 4-17
2.8 Function Decoder 4-18
2.8.1 Control Bus Hardware 4-18
2.8.2 Interface Bus Hardware 4-18
2.8.3 Interface Function Bus Hardware 4-19
2.8.4 Retry/Initial and New Track Flags 4-19
2.8.5 Tag Bus Hardware 4-19
2.8.6 Internal Control Word Hardware 4-19
2.8.7 File Mask and EOC Hardware 4-20
2.8.8 Interface Function Validation 4-20
2.9 Power On and Power Fail Circuitry 4-20
2.10 Drive Receivers and Transmitters 4-20
2.11 Flag Buffer and Overrun 4-22
APPENDIX I: Disc Drive Interface 4-23
APPENDIX II: Computer Interface 4-31

DEVICE CONTROLLER PCA

1.0 DEVICE CONTROLLER CHARACTERISTICS

The device controller PCA, like the microprocessor and ECC PCA's, resides on a single 3000-size printed circuit board. This board communicates with the microprocessor PCA via the MIO bus, five external address lines, and various flags; in turn the device controller sends and takes information from the disc drive and CPU interface (via various dedicated bus lines and flags), as well as controlling the operation of the ECC/ROM board. 5 volt current consumption is 4.5 amps.

Communication of data to or from the disc drive requires proper formatting or separating of that data. The process of formatting the information requires proper mixing of the 7.5 MHz data rate clock with the data to be recorded such that upon reading, these two signals can be properly separated. An MFM (modified frequency modulation) type encoding is used, employing the following rules:

1) a transition is made in the middle of all "1" bit cells;

2) a transition is made at the boundary of two adjacent "0" bit cells.

Such encoding helps minimize effects of pulse crowding as well.

Before the encoded data is passed to the disc drive for writing, precompensation of the data stream is employed to circumvent the effects that the disc media introduces upon recording. These effects include those of d.c. offset upon playback, and overlapping effects of crowded pulses.

As previously mentioned, reading data from the disc requires separating the data clock from the written data. Allowances also must be made for the fact that the speed of the disc upon playback may differ from that when recording. Thus, the separator locks onto the nominally 7.5 MHz data stream and, utilizing a phase lock loop and appropriate decoding hardware, obtains the original recorded data. The data clock separated from the encoded data is used to clock other hardware, including the ECC hardware (described in the next section) and the CRCC (cyclic redundancy code check) hardware.

The CRCC section of the device controller originally was to be the only resident error indicator employed on the 13037A. However, the ECC hardware became standard equipment before the disc controller was released, and hence the CRCC is used only to indicate any data error. (The ECC decides whether it is correctable, and what is needed to correct it.)

During a WRITE operation, serial data is shifted through the CRCC hardware; at the end of the data field, a characteristic CRCC word has been produced for the preceding data, and this 16-bit word is now serially transferred to the disc. Upon reading, all information through (and including) the CRCC word is clocked through the CRCC hardware; at the end of the CRCC word the contents of the CRCC register are examined, and if any bit is not zero, the CRCC hardware reports a data error via an appropriate flag.

In reading or writing operations, one encounters times when serial data must be converted to parallel data (i.e., during a READ command), and vice versa (i.e., during a WRITE command). Such conversions are handled in the SERDES (serial-deserializer) hardware when appropriate.

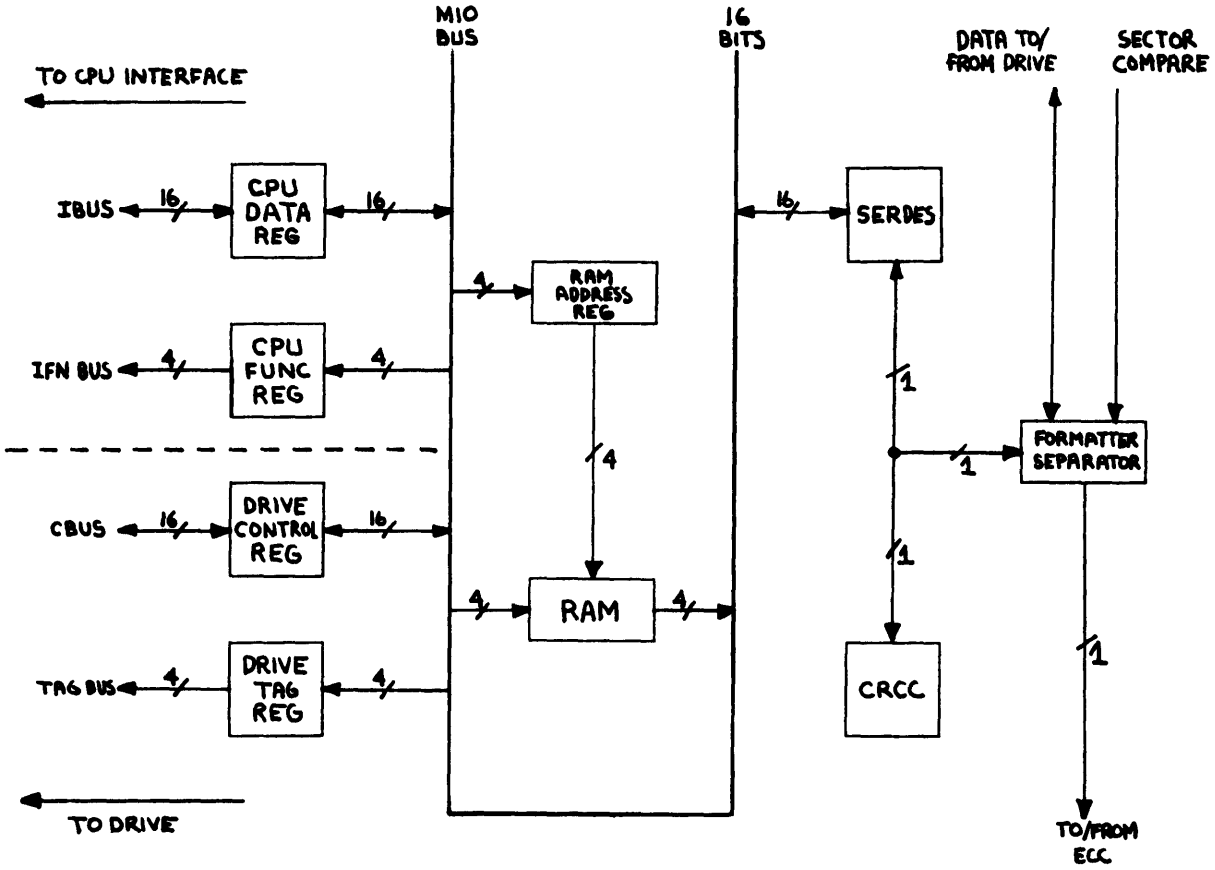


Figure 1. Device Controller Block Diagram

The SERDES hardware, as well as the bus buffers and latches, RAM and RAM address logic, and ICW (internal control word) hardware, is firmware controlled via the XADDR lines from the microcomputer board. These lines drive a MUX, enabling a specific hardware function selected by the microcode. When enabled, the selected hardware will (when appropriate) combine various external signals (i.e., LBOUT or UBOUT, INPUT, etc.) with relevant MIO bus lines to generate system flags, set up the file mask, validate data transfers, or perform other indicated tasks.

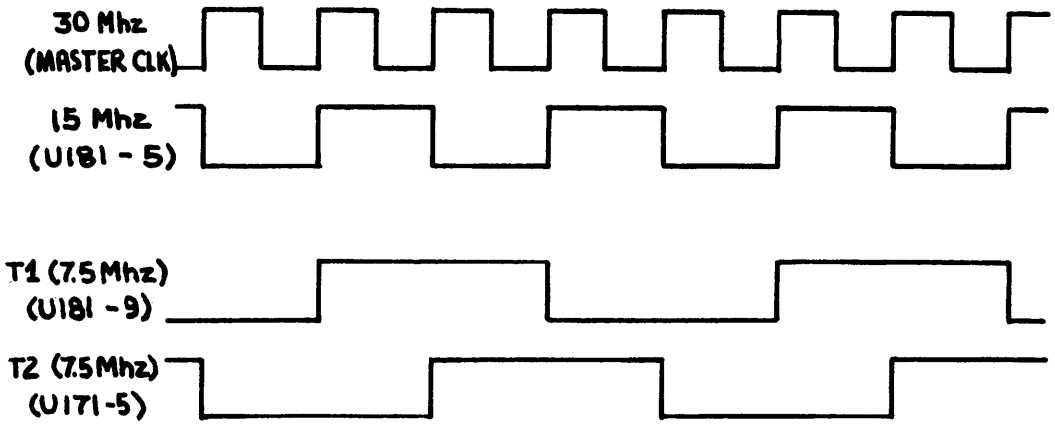
The ICW hardware, selected as described above and driven by the MIO bus, sets up various signals enabling reading, writing, and other functions (including enabling or disabling ECC shifts). The ICW (taken from the MIO bus) is latched into an ICW register until another microcode command overwrites that information.

A basic device controller block diagram is shown in Figure 1. The next section will describe these blocks and other hardware in more detail.

2.0 HARDWARE DESCRIPTION

2.1 FORMATTER/SEPARATOR CLOCK

U181 is a D-type flip-flop that functions as an R-S flip-flop with a 15 MHz input signal derived from the 30 MHz master clock on the microcomputer board (older versions take the 30 MHz directly from the master clock and incorporate U181 as a "divide-by-two" counter); this 15 MHz clock is divided by U171 and the other half of U181 into a two phase, 7.5 MHz clock incorporated by the formatter in encoding the data (the 7.5 MHz is used by the separator only as a sequence timing clock and PLL holding frequency). The relationship between the clock phases is shown below.



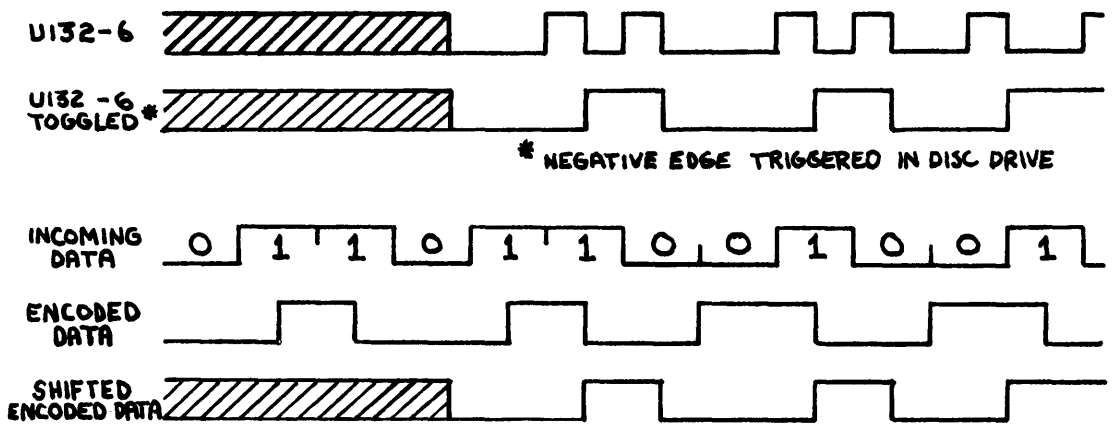
The falling edge of T2 will delineate the bit cell boundaries of the data when encoding, as will be described later in the next section.

2.2 DATA FORMATTER

With $\overline{\text{SECTOR COMPARE}}$ and WRITE both true, U189-6 provides a high WRITE GATE level (U142-2 generates a low $\overline{\text{WRITE GATE}}$ level) that enables various formatter hardware. Data to be written is provided at a 7.5 MHz system rate to U169-2, and appears at U161-4. U161 is a 74S175 quad D-type flip-flop incorporated as a 4-bit shift register through which incoming serial data is clocked to $\overline{T2}$. The various outputs are utilized in detecting "1's", "0" pairs, and the two data patterns requiring precompensation before writing onto the disc ("1101", "1011").

U143-11 goes high on detection of a "0" pair; this event is clocked into U151 by T1 (U181-9) "1's" are clocked into U141 by $\overline{T1}$. The cases of 1101 and 1011 are detected by U162-8 and U162-6 respectively; these events are clocked into U121 and U131 (both D-type flip-flops) by the output of U132-6 delayed 40 nanoseconds (more will be said about this later). U133-8 and U133-6, in conjunction with $\overline{T2}$ and T2, gate the "one" and "zero pair" signals through at the proper time for mixing by U132. U132-6 thus produces an encoded output which, when passed through the toggle flip-flop in the disc drive, gives the encoded signal to be written onto the disc.

Figure 2 outlines the relationship between the various signals for a sample data stream. (Shown below is the relationship between the encoded data and U132-6 clocking a toggle flip-flop.) The 3.5-bit cell delay of the formatter encoded data is the result of the combined delay of the shift register and event detection latches.



Although the data is successfully encoded at U132-6, precompensation must be applied to patterns 1101 and 1011 to circumvent media effects when writing (signals are delayed or advanced, respectively, to move the inner "one's" of 1101 and 1011 patterns away from the adjacent zero bit cell). This compensation is accomplished by passing the signal at U132-6 through U152, a 100-nanosecond delay line with 10-nanosecond taps. Normal data is delayed 30 nanoseconds and passed to U153 for subsequent gating. Detected 1101 patterns are gated through U153 as 40-nanosecond delayed data, while detected 1101 patterns are gated through U153 as 20-nanosecond delayed data. Normal, delayed, and advanced data appearing at U153-3, U153-8, and U153-6, respectively, are combined at U146-8 to provide the final WRITE DATA output.

U143-3 is used to disable the normal signal in passing to U153 when either a delayed or an advanced signal is to be passed through to U146. U121-9 and U131-9 (for detected 1101 events), and U131-5 and U121-5 (for detected 1011 events) are clocked by respective phases of the 40-nanosecond delayed data to set up for subsequent enabling of new delayed or advanced signals.

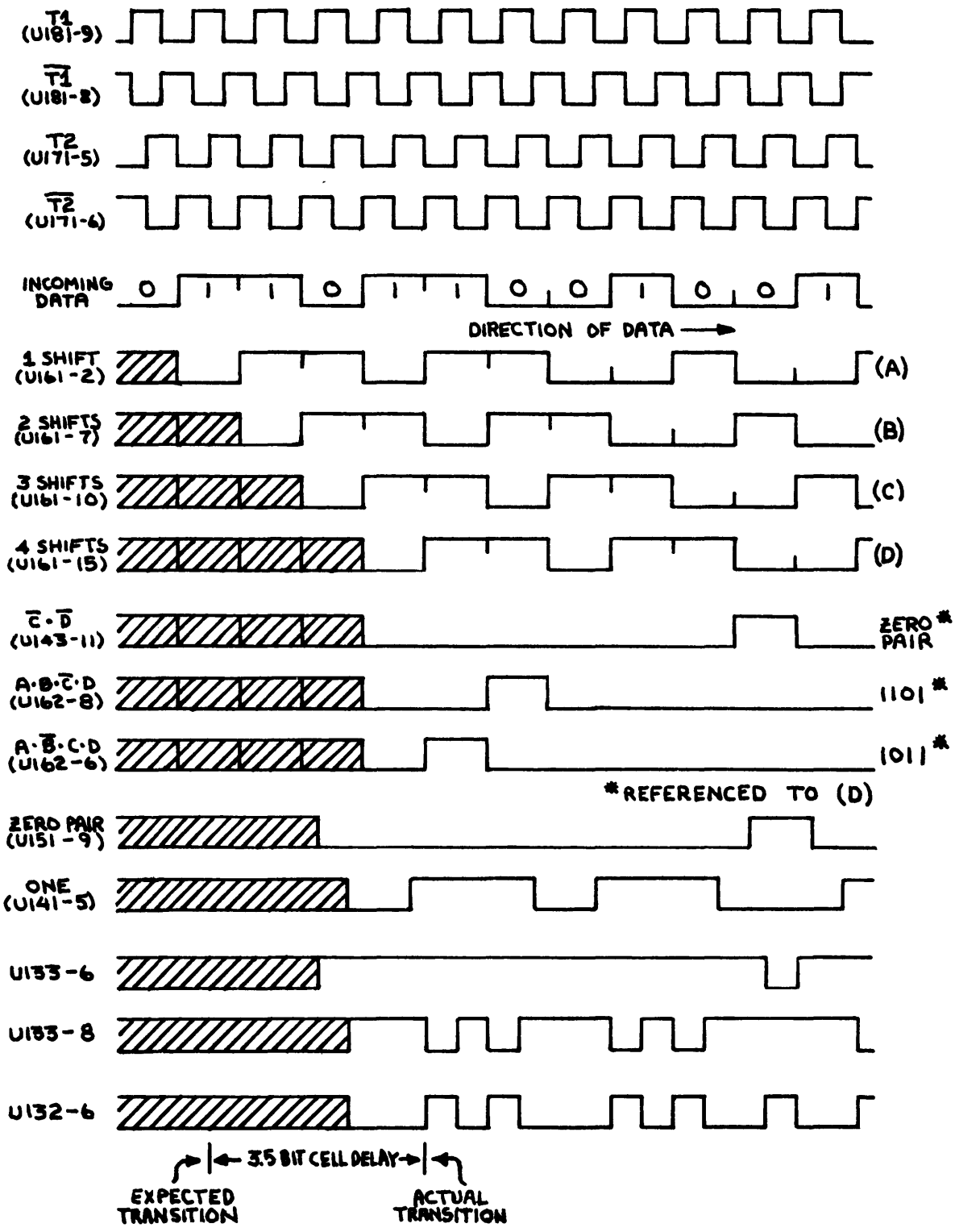
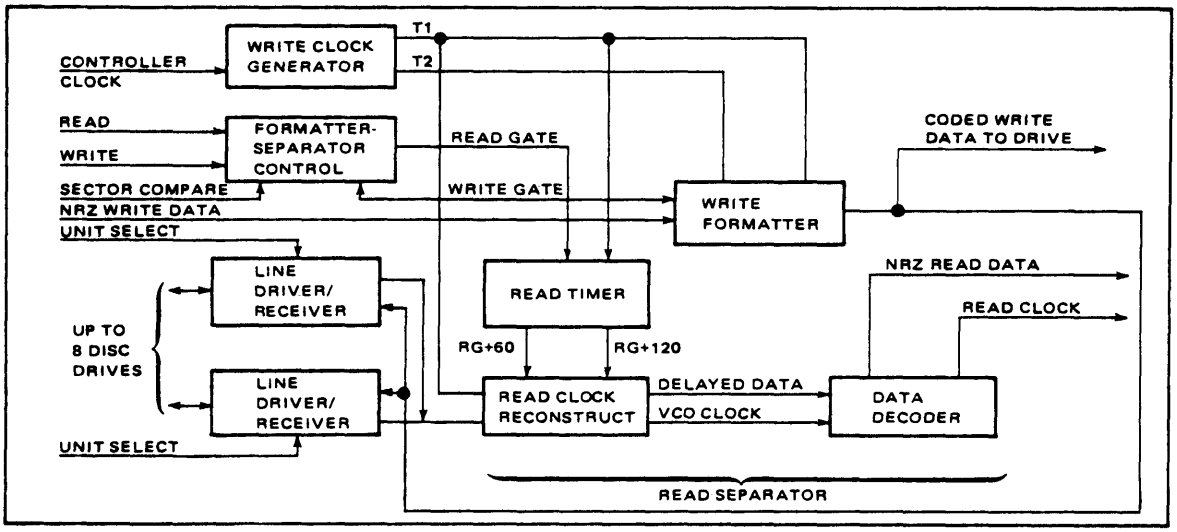

T1 (U181-9)
T1 (U181-8)
T2 (U171-5)
T2 (U171-4)
INCOMING DATA
0 1 1 1 0 1 1 1 0 0 1 1 0 0 1
DIRECTION OF DATA
1 SHIFT (U161-2)
(A)
2 SHIFTS (U161-7)
(B)
3 SHIFTS (U161-10)
(C)
4 SHIFTS (U161-15)
(D)
C·D (U143-11)
ZERO PAIR*
A·B·C·D (U162-8)
1101*
A·B·C·D (U162-6)
1011*
*REFERENCED TO (D)
ZERO PAIR (U151-9)
ONE (U141-5)
U133-6
U133-8
U132-6
3.5 BIT CELL DELAY
EXPECTED TRANSITION
ACTUAL TRANSITION

Figure 2

2.3 DATA SEPARATOR

The data separator employs both analog and digital hardware to allow the device to successfully separate data and clock signals from an incoming data stream whose rate is slightly varying. Shown below is the separator circuitry in relationship to the formatter/ separator section of the device controller.



2.3.1 SEPARATOR CONTROL AND CLOCK SELECT LOGIC

Prior to a true READ GATE (U189-11), U144-15 is held reset and U144-14 causes AND-OR output U174-6 to gate $\overline{T1}$ (U181-8) onto the DATA line of the PLL. At the same time U144-15 holds U145 reset, causing the SELECTED CLOCK line (U174-8) to carry the divided VCO output of U155-5. In this way, for non-READ operations, the PLL is held at the system storage rate of exactly 7.5 MHz.

With $\overline{\text{SECTOR COMPARE}}$ and READ both true, U189-11 provides a valid READ GATE signal, enabling U144-15 and gating T1 (U181-9) through U189-8 to be counted by U154 and U134. Note that U144-15 continues to hold U145 reset, so that the PLL will continue to lock onto the 7.5 MHz system clock until U144-15 goes high, as described below.

U154 and U134 are connected as divide-by-60 (at U134-11) and divide-by-120 (at U134-12) counters. Sixty pulses of T1 after the READ GATE goes high, U134-11 clocks U144-15 into a high state (U144-14 conversely going low); U164 and U174 consequently gate 70-nanosecond delayed data (from delay line U152) onto the DATA line (during the second 60 pulses of T1, the PLL locks up on the zero sync field read from the disc).

One hundred and twenty pulses of T1 after the READ GATE goes high, U134-12 clocks U145-11 high (U145-10 goes low), disabling counters U154 and U134 and enabling the next positive transition of the nominally 7.5 MHz VCO output (U112-5) to clock a high state through to U145-15. At this point, the clock select circuit of U175 is enabled, and U174 consequently gates U175-9 (the clock select circuit output) onto the SELECTED CLOCK line (U174-8). At this point T1 is disabled (U181-13 goes low), as it was not needed since the 60-bit count (when the DATA line was switched from T1 to 70-nanosecond delayed data). From now until $\overline{\text{SECTOR COMPARE}}$ is lost, the PLL tries to lock the VCO output onto the clock select output (which is generated by the incoming data as described below.)

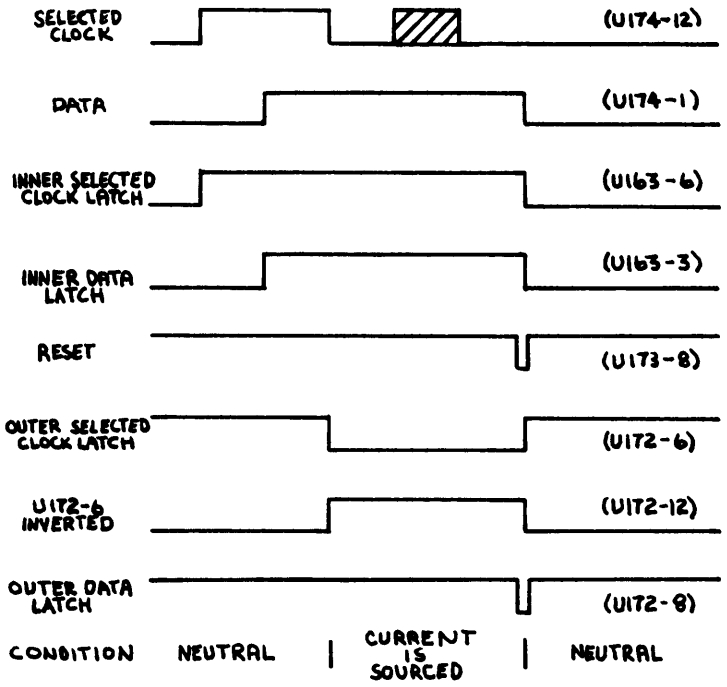
Data coming from the disc drive is generated by a bi-directional one-shot having an output pulse duration of 58 nanoseconds (nominal). After 120 pulses of T1, the clock select circuit (U175) receives the incoming data (undelayed) and generates from it a VCO dependent wavetrain coincident with the delayed incoming data. Both the delayed data and the generated wavetrain are fed to the PLL phase comparator (via the DATA line and the SELECTED CLOCK line, respectively) for use in matching the VCO frequency to that of the incoming data (this process will become evident later). Figure 3 shows the relationship between the VCO, incoming data, and clock select circuit pulsetrains.

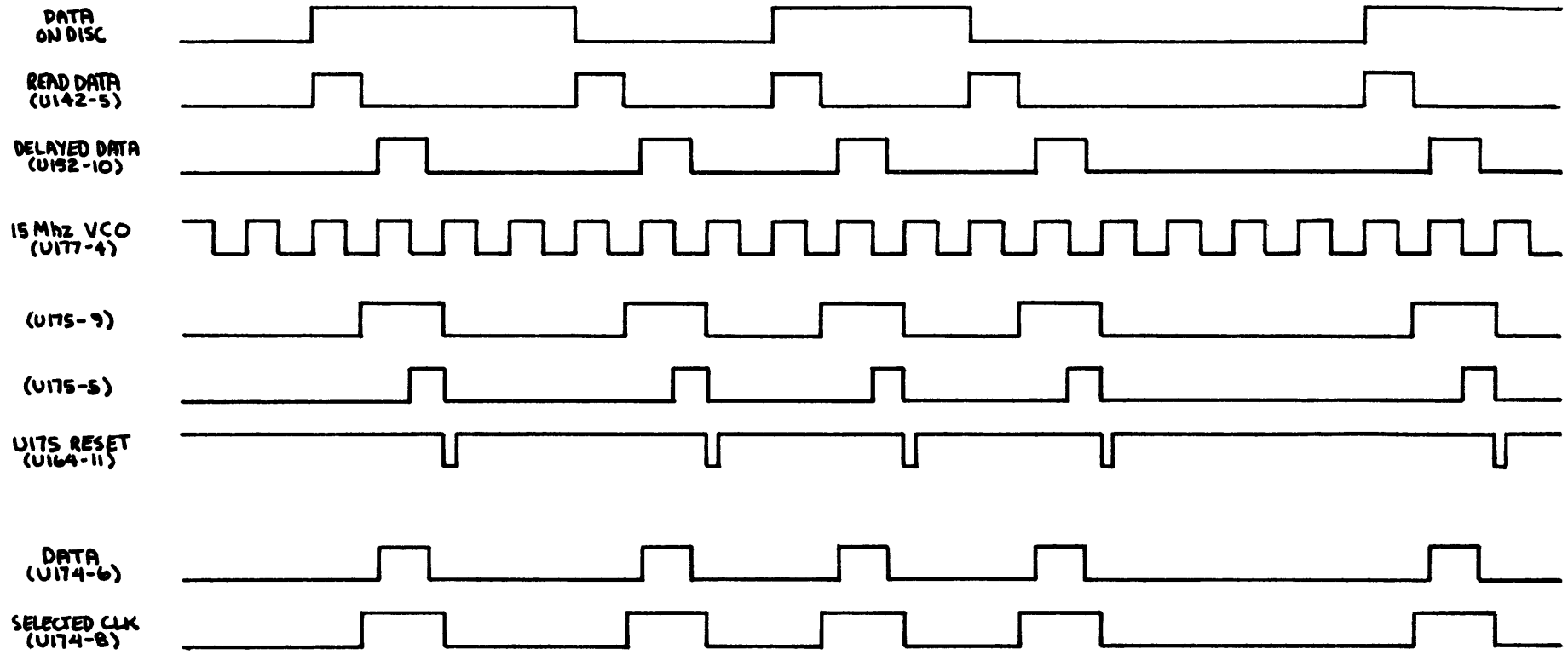
2.3.2 PHASE COMPARATOR AND VCO

Phase comparator logic (composed of U163, U172, U173, and U174) is redrawn in figure 4 to make circuit operation more apparent. U163 forms two inner latches, while U172 and U174 form two outer latches around those of U163; U173 provides a reset function for all latches (more of this will be described shortly). CR2 and CR3 make certain that current is sourced, sunk, or neither, depending on the conditions of U172-12 and U172-8 (see figure 4 insert).

When the SELECTED CLOCK provides a positive transition at U174-12, the upper inner latch (U163-6-8) becomes set; a subsequent negative transition will set the outer latch (U172-6 and U174-11). Further transitions of the SELECTED CLOCK line will produce no change in the state of either of these latches.

An analagous situation applies to DATA line latches. Note that transitions in either control lines (DATA or SELECTED CLOCK) effect only their corresponding logic. However, when all latches are set (i.e., both DATA and SELECTED CLOCK lines have encountered positive-going followed by negative-going transitions), U173 will go low, resetting all four latches to their original states. Thus the phase comparator will either source or sink current (depending on which control line received the first negative transition) between only the trailing edges of the DATA and SELECTED CLOCK signals. The timing diagram of figure 4 illustrates the various cases encountered during proper separator operation. Below is shown internal timing of the phase comparator for a specific case.





CLOCK SELECT CIRCUIT
WAVETRAINS

FIGURE 3

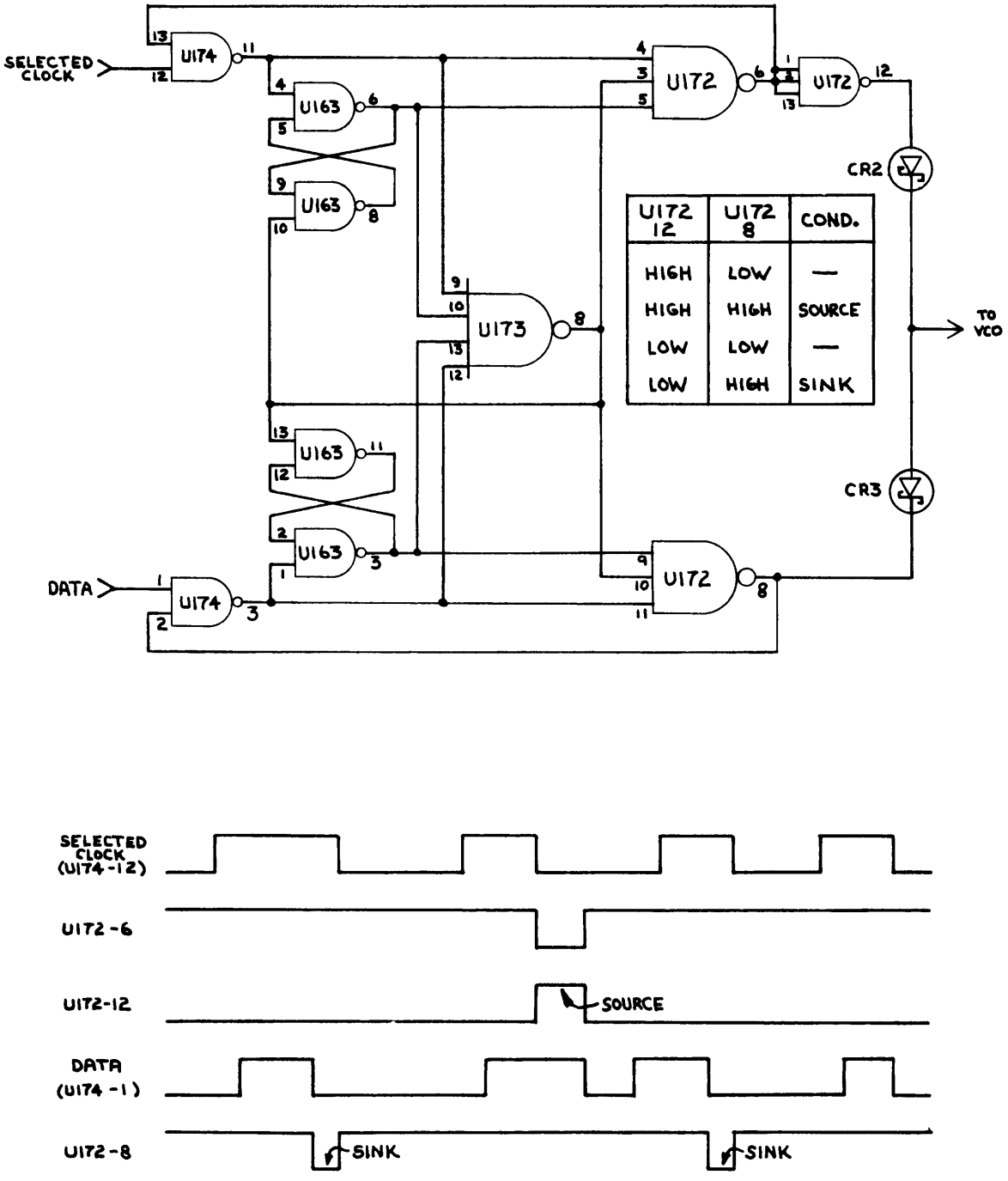


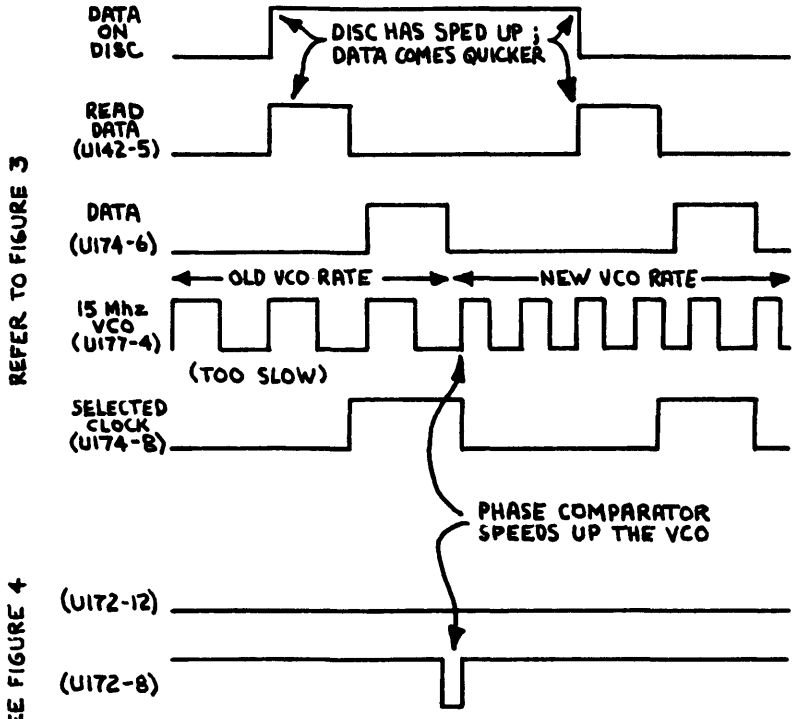
Figure 4. Phase Comparator Logic and Timing

Figure 5 shows the VCO circuit and a related block diagram. The phase comparator feeds an integrating amplifier (via the low pass filter); because the current sourced or sunk will remain relatively constant with time, the integrator is needed to convert the time that the current is sourced or sunk to a corresponding increase or decrease in voltage at the integrator's output (as described below).

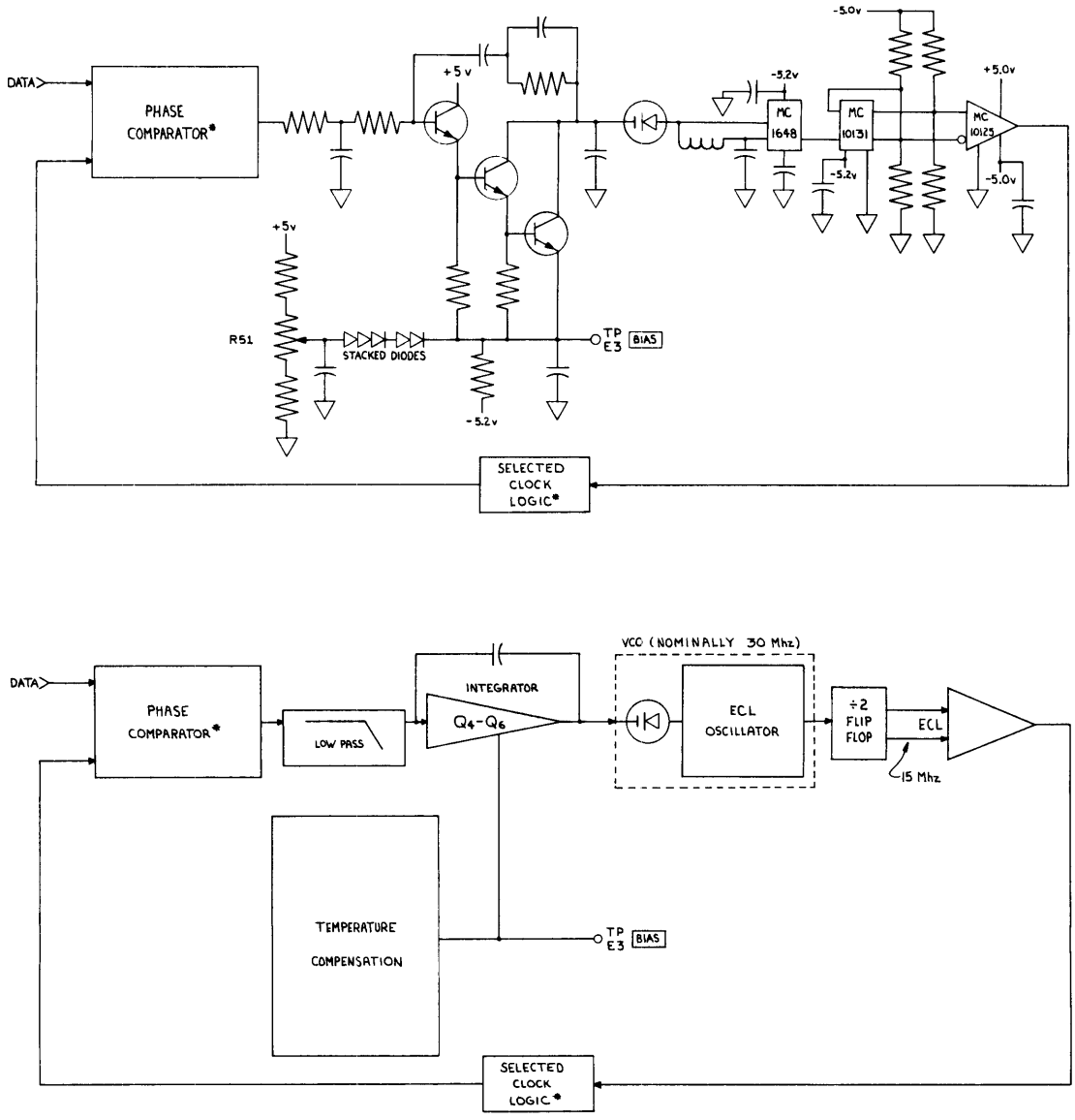
When the phase comparator sources current, C42 will change in an effort to maintain a relatively constant voltage at the base of Q4 (i.e., three base-emitter potentials above the a.c. ground of test point E3). As a result the capacitor potential will increase, causing the voltage at the collector of Darlington pair Q5 and Q6 to fall (similarly, sinking of current by the phase comparator will cause an increase in voltage at the output of the integrator by discharging C42 and thereby reducing the potential across it).

The cathode of the varicap remains basically fixed; therefore when the voltage output of the integrator falls, the reverse bias across the varicap will decrease. A smaller reverse bias will increase the capacitance associated with the varicap and, because it is in the tuned LC section of the 30 MHz ECL oscillator, will cause the VCO rate to slow down (a similar analysis will show that a rising integrator output will increase the reverse bias of the varicap, decreasing its associated capacitance and speeding up the VCO rate). Hence, the phase comparator can slow down the VCO by sourcing current (or speed it up by sinking current).

By speeding up or slowing down the VCO, the phase comparator can match the trailing edges of the DATA and SELECTED CLOCK lines, thus synchronizing the incoming data rate and the separator clock. Recall that the clock select circuit generates a falling edge that is time dependent on the VCO (refer to figure 3). Appropriately speeding up or slowing down the VCO will cause the trailing edge of the SELECTED CLOCK line (currently gating the output of the clock select circuit) to move in the direction of that of the DATA line (currently gating delayed data), as shown for various cases in figure 4. Illustrated below is a more complete timing diagram relating the clock select logic, phase comparator, and VCO for the cases of disc speed-up and slow-down.

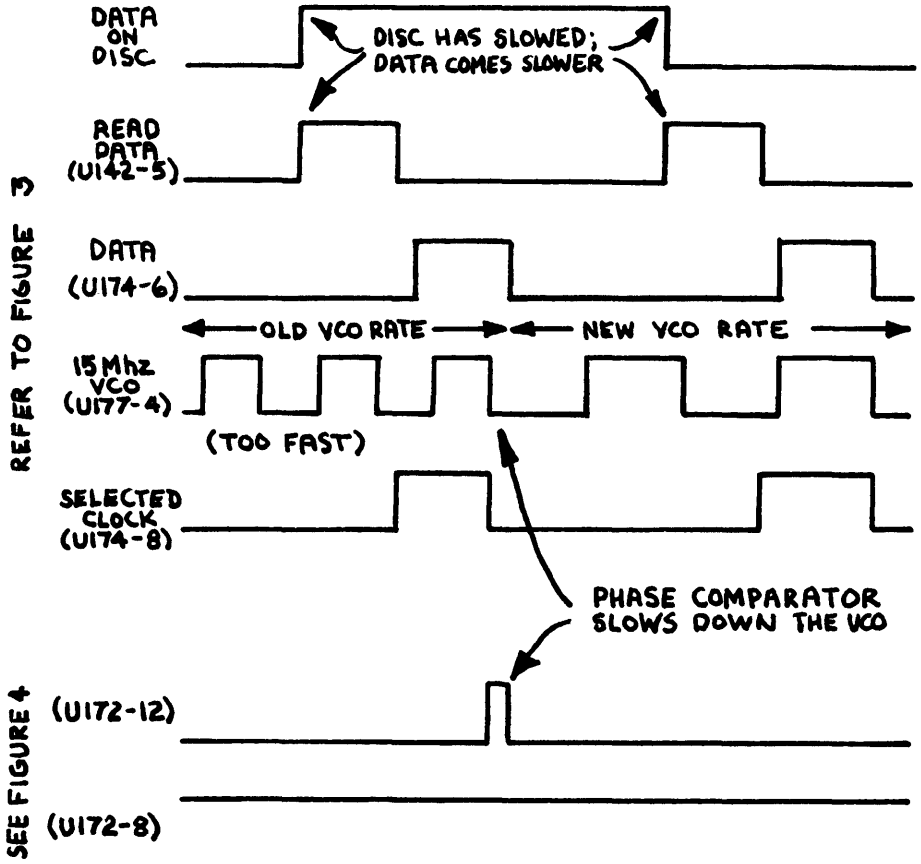


DISC SPEEDUP



* SEE PREVIOUS SECTIONS

Figure 5



DISC SLOWDOWN

A final point of interest concerning the VCO is the temperature compensation circuitry. The stacked diodes (CR5 and CR6) correct for potential differences across the transistors' base-emitter junctions due to variations in temperature. Initial adjustment is made at power on; R51 is adjusted until test point E3 is at zero potential. The phase comparator now neither sources or sinks current for constant VCO frequencies. The diodes will subsequently track with the transistors to maintain this condition throughout the specified operating temperature range of the controller.

2.3.3 FINAL DECODING LOGIC

U155-5 divides the nominally 15 MHz VCO output by two, returning a nominally 7.5 MHz VCO dependent square wave to the remaining decoder logic and to the PLL control logic. During the 60th to 120th count of T1, U155-5 is in the feedback loop of the PLL and subsequently becomes locked onto the zero sync field. U155-9 toggles 90° out of phase of U155-5 providing a "one's window" for subsequent decoding of "one's." The "one's window" at U155-9 has a duty cycle of slightly greater than 50% because advanced and retarded clocks to U155-13 are steered by U155-5 through U188. U156-5 will go high whenever the delayed data goes low during a "one's window," thus indicating a detected "one"; U157-6 will subsequently go low, latching this detected "one" into U166-5 for final outputting. With U157-6 low (U165-4 high) and U166-5 now high (U156-6 went high at the first detection of the "one"), U146-6 goes low resetting U156-5. The next trailing edge of the "one's window" will either provide clocking of another "one" into U166-5 or cause it to return to zero (depending on whether the subsequent circuitry detects a "one" or "zero" as the next bit). Final output of the decoded data occurs at U141-9; data at buffer U166-6 is clocked out through U141-9 via U155-5 (recall that U155-5 is the nominally 7.5 MHz VCO dependent output that became locked onto the zero sync

field; because transitions at "zero" bit cells occur at bit cell boundaries, it is this output that is used for final clocking of the decoded data from the separator).

U156-9 latches onto the first detected "one" after the sync field; this "one" by convention proceeds all sector information and data, as it provides the decoding logic with a way of syncing onto the relevant data that follows the introductory zero sync field. With U156-9 high, U157-3 gates the nominally 7.5 MHz VCO dependent output of U155-5 through U157-8 to provide the data clock for subsequent circuitry utilizing the decoded data.

Note that U155-9 and U166-5 are enabled by U144-15 after 60 counts of T1; after 120 bits, U156-9 is enabled, and U157-11 is gated to pass U166-6 as READ NRZ DATA.

Figure 6 provides overall timing for the final decoding logic.

2.4 SERDES, EOW, AND $\overline{\text{SYNC}}$

U98 and U128 form a 16-bit parallel load serial shift register for use by the SERDES hardware. U108, U118, and U138 form the SERDES parallel output buffer (SPOBF) while U97, U107, U117, and U127 form the parallel input buffer (SPIBF).

Serial data enters SERDES via U98-1-2; with each subsequent cycle of the DATA CLOCK (from the separator), $\overline{\text{DCLK 2}}$ will shift this data through the SERDES hardware. After 16 counts, U42 signals an EOW (end of word) and, after being delayed two bits by U52, causes U31-6 to generate a $\overline{\text{LOAD SPIBF}}$ signal that latches this 16-bit word onto the MIO bus via U97, U107, U117, and U127 (note that the SPIBF must first be enabled with an $\overline{\text{ENABLE SPIBF}}$ signal at pins 1 and 2 of each SPIBF latch). U52 incorporates the indicated two bit delay to compensate for the two bit delay of the separator hardware upon decoding read data.

Converse to the above case requiring incoming serial data from the disc to be converted to parallel data for use by the controller and CPU, parallel data to be written onto the disc must be serialized before being sent to the formatter. For this case U41-11 generates a $\overline{\text{LOAD}}$ signal at each EOW, causing the shift registers to load the current SPOBF contents (note that the SPOBF is updated by $\overline{\text{LBOUT1}}$; during clock phase T4 of appropriate lower byte instructions, the SPOBF is loaded with the current MIO bus contents). The formatter data clock (T2 now gated onto $\overline{\text{DCLK2}}$) continues to clock SERDES, with the serial data passing from U128-11 to MUX U51 (which selects from write data, ECC data, and CRCC data, depending on which requires writing onto the disc).

U51 selects appropriate data to be sent to the disc drive by monitoring the ENABLE CRCC SHIFT line. When the appropriate logic sends this line true, U51 deselects SERDES data and selects CRCC data; at the following $\overline{\text{SYNC}}$ signal U62-5 goes high, causing U51 to select serial ECC data from the ECC/ROM PCA. Note that SERIAL DATA OUT (U51-7) is sent to the formatter for encoding before being sent to the disc for subsequent writing.

The EOW latch (U72-3-11) is set either on sector overrun (generated by U62-9 when $\overline{\text{SECTOR COMPARE}}$ is lost) or when a $\overline{\text{SYNC}}$ pulse is encountered (refer to later paragraphs concerning the generation of this pulse). Resetting of the EOW flag is provided whenever an $\overline{\text{ENABLE SPOBF}}$ or $\overline{\text{ENABLE SPIBF}}$ signal becomes true; U148-11 will subsequently go low to reset the EOW latch (formed by U72-3-11). Figure 7 shows a simplified schematic representation of the EOW flag hardware, as well as the appropriate timing diagram.

$\overline{\text{SYNC}}$ hardware consists of U31, U41, U44, and U148. EOW pulses from U42-15 (on WRITE instructions), or once delayed EOW pulses from U52-5 (on READ commands), combine with the DATA CLOCK to provide the $\overline{\text{SYNC}}$ signal (U31-8). The delayed $\overline{\text{SYNC}}$ signal for READ operations is necessitated by the one bit delay of read data in the separator clock select

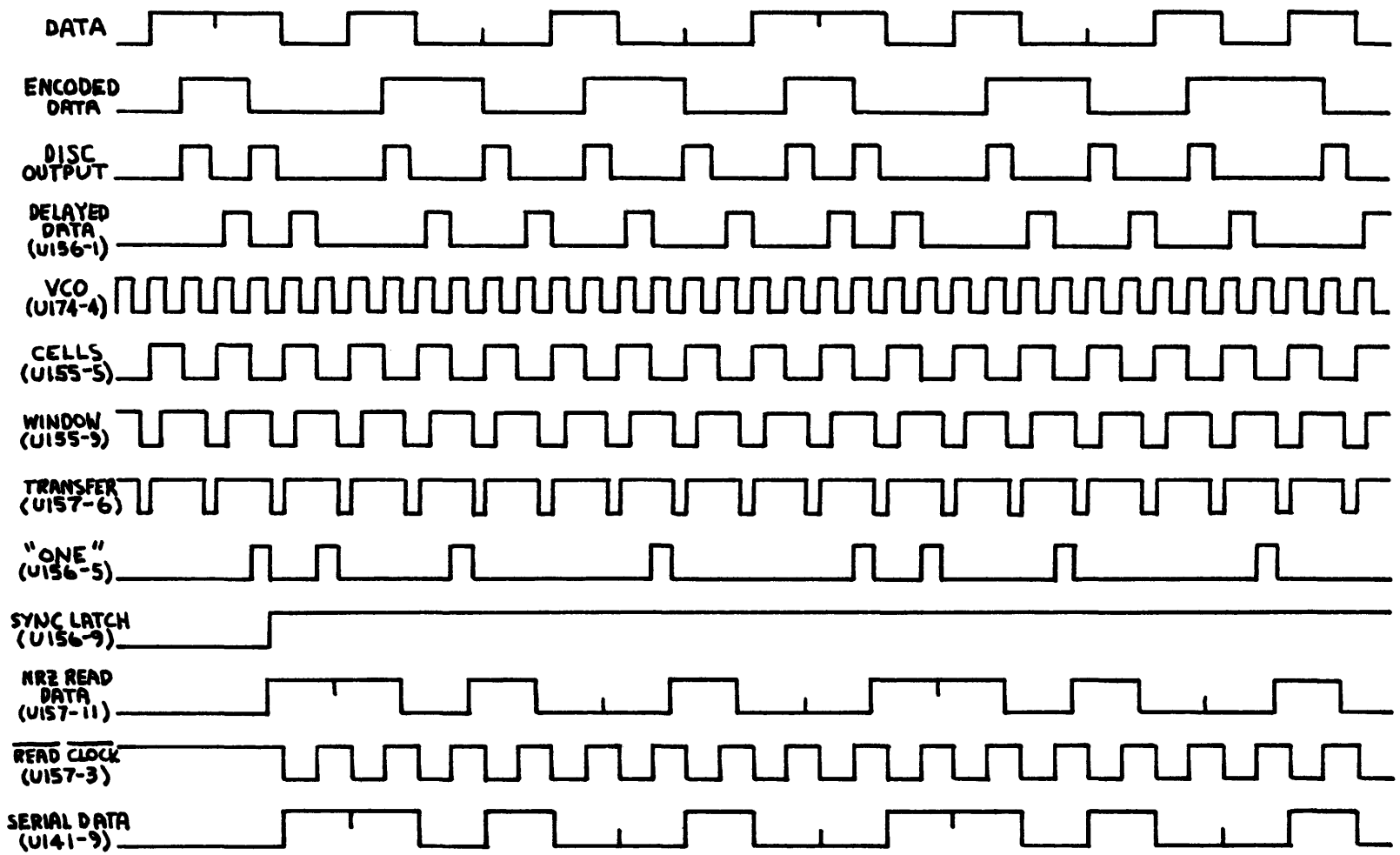


Figure 6. Decoder Logic Timing

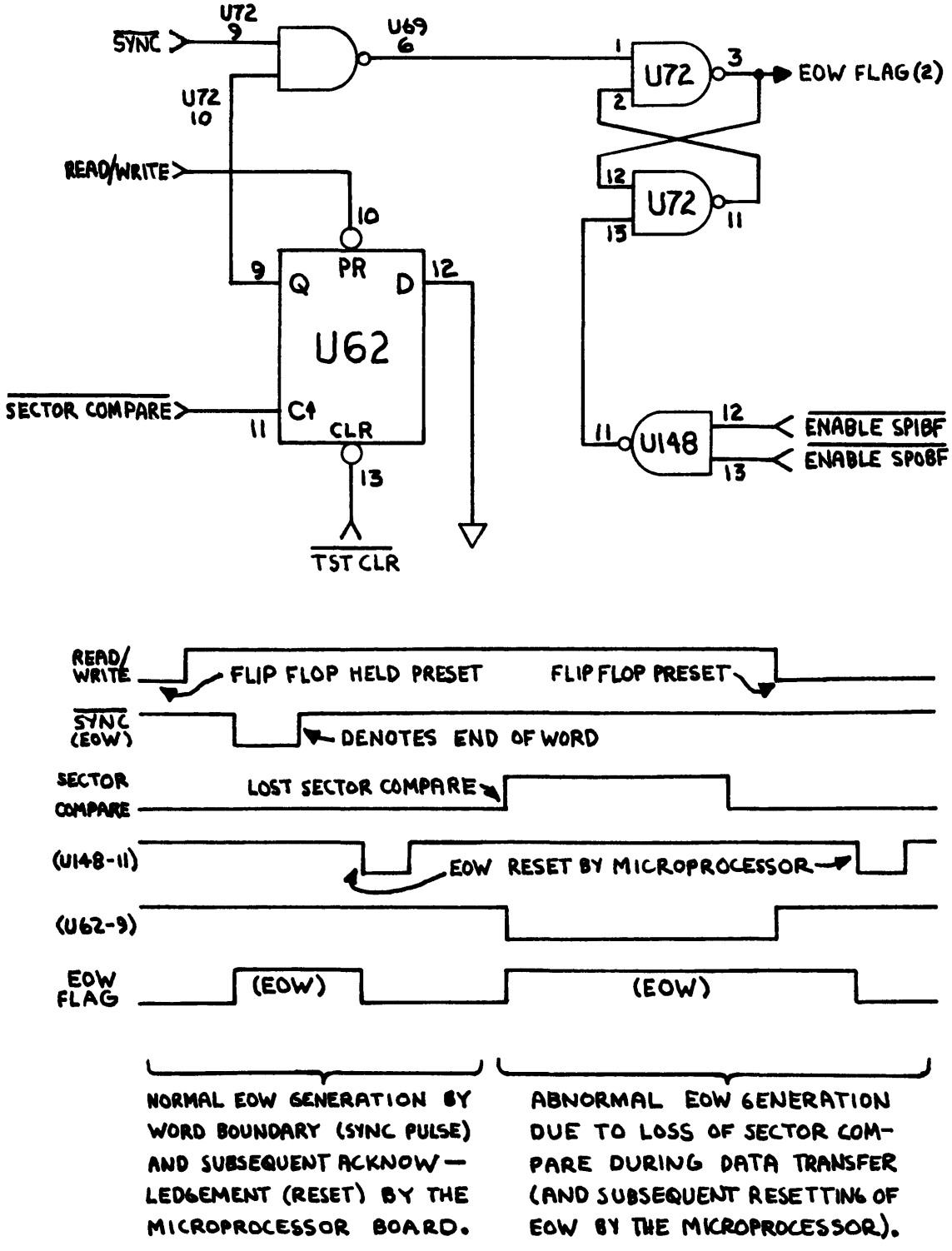


Figure 7. EOW Flag Circuit

circuit (see Section 2.3.1). (Because the $\overline{\text{SYNC}}$ pulse is incorporated into ECC timing considerations, it might prove useful to refer to Section 2.4.2 of the ECC description for further information.)

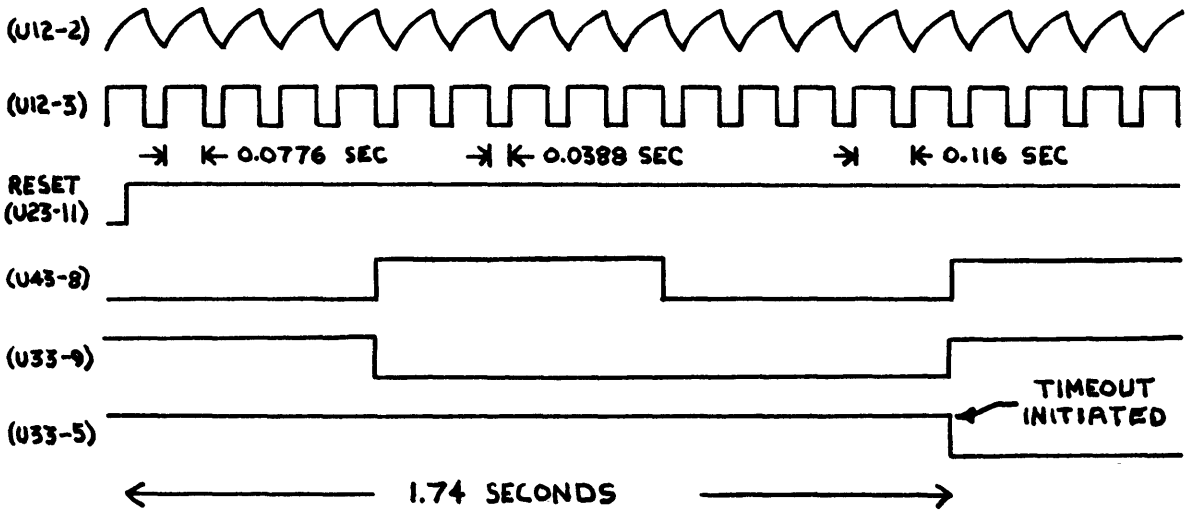
2.5 CRCC

The CRCC (cyclic redundancy code check) hardware is connected in a standard 16-bit CRCC configuration; U73-6-8-3 provide the various feedback paths around shift registers U54 and U74 to carry out the CRCC operation. U53 and U64 test the 16-bit CRCC generated polynomial for non-zero bits. If any are detected, U63-8 will go high indicating a CRCC error (the flag is tested at the appropriate time to indicate the existence of a data error).

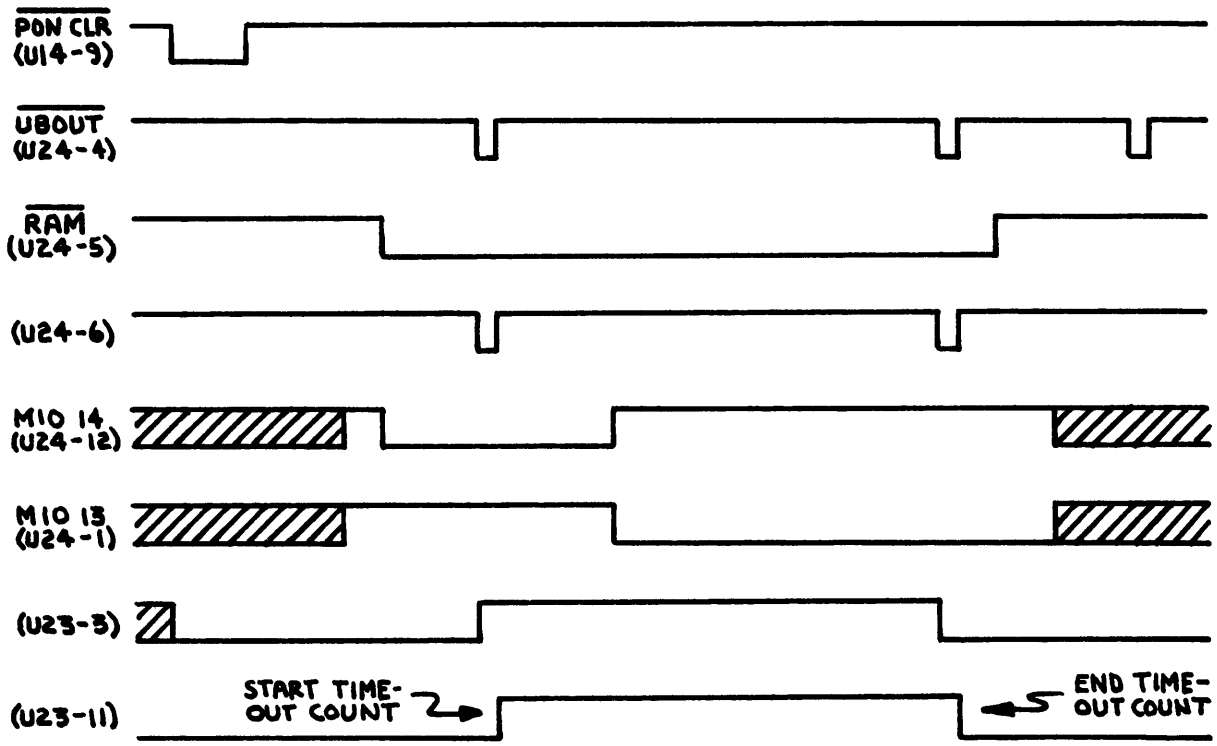
U39-6, U61-6, and U44-8 determine the source of data for CRCC processing. During a WRITE operation, serial data output from U51-7 is fed into the CRCC; otherwise serial data entering SERDES is concurrently gated into the CRCC hardware via U61.

2.6 TIMEOUT CIRCUITRY

U12 is a type 555 I.C. timer configured as an astable multi-vibrator with a period of 0.116 second (nominal) as shown below. The timer is deliberately operated at a rate greater than needed to generate the appropriate timeout period because the 555 is inherently more stable at higher frequencies (owing primarily to leakage currents in C3); as such, a divide circuit is needed to lengthen the 0.116-second period of the 555 to the desired 1.8-second (nominal) timeout period. U43 and U33 perform this dividing function.



Timeouts are initiated and reset by the gated latch formed by U14, U23, and U24. U23-3-6 form the basic latch, with U14-11-8 providing proper gating to disable timeouts during power-on clears or as a function of P2-4. U24-6-3-11 provide gating of MIO lines during appropriate intervals (i.e., during T4 of an upper byte instruction) to initiate or conclude the timing sequence. U23-11 provides the final gating of the reset/count signal to the dividing network. Below is illustrated the timing diagram for the timeout reset.



Note that U14-6 (with associated logic) will generate a true $\overline{\text{START}}$ signal whenever a timeout occurs; this signal is used by other hardware as will be described later.

2.7 RAM

The 7489 RAM (U159) functions as a scratchpad memory for the controller. In it are stored the data shown below.

BIT 3	2	1	0	WORD NO.	
X	I	I	I	15	CPU INTERFACE LAST POLLED FOR PENDING COMMAND
X	I	I	I	14	CPU INTERFACE CURRENTLY CONNECTED TO CONTROLLER
C	C	C	C	13	SECTOR COUNTER USED BY MICROPROGRAM
DRV		TYP		12	DISC DRIVE TYPE WORD
P	F	X	X	11	P=PLATTER PROTECT (READ ONLY) F=FORMAT OVERRIDE
DRV		ATN		8	PREVIOUS ATTENTION
I	I	I	H	7	CPU INTERFACE AND HOLD BIT FOR DISC DRIVES 0-7
				.	I=INTERFACE TO WHICH ASSOCIATED DRIVE (WORD NUMBER) WAS LAST CONNECTED
				.	H=SET INDICATES DISC DRIVE IS RESERVED FOR A SERIES OF OPERATIONS BY ASSOCIATED INTERFACE WORD NUMBER. NO OTHER CPU INTERFACE MAY ACCESS IT.
I	I	I	H	1	
I	I	I	H	0	NOTE THAT ONLY 8 DRIVES ARE MAPPED INTO RAM

U159 is addressed by the current contents of U158; MIO bus data (lines 0 through 3) is latched into U158 during LBOUT of a low RAMAD (RAM address) signal at U168-4 (thus 168-6 will latch MIO bus data into U158 during clock phase T4 of a proper microcode instruction). Data is written into the addressed memory only when RAM is low (thus enabling the memory enable of the RAM at U159-2) and LBOUT becomes true (thus during T4 of a lower byte instruction LBOUT goes low causing U159-3, the write enable of the RAM, to write the four lower MIO bits into the selected memory location). Note that although the write enable is set true during every lower byte instruction, data will not be written into RAM unless the memory enable is also true. Consequently data is read out of the RAM whenever U159-2 is low, but it is not gated onto the MIO bus unless U149 is enabled at U149-2-4-10-12 by U167-3 (this occurs only when the RAM has its memory enable pin true and the instuction decoding of the microprocessor PCA sets the INPUT line high).

2.8 FUNCTION DECODER

XADDR0-4 of the microprocessor PCA (available at P2-17-26-6-15-10) and the EXT SEL (P2-32) cause U59 to select one of fourteen (two being not currently assigned) internal functions of the device controller. Depending on the function selected, a particular gate of U48, U29, or U49 will be enabled to pass the appropriate control signal to the desired hardware. Described below are the various hardware implementations of these internal functions (note that the RAM, RAMAD, SPIBF ENABLE, and SPOBF ENABLE lines are generated by U59, but the corresponding hardware have already been described).

2.8.1 CONTROL BUS HARDWARE

Depending on whether CBUS information is going into or coming out of the controller, U59-5 (CBUS IN) or U59-3 (CBUS OUT) will be low. With U59-5 low, 8T26's U96, U106, U116, and U126 will be enabled in a receiver mode and consequently gate CBUS data onto the MIO bus (note that CBUS8 preceding these inverting bus drivers represents SECTOR COMPARE for other hardware logic).

Outgoing CBUS data must first be latched into U58, U68, and U78 (8T26's U96, U106, U116, and U126 are enabled as CBUS drivers by an appropriate TBUS command); with U59-3 low, U49-6 allows LBOUT to clock MIO data into these latches for subsequent loading onto the CBUS.

2.8.2 INTERFACE BUS HARDWARE

U59-4 being low enables the latching of MIO bus data into U57, U67, and U77 (this data is driven onto the MIO bus when 8T26's U56, U66, U76, and U86 are enabled in a driver configuration by interface function bus hardware). This operation will succeed only when INPUT (P2-8) is low (enabling U48-3); LBOUT passes through U48-6 (enabled by U59-4 being low) and performs the actual latching of data.

Note that U168-8 is subsequently enabled when U59-3 goes low; however INPUT (P2-8) must be high to allow U168-8 to enable 8T26's U56, U66, U76, and U86 in a receiver configuration (thus gating IBUS information onto the MIO bus). In this way, the INPUT signal can be used to decode a single IBUS EN command into an input or output operation without requiring another output of U59.

Whenever U59-4 goes low U69-2 subsequently goes high, allowing clock phase T4 (P2-3) to latch a high state at U18-9; consequently U21-6 will send IFCLK (J1-31) low, validating the individual word transfer on the IBUS. IFCLK will remain true until clock phase T4 of the next

instruction (unless that instruction sets U59-3 low), because U69-2 will go low as U59-3 goes high, thus allowing U18-9 to clock in a low state (U21-6 subsequently goes high).

It is important to remember that 8T26's U56, U66, U76, and U86 must be enabled prior to latching MIO bus data into U57, U67, and U77, as the validation strobe ($\overline{\text{IFCLK}}$) is sent only at this time.

2.8.3 INTERFACE FUNCTION BUS HARDWARE

U59-6 controls both the interface function bus and the clock offset enable. When U59-6 goes low, U29-8 allows LBOUT to latch MIO data into U47. U17 and U21 are always enabled, sending this latched data out on the four bit interface function bus (IFN0-3) and the interface receiver ($\overline{\text{ENIR}}$) and interface driver ($\overline{\text{ENID}}$) enable control lines.

2.8.4 RETRY/INITIAL AND NEW TRACK FLAGS

U59-7 controls the retry-initial flag. When it is low, U29-6 passes $\overline{\text{LBOUT}}$ to allow clocking of MIO 0 data into U88-9. Similarly, U59-8 controls the new track flag; $\overline{\text{UBOUT}}$, when U59-8 is low, passes through U29-8, clocking MIO 15 data into U88-5. These flags appear at P2-22 and P2-26 respectively (representing flags 9 and 5).

2.8.5 TAG BUS HARDWARE

U59-5 will go low whenever tag bus data is to be updated. When this occurs, U49-8 passes $\overline{\text{LBOUT}}$ to latch MIO bits 0 to 3 into U27. U32 is always enabled, and consequently passes this data onto the tag bus.

Note that TBUS 3 (U27-10) will, when high, enable drivers U96, U106, U116, and U126 to pass latched MIO bus contents from U58, U68, and U78 onto the CBUS (refer back to section 2.8.1).

2.8.6 INTERNAL CONTROL WORD HARDWARE

The internal control word (ICW) generates the internal READ and WRITE commands, as well as CRCC functions, $\overline{\text{STROBE}}$ signals, etc.

When U59-10 goes low, U49-3 is gated to pass $\overline{\text{UBOUT}}$ to the ICW latches (U38 and U26-5). With a $\overline{\text{UBOUT}}$ pulse, MIO data is latched into U38 for ICW decoding, and U26 for the $\overline{\text{STROBE}}$ signal circuitry. U38 obtains the READ (MIO 8), WRITE (MIO 9), and READ/WRITE (MIO 10) signals directly. MIO bits 10 – 12 appear for processing by U16 (dual D-type flip-flop) and subsequent control of the CRCC hardware, as described below. Note that both U38 and U26-5 are cleared by a $\overline{\text{START}}$ pulse.

U16-5 and U16-9 decode certain ICW data to provide the INH CRCC CLK and EN CRCC SHIFT signals; the $\overline{\text{SYNC}}$ pulse will latch ICW data into U16-5-9 at the appropriate time during a READ or WRITE operation (by using the $\overline{\text{SYNC}}$ pulse as a clock, the circuitry can synchronize with the boundary of the last data word). Notice that a false READ/WRITE signal resets U16-5 (thus preventing any CRCC shifting). U16-9 reset and data functions are under the control of two distinct ICW bits (U38-7 and U38-5), while the data function of U16-5 is controlled by the same ICW bit as its reset (U38-10 and U38-12 both latch MIO 10 data).

$\overline{\text{STROBE}}$ hardware is controlled both by POWER ON and ICW signals (the former will be described in section 2.9). Each signal controls one of the two series transistors of U25; note that if any are "off," R39 and R40 will pull the $\overline{\text{STROBE}}$ signal to a high state (only when both are conducting will the $\overline{\text{STROBE}}$ line go true).

When the $\overline{\text{ICW CLK}}$ (U49-3) latches a "zero" (from MIO 13), U25-3 will invert it and cause its series transistor to conduct (normally the other transistor is already biased "on" by the POWER ON hardware); the $\overline{\text{STROBE}}$ line will go true unless a $\overline{\text{START}}$ pulse sets U26-5 to its normal high state (thus returning $\overline{\text{STROBE}}$ high).

2.8.7 FILE MASK AND EOC HARDWARE

The file mask and EOC (end of cylinder) flag are both selected when U59-13 goes low. A lower byte instruction will cause U29-3 to clock MIO 8 data onto U18-5 to generate the appropriate EOC flag; an upper byte instruction causes U29-11 to clock MIO bits 0, 1, 2, and 3 into U37-5, U37-9, and U26-9, respectively, thus generating the AUTSK (auto seek) flag, CYSRF (cylinder/surface) flag, SPREN (sparing enabled) flag, and seek operation's direction bit (notice that the latter is enabled onto MIO 14 only when an INPUT mode operation is in progress and the RAM is selected).

2.8.8 INTERFACE FUNCTION VALIDATION

Interface function bus commands are validated whenever U59-14 goes low. $\overline{\text{UBOUT}}$ is enabled through U48-11 to clock MIO 8 data into U36-5; this signal is subsequently inverted and driven to the interface by U21-11 (8T09 driver), which is always enabled. Note that this $\overline{\text{IFN VALID}}$ signal will remain in the current state until another instruction selects this hardware and clocks opposite data into U36-5.

2.9 POWER ON AND POWER FAIL CIRCUITRY

When controller power is applied, a POWER ON signal is sent to the controller via P1-9. Q2 will then conduct to drive the "power on" hardware and enable any subsequent $\overline{\text{STROBE}}$ signal.

Because the 13037B must be able to respond to the clear signal pulse train generated by 21XX CPU's, a digital low pass filter was incorporated in the clear circuitry. The falling edge of the clear signal at J1-2B causes U22-11 to go high. U22-4, 5 goes immediately high to cause U22-6 to generate a true $\overline{\text{PON CLR}}$ signal within the controller. When the clear signal returns high, U22-11 will return low; however, CR7 is now reverse biased, and its failure to conduct forces the RC time constant of R60 and C57. This cycle repeats throughout the clear pulse train, with a true $\overline{\text{PON CLR}}$ signal eventually winning out.

Note whenever POWER ON is true, Q1 is saturated and hence the POWER FAIL signal is false; if, however, POWER ON is lost causing the emitter of Q2 to go low, Q1 turns off to generate a true POWER FAIL signal (in effect J1-18, the POWER FAIL connection, acts as an open collector output that provides a CPU power fail signal).

2.10 DRIVE RECEIVERS AND TRANSMITTERS

Eight identical circuits are employed as interfaces between the disc and the controller. Each disc sends two differential signal lines and one select line to the device controller for subsequent processing. Figure 8 illustrates one of the eight transceiver circuits.

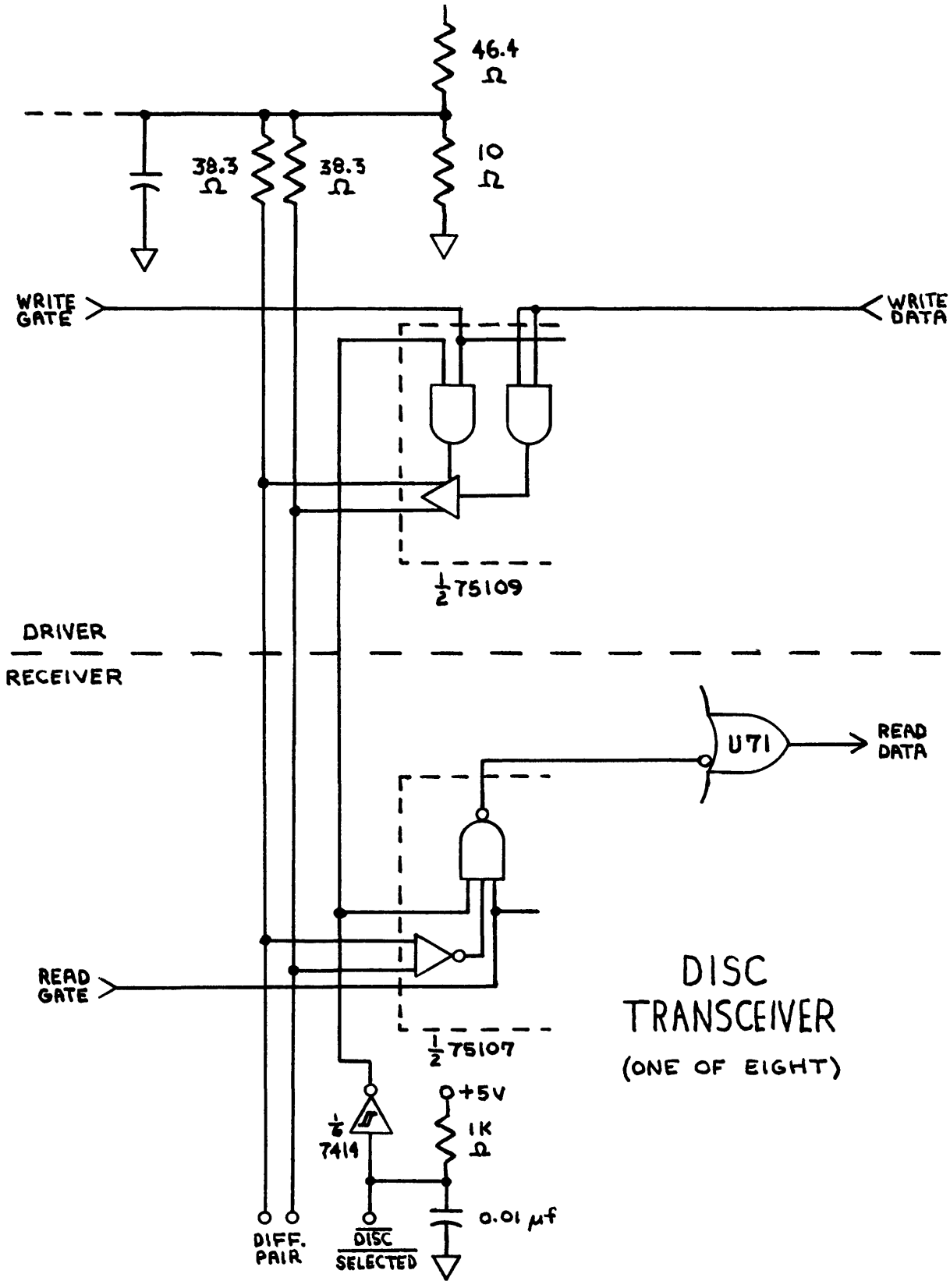

46.4 Ω
38.3 Ω
38.3 Ω
10 Ω
WRITE GATE
WRITE DATA
½ 75109
DRIVER
RECEIVER
U71
READ DATA
READ GATE
½ 75107
DISC TRANSCEIVER
(ONE OF EIGHT)
+5V
1K Ω
¼ 7414
0.01 μf
DIFF. PAIR
DISC SELECTED

Figure 8

The selected drive will send a $\overline{\text{DISC SELECTED}}$ signal to the appropriate transceiver hardware of the device controller. This signal, along with a READ GATE or WRITE GATE signal, will enable either the receiver (75107) or the driver (75109) circuit, respectively. The former will take data from the differential pair and pass it to U71; the latter will drive the differential pair with WRITE DATA. Note that because only one drive will be selected at any one time, there will be no conflict of READ DATA at U71.

2.11 FLAG BUFFER AND OVERRUN

All information between any device is sent ground true; the interface flags, therefore, need inverting and buffering for subsequent use by the controller. U19 provides both buffering and inversion of these flags, as well as the double buffering of the $\overline{\text{START}}$ signal (thus creating the $\overline{\text{CLEAR}}$ signal at P2-2).

Note that the incoming interface overrun flag (flag 7) is OR'ed with a controller-generated signal (at U35-6); during write operations the controller will generate an overrun error (independent of any overrun condition indicated by the interface flag) whenever a write is attempted without available data (unless, of course, an end-of-data condition is detected, whereupon the last word sent is continually written onto the remaining portion of the sector). U45 forms the controller overrun latch; it is enabled at U45-5 whenever the controller is in a write mode, and has as its input (set side) the output U35-11. This gate, in conjunction with U35-8, allows any $\overline{\text{IFCLK}}$ pulse (indicating a word transfer) to set the overrun latch unless U35-8 detects a DTRY (flag 1) or EOD (flag 6) condition (thus disabling the $\overline{\text{IFCLK}}$ pulse at U35-11). When the write mode is lost, the overrun latch is held reset until any subsequent write operation.

APPENDIX I

DISC DRIVE INTERFACE

CONTROLLER/DISC DRIVE INTERFACE

The Controller/Disc Interface will have the following groups of lines:

1. TAG BUS — Four lines specifying what function is to be performed.
2. CONTROL BUS — Sixteen bidirectional lines containing additional command information, drive conditions, etc.
3. COMMAND STROBE — Validates all Tag Bus functions.
4. FORMATTED DATA — A bidirectional line transmitting bit formatted data between the Controller and Disc Unit.

A schematic is shown in figure 4A-1.

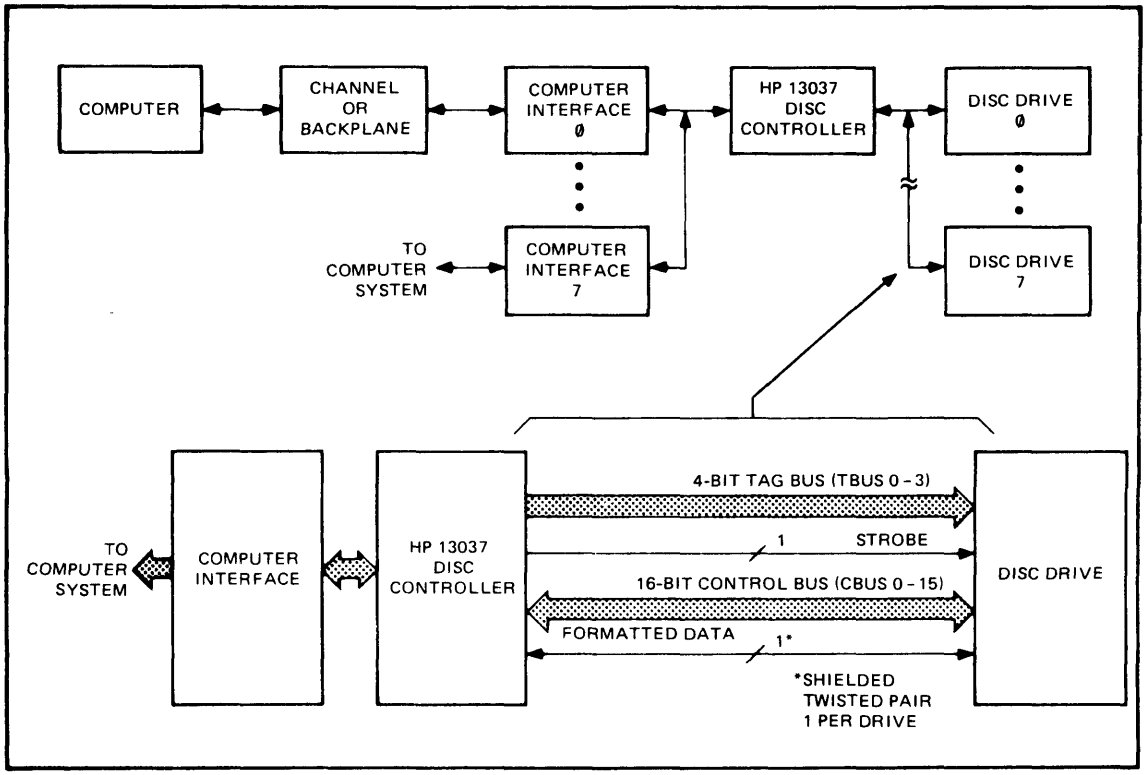


Figure 4A-1. Disc Drive Interface

TAG BUS FUNCTIONS

TAG BUS functions are summarized in table 4A-1.

The TAG BUS is a four-bit bus validated by command strobe, transmitting drive functions from the controller. All edge validations are by the leading edge of the strobe.

Table 4A-1. Tag Bus Functions Summary

TAG BUS					CONTROL BUS (Refer to Table A-2)	
CODE BIT				OPERATION		
3	2	1	0			
0	0	0	0	READ*	STATUS	INFORMATION FROM THE DISC DRIVE
0	0	0	1	WRITE*	STATUS	
0	0	1	0	REQUEST STATUS*	STATUS	
0	0	1	1	REQUEST ATTENTION	ATTENTION	
0	1	0	0	DISCONNECT		
0	1	0	1	CLEAR		
0	1	1	0	REQUEST SECTOR*		
0	1	1	1	NOT USED		
1	0	0	0	SEEK*	CYLINDER ADDRESS	INFORMATION FROM THE CONTROLLER
1	0	0	1	ADDRESS RECORD*	HEAD-SECTOR ADDRESS	
1	0	1	0	ADDRESS UNIT	UNIT ADDRESS	
1	0	1	1	RECALIBRATE*		
1	1	0	0	TRANSMIT SECTOR*	SECTOR ADDRESS	
1	1	0	1	OFFSET*	OFFSET	
1	1	1	0	CLEAR STATUS*	SELECT CLEAR	
1	1	1	1	NOT USED		

*Only selected units will respond.

Tag bus bit 3 determines whether the controller or the disc drive will place information on the control bus.

Units respond to commands only after being selected; the exceptions are Address Unit, Request Attention, Disconnect, and Clear.

READ

Select required. Drive gates status on the control bus. When this function is valid the disc drive waits for the leading edge of its internal sector compare signal, then transmits sector compare in the status word and bit-encoded data from the selected head on the formatted data lines.

WRITE

Select required. Drive gates status on the control bus. When this function is valid the disc drive waits for the leading edge of its internal sector compare signal, then transmits sector compare in the status word and accepts bit-encoded data for the selected head on the formatted data lines.

REQUEST STATUS

Select required. When this function is valid the drive gates the contents of its status register on the control bus. See table 4A-2 for status bit assignments.

REQUEST ATTENTION (REQUEST IDENTITY)

Select not required. When this function is valid the drive gates its attention bit on the line of the control bus corresponding to its unit number.

The Rotation Position Sensing (RPS) feature allows the drive to transmit this attention bit with a lookahead, requiring that the attention bit go true N sectors in advance (where N is any number between 0 and 15 inclusive). This delay is selectable on each disc drive by a strap. It should be noted that without RPS enabled, attention will remain true until disabled by the controller; with RPS, the attention is gated and remains true only during the time that the target sector (−N) passes underneath the heads.

DISCONNECT

Select not required. The disc drive responds to this function by clearing its select flip-flop. When this flip-flop is false the drive will not respond to select-required functions.

CLEAR

Select not required. The disc drive clears its attention bit, non-destructive read/write faults, plus any other appropriate bits (e.g., first status, sector address register).

REQUEST SECTOR

Select required. The disc drive transmits the contents of its "current address" counter and the head address register on the control bus.

Note: There are two current sector counters in the 7905 and 7906 drives; one is for the fixed disc and the other is for the removable disc (this is necessary as reloading a cartridge can cause sector skew between these discs).

SEEK

Select required. Control bus contains cylinder address. On the trailing edge of command strobe the drive clocks the control bus contents into its cylinder address register and initiates a seek to that address. Upon completion of the seek, the attention bit is set. If the address is illegal the drive sets seek check and attention.

ADDRESS RECORD

Select required. Control bus contains head-sector address. On the leading edge of the command strobe the drive clocks the head address field of the control bus into its head address register. On the trailing edge the sector address field is clocked from the control bus into the sector address register (note that an illegal address in either or both fields will not be latched; instead an attention and seek check will be generated by the trailing edge of the command strobe).

ADDRESS UNIT

Select not required. Control bus contains 3-bit unit number. Disc drive responds by setting its select flip-flop if the control bus contents match the disc drive address. If this bit is true it responds to all select-required commands.

RECALIBRATE

Select required. The disc drive positions its heads over cylinder 0 and clears its "current cylinder address" register.

TRANSMIT SECTOR

Select required. Control bus contains sector address. On the leading edge of command strobe, the drive clocks the sector address only into its sector address register. The head address register is not modified.

Note: This function was designed to permit flexibility in defective/alternate track operations by allowing the sector address to be changed without the head address being touched.

OFFSET

Select required. On the leading edge of command strobe, the drive clocks the control bus contents into its position offset register. The Drive Busy status bit goes true while the heads move to their offset position. See table 4A-2 for bit significance.

Note: Designed for marginal data recovery purposes, OFFSET allows 63 increments, in either direction, from the nominal track center carriage position. The physical amount for each increment depends on the characteristics of the particular drive and/or surface being used. The offset may be modified by another offset, or cancelled by a subsequent SEEK or RECALIBRATE function.

CLEAR STATUS

Select required. Control bus contains bits specifying which drive status to clear. The drive clears the appropriate status bits in response to this function. See table 4A-2 for CLEAR STATUS bit assignments.

CONTROL BUS FUNCTIONS

CONTROL BUS functions are summarized in table 4A-2.

The CONTROL BUS is a sixteen-bit bidirectional bus used to transmit control information and modifiers between the disc drive and the controller. Depending on the tag bus, the control bus contains one of the following:

ATTENTION

A line-per-drive response. Each drive sets its attention bit when it loads, unloads, completes a seek, faults, or sets seek check in response to an illegal cylinder address. The bit is cleared by a clear command or a clear status command with bit 0 on. When attention is put on the control bus, each disc unit drives only the bus line corresponding to its logical unit number.

Table 4A-2. Control Bus Functions Summary

BUS LINE	CLEAR STATUS	OFFSET	CYLINDER	HEAD-SECTOR	UNIT	STATUS	ATTENTION
0	Attention	1	1	Sector 1	1	Drive Busy	Unit 0
1	First Status	2	2	2	2	Drive Ready	1
2		4	4	4	4	Seek Check	2
3		8	8	8		First Status	3
4		16	16	16		Drive Fault	4
5		32	32	32		Format	5
6			64			Protected	6
7		Sign	128			Attention	7
8			256	Head 1		Sector Compare	
9			512	2		Drive Type 1	
10				4		Drive Type 2	
11				8		Drive Type 4	
12						Drive Type 8	
13							
14							
15							

UNIT

Valid unit numbers are 0 to 7.

CYLINDER

Valid cylinder numbers depend on drive type.

HEAD-SECTOR

Valid head and sector numbers depend on drive type.

OFFSET

Valid offset numbers are 0 to 63, positive or negative. Negative offsets are in sign-magnitude form. +0 = −0.

CLEAR STATUS

Bit 0 on specifies that the attention bit should be cleared; bit 1 on specifies that the first status bit be cleared.

STATUS

Contains the current drive status:

Drive Busy — True if the heads are not positioned and settled over a valid track.

Drive Ready — True if the heads are over the disc (and, for the 7906, the temperature compensation requirements have been satisfied).

Seek Check — Set if the controller transmits an invalid cylinder, head, or sector address, or if a seek is attempted while the drive is still executing a previous seek command. Cleared when a valid operation is performed to correct the error. Any attention bit can then be reset by the controller.

Note: The bounds checking is done by the disc drive.

First Status — Set when drive first loads the heads on the disc, i.e., by going from a "not ready" to a "ready" condition. Cleared by a clear status command with bit 1 set.

Note: This is designed to provide separate status for the controller for unexpected events.

Drive Fault — Set when the drive detects either a read/write or servo fault; neither can be caused by the controller under normal circumstances. Non-destructive read/write faults can be cleared by a clear command; servo faults and destructive read/write faults require operator intervention.

Format — Transmits the condition of the format switch located at the front of the drive. This switch may be set to the "format" position to allow track initialization, or the controller designer may use it for any other system design purpose.

Protected — Transmits the condition of the platter protect switch located on the front of the disc drive corresponding to the currently addressed head.

Attention — The condition of the attention bit.

Sector Compare — True while a read or write command is true following the coincidence of a leading edge of the drive's internal signal comparing the sector address register and the "current sector address" counter. Cleared when the command is removed or when the disc drive determines that it is not safe to continue the transfer because the sector has passed.

Drive Type — Four encoded bits which allow controller to determine number of heads and number of sectors per track.

COMMAND STROBE LINE

Normally the leading edge validates all functions on the tag bus. The function is valid only if this line is true. The trailing edge is used when the drive is validating the contents of the CBUS.

FORMATTED DATA LINES

A differential pair used to transmit serial bit formatted data to and from the disc drive. A separate pair is used for each disc drive. Each differential pair has a shield that becomes grounded when its respective drive is selected. This shield is used to enable its corresponding data port on the 13037.

DRIVERS/RECEIVERS

All lines are ground true. FORMATTED DATA uses differential pairs. Termination of all interface lines will be provided at the disc drive located physically farthest down the cable from the controller. All signals are transmitted on twisted pairs. With the exception of FORMATTED DATA, one side of each twisted pair is terminated to Logic Ground at the DISC UNIT and at the CONTROLLER.

SERIAL BIT ENCODED DATA

Coding Scheme — Delay modulation, self clocking with one transition per bit cell. A data pulse is written for each "1" data bit. The data pulse occurs in the middle of the bit cell.

A clock pulse is written only between two consecutive "0" data bits. This clock bit occurs at the cell boundary between the "0" data bits.

Write Clock Frequency — The Write Clock Frequency is 7.50 megahertz ±0.01%.

Bit Cell Time — 133.33 nanoseconds nominal.

Read Data Pulse Width — 50 nanoseconds nominal.

Sector Timing — The leading edge of any sector pulse relative to its nominal location shall not vary more than ±5 microseconds (this includes sector pulse circuitry; deviation between heads on the same disc will be less than 4 microseconds).

APPENDIX II

COMPUTER INTERFACE

SIGNAL LINES:

Clear

Hard clear on controller logic. May be generated by CPU power up/down, manual preset button, or programmed signal not otherwise interpreted by the controller. May be disabled on some interfaces. (This signal is not mandatory.)

Note: Single pulse hardware Clear signals must remain true for at least 500 μs; digital low-pass filtering of this signal within the 13037 will respond to pulse trains of sufficient duration with periods less than this 500 μs criterion.

Data Bus (IBUS 0-15)

Sixteen bit bus used to transmit commands, data, status, and addresses between the controller and interface in both directions.

ENID (Enable Interface Drivers)

Interface must be selected. Enables data bus drivers on interface.

ENIR (Enable Interface Receivers)

Enables data bus receivers on the interface.

Function Bus (IFN 0-3)

Four bit bus validated by IFVLD. Transmits interface functions from the controller.

IFCLK (Interface Clock)

Validates word transfers on the data bus while IFIN, IFGTC, IFOUT, or WRTIO function is valid. Trailing edge must be used. When IFOUT is true, controller reads data at the leading edge.

IFVLD (Interface Function Valid)

Validates function on the function bus. The function is valid only if this line is true. If an edge is used, it must be the trailing edge.

Flags from Interface

Flags are gated out by an interface whose select bit is set.

CMRDY (Command Ready)

True if a command is present in the command register. Cleared by IFGTC.

DTRDY (Data Ready)

True if data is present in the data buffer. Cleared when the data buffer is emptied.

EOD (End of Data)

True if the channel has completed a block transfer and the data buffer is empty. Not set during data chaining until the entire transfer is complete. Cleared when next command is transferred from the CPU to the interface. Note that while completing a sector transfer, the controller may continue to fetch from the data buffer even though EOD is set; therefore, the next command may not be preloaded into that data buffer.

OVRUN (Read Overrun)

Data buffer was full and controller tried to overwrite, or data buffer was empty and CPU attempted to fetch. Setting is prohibited by EOD, and is cleared when the next command is sent to the interface.

Note: Write Overrun is detected by the controller whenever the data buffer is empty and the controller attempts to fetch (unless EOD is also set).

XFRNG (Transfer No Good)

False unless the interface or channel detects an error condition (other than overrun) which prohibits transfer of data. Cleared by STINT.

INTOK (Interrupt OK)

True if the interface may be interrupted due to a disc drive attention request. Other interrupt conditions do not examine this flag.

Function Bus Orders

Orders listed are validated by IFVLD. Any edge validations are by trailing edge.

BUSY

Interface must be selected. ENIR is true. Clocks bit 0 of the data bus into a bit on the interface which, when bit 0 is high, signifies that the controller has accepted a command and is executing it, and the requested disc drive (if any) is available. (Bit 0 low – not busy.) Use IFVLD as clock. (This function is not mandatory.)

DSCIF (Disconnect Interface)

All interfaces respond. Used to clear interface select bit. When the select bit is false, the interface will not respond to select-required commands, or gate its flags or data bus out to the controller. Use IFVLD as clock. (This function is mandatory only for multiple-CPU subsystems.)

DVEND (Device End)

Interface must be selected. Transmitted by the controller to terminate an operation it considers retryable (correctable or uncorrectable data error on read operations, overrun on any data operation). May be used to increment a retry counter, must signal that the current controller command has completed. Use IFVLD as clock.

OVRUN (Read Overrun)

Data buffer was full and controller tried to overwrite, or data buffer was empty and CPU attempted to fetch. Setting is prohibited by EOD, and is cleared when the next command is sent to the interface.

Note: Write Overrun is detected by the controller whenever the data buffer is empty and the controller attempts to fetch (unless EOD is also set).

XFRNG (Transfer No Good)

False unless the interface or channel detects an error condition (other than overrun) which prohibits transfer of data. Cleared by STINT.

INTOK (Interrupt OK)

True if the interface may be interrupted due to a disc drive attention request. Other interrupt conditions do not examine this flag.

Function Bus Orders

Orders listed are validated by IFVLD. Any edge validations are by trailing edge.

BUSY

Interface must be selected. ENIR is true. Clocks bit 0 of the data bus into a bit on the interface which, when bit 0 is high, signifies that the controller has accepted a command and is executing it, and the requested disc drive (if any) is available. (Bit 0 low – not busy.) Use IFVLD as clock. (This function is not mandatory.)

DSCIF (Disconnect Interface)

All interfaces respond. Used to clear interface select bit. When the select bit is false, the interface will not respond to select-required commands, or gate its flags or data bus out to the controller. Use IFVLD as clock. (This function is mandatory only for multiple-CPU subsystems.)

DVEND (Device End)

Interface must be selected. Transmitted by the controller to terminate an operation it considers retryable (correctable or uncorrectable data error on read operations, overrun on any data operation). May be used to increment a retry counter, must signal that the current controller command has completed. Use IFVLD as clock.

IFIN (Data In, Controller to Interface)

Interface must be selected. ENIR is true. Enables transfers into the CPU from the controller. While IFIN is true, the trailing edge of IFCLK validates individual word transfers. This function is used for all transfers into the CPU.

IFGTC (Get Command from Interface)

Interface must be selected. ENID is true. Used to gate the contents of the command register on the interface onto the data bus. Clears CMRDY flag.

IFIN (Data In, Controller to Interface)

Interface must be selected. ENIR is true. Enables transfers into the CPU from the controller. While IFIN is true, the trailing edge of IFCLK validates individual word transfers. This function is used for all transfers into the CPU.

IFGTC (Get Command from Interface)

Interface must be selected. ENID is true. Used to gate the contents of the command register on the interface onto the data bus. Clears CMRDY flag.

IFOUT (Data Out, Interface to Controller)

Interface must be selected. ENID is true. Gates the interface data buffer onto the data bus. Data is accepted by the controller at the leading edge of IFCLK. Transfer validation is indicated by the trailing edge of IFCLK. Used in all word fetches to the controller except command fetch which uses IFGTC.

IFPRF (Pre-Fetch Command from Interface)

Interface must be selected. ENID is true. Gates the contents of the command register of the interface onto the data bus (as in IFGTC) but does not clear the CMRDY flag or otherwise alter the environment on the interface. Thus the same command can be obtained any number of times with this order. IFGTC should be used when the command is being obtained for the last time.

RQSRV (Request Service)

Interface must be selected. Sets service request explicitly at the end of any block transfer (in or out) involving more than the command word (e.g., SEEK, READ, STATUS, etc.). While a block transfer is in progress, the interface may not fetch the next command unless it goes to a buffer other than the data buffer. RQSRV signals the interface that the controller has finished with its block transfer and it is all right to fetch the next command. Use IFVLD as clock. (This function is not mandatory.)

SELIF (Select Interface)

Interface need not be selected. ENIR is true. A three-bit address is present on the lower three bits of the data bus. If it matches the jumpered address on the interface, the interface uses IFVLD to set its select bit. When the select bit is true the interface responds to the select-required commands, responds to ENID, and gates its flags to the controller. (Mandatory only for multiple-CPU subsystems. Otherwise the interface may have its select bit wired true.)

SRTRY (Set Retry Counter)

Interface must be selected. ENIR is true. One byte of mode control data is present on the lower byte (8 bits) of the data bus. The lower 4 bits of this byte is interpreted by the controller and should be ignored by the interface. The upper 4 bits of this lower byte is for use by the interface (e.g., as a retry counter setting). This byte is an image of the lower byte passed in a Set File Mask controller instruction. Use IFVLD as clock. (This function is not mandatory.)

STDFL (Set Data Flag)

Interface must be selected. Sets a bit on the interface:

To request direct transfer of a single word (SEEK, ADDRESS RECORD, STATUS, REQUEST SYNDROME, VERIFY, READ WITH OFFSET, REQUEST SECTOR, LOAD TIO REGISTER).

When a data operation is complete (COLD LOAD, READ, READ FULL SECTOR, VERIFY, WRITE, WRITE FULL SECTOR, INITIALIZE, READ WITH OFFSET, READ WITHOUT VERIFY).

To signal completion of a single-transaction command (SET FILE MASK, WAKEUP, CLEAR). May be used to set interrupt request. Use IFVLD as clock. (This function is not mandatory.)

STINT (Set Interrupt)

Interface must be selected. Sets interrupt request bit on the interface when the controller discovers an error condition, or when a drive is requesting attention.

WRTIO

Interface must be selected. ENIR is true. Data bus (full sixteen bits) contains controller status to be clocked into a CPU-testable status register. Use IFCLK trailing edge as clock. (This function is not mandatory.)

Function Bus Summary

FUNCTION BUS	MNEMONIC	FUNCTION DESCRIPTION	DATA BUS CONTENTS
00	STINT	Interrupt Request	
01	STDFL	Information Request	
02	IFPRF	Pre-fetch Command	Command Word
03	SELIF	Select Interface	Interface Address
04	SRTRY	Set Retry Counter	Retry Count
05	DVEND	Device End	
06		(Reserved)	
07	RQSRV	Request Service	
10		(Reserved)	
11	DSCIF	Disconnect Interface	
12	WRTIO	Write TIO	Status-1
13	IFOUT	Data Out (Write to Disc)	Data
14	IFIN	Data In (Read from Disc)	Data
15	IFGTC	Get Command	Command Word
16	BUSY	Set/Clear Controller Busy Bit	Busy Status
17		(Reserved)	

INTERRUPTS

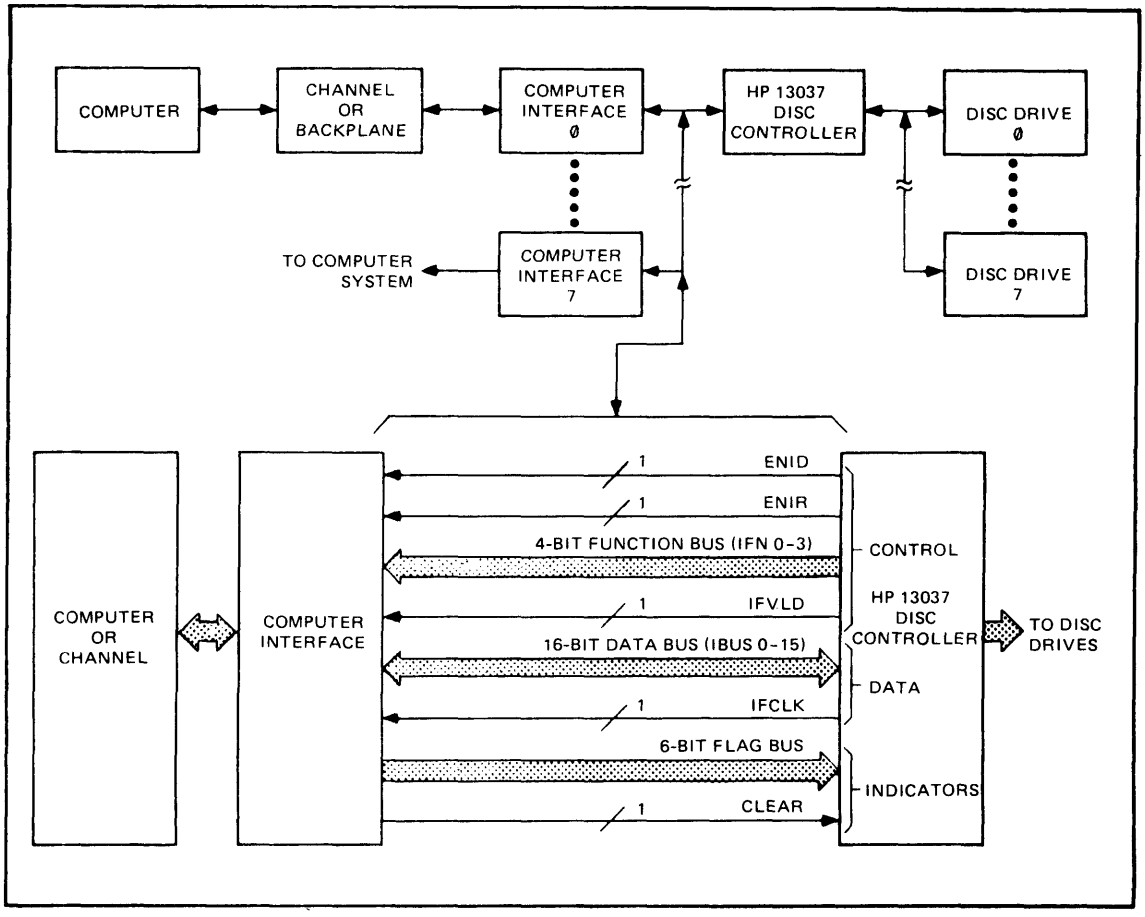
The controller generally will request an interrupt (i.e., transmit STINT or DVEND) whenever the S1 field of the Status-1 word becomes non-zero (when the S1 field indicates a drive attention status, the INTOK flag must also be true for STINT to be transmitted). This includes driver status changes (access ready error), incorrect conditions encountered during an operation (Status-2 error, address miscompare, defective or spare track access error, etc.) or program error (end of logical cylinder, illegal opcode). Additionally, at the end of a data transfer, the controller transmits STDFL to the interface, which may cause an interrupt.

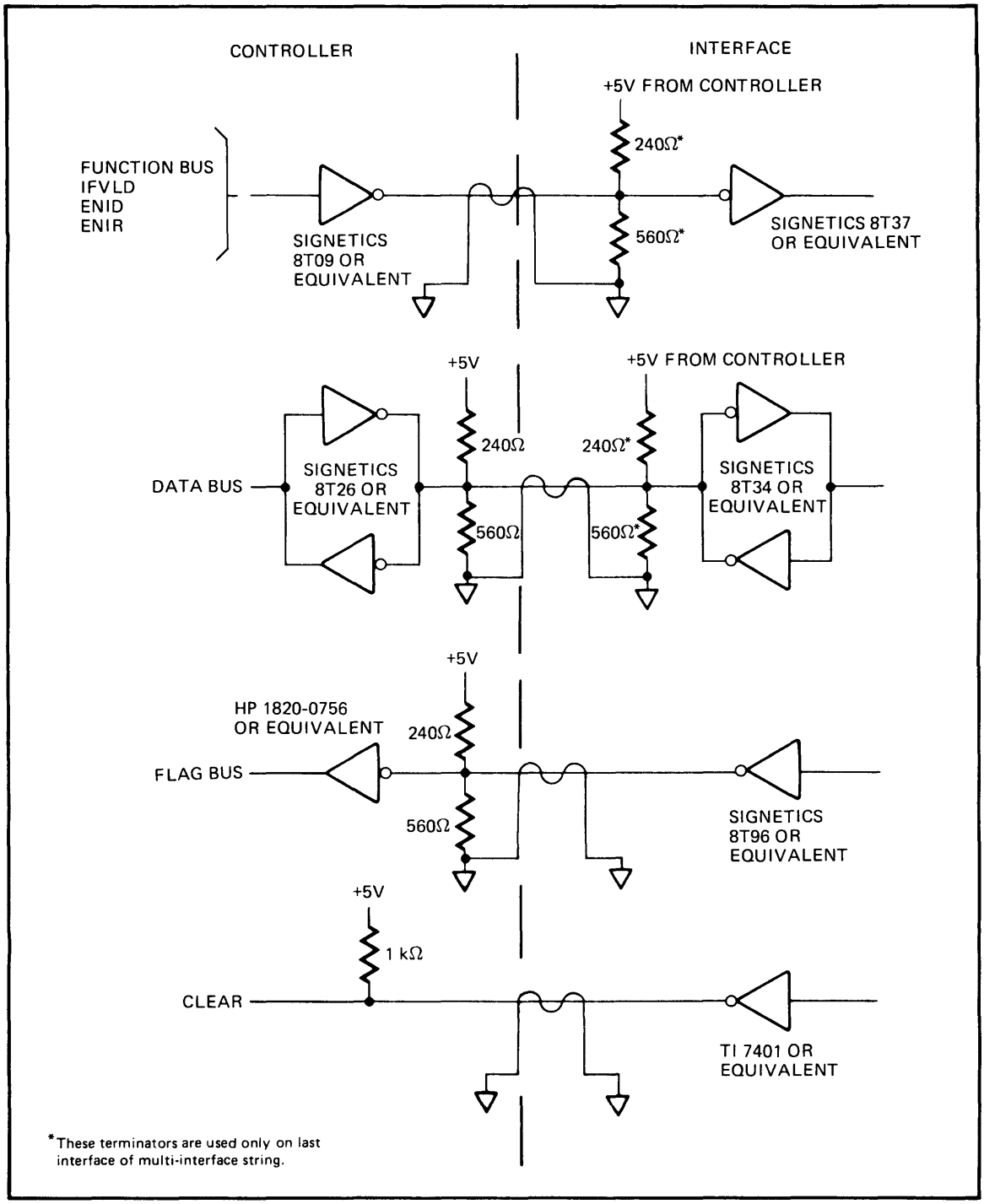
On any interrupt or command completion the CPU should examine the TIO register (if used) or perform a status operation to determine the cause and, if applicable, the unit number.

Overrun, Possibly Correctable Data Error, and Uncorrectable Data Error are considered retryable, so rather than transmit STINT, the controller transmits DVEND to the interface and increments the retry counter (if used). However, if the retry counter rolls over, the interface will interrupt the CPU. If the S1 field indicates that a Possibly Correctable Data Error has occurred, the CPU may attempt to correct this error by issuing a REQUEST SYNDROME command to the controller.

Note that interrupts generated for non-zero S1 fields of the Status-1 word will cause the controller to clear any attention bit from the drive before accepting any subsequent commands.

Controller Interface




CONTROLLER
INTERFACE
+5V FROM CONTROLLER
240Ω*
FUNCTION BUS
IFVLD
ENID
ENIR
SIGNETICS
8T09 OR
EQUIVALENT
560Ω*
SIGNETICS 8T37
OR EQUIVALENT
+5V
+5V FROM CONTROLLER
240Ω
240Ω*
DATA BUS
SIGNETICS
8T26 OR
EQUIVALENT
560Ω
560Ω*
SIGNETICS
8T34 OR
EQUIVALENT
+5V
HP 1820-0756
OR EQUIVALENT
240Ω
FLAG BUS
560Ω
SIGNETICS
8T96 OR
EQUIVALENT
+5V
1 kΩ
CLEAR
TI 7401 OR
EQUIVALENT
*These terminators are used only on last
interface of multi-interface string.

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60028
13037-66028
13037-68028

DATE CODE : F-2135

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C101	0160-2055	CAP .01UF-20+80%
C103	0160-2055	CAP .01UF-20+80%
C104	0160-2055	CAP .01UF-20+80%
C105	0160-2055	CAP .01UF-20+80%
C106	0160-0128	CAP 2.2UF 20%
C107	0180-0374	CAP 10UF 10%
C110	0160-2055	CAP .01UF-20+80%
C111	0180-0291	CAP 1UF 10%
C112	0180-0374	CAP 10UF 10%
C113	0160-2055	CAP .01UF-20+80%
C114	0160-2055	CAP .01UF-20+80%
C115	0160-2055	CAP .01UF-20+80%
C201	0160-2055	CAP .01UF-20+80%
C202	0160-2055	CAP .01UF-20+80%
C203	0160-2055	CAP .01UF-20+80%
C204	0160-2055	CAP .01UF-20+80%
C205	0160-2055	CAP .01UF-20+80%
C206	0160-2055	CAP .01UF-20+80%
C207	0160-2055	CAP .01UF-20+80%
C210	0160-2055	CAP .01UF-20+80%
C211	0160-2055	CAP .01UF-20+80%
C212	0160-2055	CAP .01UF-20+80%
C213	0160-2055	CAP .01UF-20+80%
C214	0160-2055	CAP .01UF-20+80%
C215	0160-2055	CAP .01UF-20+80%
C216	0160-2055	CAP .01UF-20+80%
C217	0160-2055	CAP .01UF-20+80%
C218	0160-2055	CAP .01UF-20+80%
C220	0160-2055	CAP .01UF-20+80%
C221	0160-2055	CAP .01UF-20+80%
C223	0160-2055	CAP .01UF-20+80%
C224	0160-2055	CAP .01UF-20+80%
C225	0160-2055	CAP .01UF-20+80%
C301	0160-2055	CAP .01UF-20+80%
C302	0160-2055	CAP .01UF-20+80%
C303	0160-2055	CAP .01UF-20+80%
C304	0160-2055	CAP .01UF-20+80%
C305	0160-2055	CAP .01UF-20+80%
C306	0160-2055	CAP .01UF-20+80%
C307	0160-2055	CAP .01UF-20+80%
C310	0160-2055	CAP .01UF-20+80%
C311	0160-2055	CAP .01UF-20+80%
C312	0180-1714	CAP 330UF 10%
C313	0160-2055	CAP .01UF-20+80%
C314	0160-0939	CAP 430PF 5%
C315	0150-0121	CAP .1UF-20+80%
C316	0160-3456	CAP 1000PF 10%

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60028
13037-66028
13037-68028

DATE CODE : F-2135

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C317	0160-2055	CAP .01UF-20+80%
C318	0160-2055	CAP .01UF-20+80%
C320	0160-3459	CAP .02UF 20%
C321	0150-0121	CAP .1UF-20+80%
C322	0160-2055	CAP .01UF-20+80%
C323	0150-0121	CAP .1UF-20+80%
C324	0160-2055	CAP .01UF-20+80%
C325	0160-2055	CAP .01UF-20+80%
CR101	1990-0485	LED-VISIBLE
CR102	1901-0518	DIODE-SCHOTTKY
CR302	1901-0518	DIODE-SCHOTTKY
CR303	1901-0518	DIODE-SCHOTTKY
CR304	1901-0460	STABISTOR STB523
CR305	1901-0866	DIODE STABISTOR
CR306	0122-0094	DIO 34PF 10%
H177	0764-0013	RES 56 5% 2W
H177	1200-0482	SOCKET 16 DIP LO
L301	9100-3550	IDCTR 620NH 5%
Q101	1854-0477	XSTR 2N2222AT018
Q102	1854-0477	XSTR 2N2222AT018
Q103	0340-0164	INSUL-XSTR
Q103	1205-0011	HT DIS TO-5
Q103	1826-0179	IC V REG -5
Q301	1854-0071	XSTR NPN SI PL5
Q302	1854-0071	XSTR NPN SI PL5
Q303	1854-0071	XSTR NPN SI PL5
R101	0698-3441	RES 215 1%.125
R102	0683-3325	RES 3300 5% .25
R103	0757-0459	R:F 56.2K 1%.125
R104	0757-0459	R:F 56.2K 1%.125
R105	0757-0420	RES 750 1%.125
R106	0757-0420	RES 750 1%.125
R107	0757-0280	RES 1K 1%.125
R108	0757-0420	RES 750 1%.125
R110	0757-0420	RES 750 1%.125
R111	0683-4715	RES 470 5% .25
R112	1810-0030	RES NET 7X1K
R113	1810-0127	RES N 6(240+560)
R114	0757-1060	RES 196 1% .50
R116	1810-0127	RES N 6(240+560)
R117	0683-1035	RES 10K 5% .25
R120	1810-0030	RES NET 7X1K
R121	1810-0127	RES N 6(240+560)
R122	0764-0013	RES 56 5% 2W
R123	1810-0127	RES N 6(240+560)
R201	0698-3435	RES 38.3 1%.125
R202	0698-3435	RES 38.3 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60028
13037-66028
13037-68028

DATE CODE : F-2135

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R203	0698-3435	RES 38.3 1%.125
R204	0698-3435	RES 38.3 1%.125
R205	0698-3435	RES 38.3 1%.125
R206	0698-3435	RES 38.3 1%.125
R207	0698-3435	RES 38.3 1%.125
R208	0698-3435	RES 38.3 1%.125
R211	0698-3435	RES 38.3 1%.125
R212	0698-3435	RES 38.3 1%.125
R213	0698-3435	RES 38.3 1%.125
R214	0698-3435	RES 38.3 1%.125
R215	0698-3435	RES 38.3 1%.125
R216	0698-3435	RES 38.3 1%.125
R217	0698-3435	RES 38.3 1%.125
R220	0698-3435	RES 38.3 1%.125
R221	0757-0346	RES 10 1%.125
R222	0698-3398	RES 46.4 1% .50
R301	1810-0127	RES N 6(240+560)
R302	1810-0030	RES NET 7X1K
R303	1810-0127	RES N 6(240+560)
R304	1810-0030	RES NET 7X1K
R305	1810-0127	RES N 6(240+560)
R306	0683-2215	RES 220 5% .25
R310	0757-0401	RES 100 1%.125
R311	0683-3315	RES 330 5% .25
R312	0757-0421	RES 825 1%.125
R313	0757-0421	RES 825 1%.125
R314	0757-0419	RES 681 1%.125
R315	0698-0082	RES 464 1%.125
R316	0757-0280	RES 1K 1%.125
R317	0757-0280	RES 1K 1%.125
R321	0698-4037	RES 46.4 1%.125
R322	0683-0685	RES 6.8 .25 5%
R323	2100-3345	RES-VAR-TRMR
R324	0757-0403	RES 121 1%.125
R325	0757-0399	RES 82.5 1%.125
R326	0757-0403	RES 121 1%.125
R327	0757-0399	RES 82.5 1%.125
R330	1810-0030	RES NET 7X1K
R331	0757-0280	RES 1K 1%.125
R332	0757-0280	RES 1K 1%.125
U101	1820-1053	IC SN7414N
U102	1820-0723	IC SN75107N
U103	1820-0722	IC SN75109N
U106	1820-1081	IC N8T26B
U107	1820-0574	IC DM8551N
U108	1820-1196	IC SN74LS174N
U111	1820-0511	IC SN7408N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60028
13037-66028
13037-68028

DATE CODE : F-2135

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U112	1820-0723	IC SN75107N
U113	1820-0722	IC SN75109N
U116	1820-1081	IC N8T26B
U117	1820-0574	IC DM8551N
U118	1820-1195	IC SN74LS175N
U12	1826-0180	IC 555 8-DIP-P
U121	1820-0693	IC SN74S74N
U126	1820-1081	IC N8T26B
U127	1820-0574	IC DM8551N
U128	1820-0726	IC N74199N
U129	1820-0577	IC SN7416N
U131	1820-0693	IC SN74S74N
U132	1820-0690	IC SN74S40N
U133	1820-0370	IC SN74H00N
U134	1820-0055	IC SN7490N
U138	1820-1196	IC SN74LS174N
U14	1820-0141	IC MC3001P
U141	1820-0693	IC SN74S74N
U142	1820-0424	IC SN74H04N
U143	1820-1367	IC SN74S08N
U144	1820-0715	IC SN74H106N
U145	1820-0715	IC SN74H106N
U146	1820-0685	IC SN74S10N
U148	1820-0141	IC MC3001P
U149	1820-1084	IC N8T09B
U151	1820-0693	IC SN74S74N
U152	1810-0198	I.C. DELAY LINE
U153	1820-1307	IC SN74S132N
U154	1820-0056	IC SN7492N
U155	1820-0629	IC SN74S112N
U156	1820-0629	IC SN74S112N
U157	1820-0681	IC SN74S00N
U158	1820-1195	IC SN74LS175N
U159	1820-0628	IC SN7489N
U16	1820-0693	IC SN74S74N
U161	1820-1191	IC SN74S175N
U162	1820-0374	IC SN74H21N
U163	1820-0681	IC SN74S00N
U164	1820-0681	IC SN74S00N
U165	1820-0683	IC SN74S04N
U166	1820-0629	IC SN74S112N
U167	1820-0681	IC SN74S00N
U168	1820-0661	IC SN7432N
U169	1820-0174	IC SN7404N
U17	1820-1084	IC N8T09B
U171	1820-0693	IC SN74S74N
U172	1820-0685	IC SN74S10N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60028
13037-66028
13037-68028

DATE CODE : F-2135

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U173	1820-0688	IC SN74S20N
U174	1820-0681	IC SN74S00N
U175	1820-0629	IC SN74S112N
U177	1200-0482	SOCKET 16 DIP LO
U177	1820-1052	IC MC10125
U178	1820-0683	IC SN74S04N
U179	1820-0685	IC SN74S10N
U18	1820-1112	IC SN74LS74N
U181	1820-0693	IC SN74S74N
U185	1820-1108	IC MC1648P
U187	1820-0817	IC MC10131
U188	1820-1158	IC SN74S51N
U189	1820-0681	IC SN74S00N
U19	1820-0756	IC HP147B
U21	1820-1084	IC N8T09B
U22	1820-1425	IC SN74LS132N
U23	1820-0054	IC SN7400N
U24	1820-0661	IC SN7432N
U25	1820-0902	IC SN75450AN
U26	1820-1112	IC SN74LS74N
U27	1820-1195	IC SN74LS175N
U29	1820-0661	IC SN7432N
U31	1820-0681	IC SN74S00N
U32	1820-1084	IC N8T09B
U33	1820-1112	IC SN74LS74N
U34	1820-1121	IC 8093N
U35	1820-0661	IC SN7432N
U36	1820-1112	IC SN74LS74N
U37	1820-1112	IC SN74LS74N
U38	1820-1196	IC SN74LS174N
U39	1820-0174	IC SN7404N
U41	1820-0054	IC SN7400N
U42	1820-0716	IC SN74161N
U43	1820-1262	IC 74290
U44	1820-0683	IC SN74S04N
U45	1820-0054	IC SN7400N
U46	1820-1112	IC SN74LS74N
U47	1820-1196	IC SN74LS174N
U48	1820-0661	IC SN7432N
U49	1820-0661	IC SN7432N
U51	1820-0998	IC SN74S153N
U52	1820-1112	IC SN74LS74N
U53	1820-0239	IC MC3002P
U54	1820-0726	IC N74199N
U56	1820-1081	IC N8T26B
U57	1820-1195	IC SN74LS175N
U58	1820-1195	IC SN74LS175N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60028
13037-66028
13037-68028

DATE CODE : F-2135

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U59	1820-0495	IC SN74154N
U61	1820-1158	IC SN74S51N
U62	1820-1112	IC SN74LS74N
U63	1820-0070	IC SN7430N
U64	1820-0239	IC MC3002P
U66	1820-1081	IC N8T26B
U67	1820-1196	IC SN74LS174N
U68	1820-1196	IC SN74LS174N
U69	1820-0683	IC SN74S04N
U72	1820-0054	IC SN7400N
U73	1820-0282	IC SN7486N
U74	1820-0726	IC N74199N
U76	1820-1081	IC N8T26B
U77	1820-1196	IC SN74LS174N
U78	1820-1196	IC SN74LS174N
U81	1820-1053	IC SN7414N
U82	1820-0723	IC SN75107N
U83	1820-0722	IC SN75109N
U86	1820-1081	IC N8T26B
U88	1820-1112	IC SN74LS74N
U91	1820-1323	IC SN74S30N
U92	1820-0723	IC SN75107N
U93	1820-0722	IC SN75109N
U96	1820-1081	IC N8T26B
U97	1820-0574	IC DM8551N
U98	1820-0726	IC N74199N

END OF MATERIAL LIST.

ENGINEERING RESPONSIBILITY									SEPIA								
0	1	2	3	4		6		8	9		11	12		14	15		
16	17		19		21	22	23	26	27	30	32	34	37	38	43		
46	48	61	63	65		72											

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0457	[illegible]	4-24-78
B	DELETED U28. PC48-0565	LO	5-16-78
C	UPDATED DESIGNATORS PC 48-1631	K·F·L/R	4-20-79
D	CORRECTED DWG OF U14 REF, CURRENT DATE CODE E-1905 PC48-3341	[illegible]	11-16-81
E	CURRENT DATE CODE E-2135 PC 48-3361	K.F./ML	11.25.82
F	CURRENT DATE CODE F-2135 PCO 48-3405	K.F./MJM	2.11.83

D-13037 -60028 -51

INTERFACE BUS, RECEIVE SECTION SHOWN ON OTHER PAGE

CONTRO BUS RECEIVE SECTION SHOWN ON OTHER PAGE

TO SERDES INPUT REGISTER RAM

C 104, 105, 112, 113, 114, 115, 201, 202, 207, 213, 214, 218, 225
301, 302, 305, 304, 305, 310, 311, 313, 318, 324

P1-15,16,19,20,29,30
P2-1,50
P3-1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49.
J1-15,16,17,20,33,34,49,50
J3-11,12,14,15,16,19,20,29,31,33,34,45,46,47,48,49,50

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY	2-22-78 DATE	DEVICE CONTROLLER MIO BUS-OUTPUT SECTION SCHEMATIC (TITLE)
ENGINEER		HEWLETT PACKARD
RELEASE TO PROD.	4-28-78	SEE WHERE USED (NEXT ASSEMBLY)
SUPERSEDES DWG.		FINISH — SCALE NONE

13037-60028 (PART NUMBER)

D-13037 -60028 -51

SHEET 1 OF 1

SYM	REVISIONS	DATE
C	CURRENT DATE CODE E-2135 PCO 48-3321	M.F./ES 11.20.81
D	CURRENT DATE CODE E-2135 PCO 48-3405	M.F./KM 2.11.82

ENGINEERING RESPONSIBILITY																SEPIA
0	1	2	3	4		6	8		11	12	14	16				
16	17		19		21	22	23	25	28	30	32	33	38	43		
40	46	61	63	16												

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0457	M.F./EC	4.24.78
B	UPDATED DESIGNATOR → PLAN-1631	M.F. KR	4.20.79

D-13037-60028-52

SEE SDS LEFT CORNER FOR NEXT PG. (CONT'D)

CBSIN = 4

SPIBF = 16

IDTBF = 3

FROM U26-1

RAM

RAM = 0

RAM = 1

RAMAD = 0

TST CLR 3

TST CLR 2

TST CLR 12

SERDES

CRCC

CRCC/ ECC CONTROL

BIT COUNT

SERDES INPUT - TO MIO OUTPUT BUS

NOTE: ONE .01 μf CAPACITOR FOR EVERY 3 IC'S

SERIAL DATA FROM ECG

SERIAL DATA OUT

ECC SHIFT ENABLE

RESET EOW

READ/WRITE 2

ENABLE CRCC SHIFT

READ/WRITE

CRCC OUT

LOAD SPIBF

LOAD

SPARES

7408	U111-D
7416	U129 ABDE
74H00	U135 D
74H04	U142-C
3001	U143 B-C
74H106	L144-B
745112	U166 B
74S20	U178 A
74S10	U179 A
74S11	U188-C
7432	U24 C

SPARES (CONT)

74S00	U31 D
74125	U34 C-D
3003	U35 A U163 D
74LS174	U38 B
7404	
7400	U42, U55 C-D
7455	U61-B
74S04	U69 A-F
7480	U78 C
7414	U101-A-C U181 B-C

RES SPARES

R116 E	
R301 C	240/560
R115 E	
R120 A,B	
R304 A	
	1K

ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L PART NO.	MAT'L DWG NO.	MAT'L SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY		2-24-78 DATE
ENGINEER		
RELEASE TO PROD.		4-28-78
SUPERSEDES DWG.		

DEVICE CONTROLLER
INPUT SECTION OF MIO BUS
TITLE SCHEMATIC

SEE WHERE USED
NEXT ASSEMBLY

FINISH — SCALE NONE

HEWLETT PACKARD

PART NUMBER 13037-60028

D - 13037 - 60028 - 52

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY																SEPIA
0	1	2	3	4		6		8	9		11	12	14	15		
16	17		19		21	22	23	25	29	30	32	33	38	43		
45	46	61	63	10		50%	50%	50%								

D-13037-6002B-53

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0457	NO/ [illegible]	4-24-78
B	R314 WAS 464 PC48-0926.	LO/ EC	6-29-78
C	CR305 WAS 1901-0463. PC48-1247.	LO/ EC	12-29-78
D	UPDATE DESIGNATORS PC48-1631	K-F-I AR	4-20-79
E	CURRENT DATE CODE E-2135 PCO 48-3361	K.F./ [illegible]	11.20.81
F	CURRENT DATE CODE F-2135 PCO 48-3405	MF/MSM	2.11.82

FLIP-FLOP STANDARD

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

DO NOT SCALE THIS DRAWING	DRAWN BY	2-6-78 DATE	DEVICE CONTROLLER FORMATTER / SEPARATOR TITLE SCHEMATIC
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.	ENGINEER	4-25-78	HEWLETT PACKARD
TOLERANCES .XX ± .02 .XXX ± .005	RELEASE TO PROD.	4-28-78	SEE WHERE USED / 13037-60028
SEE CORP. STD. 608	MERSEDES DWG.		NEXT ASSEMBLY / PART NUMBER
			FINISH — / SCALE NONE / D-13037-60028-53

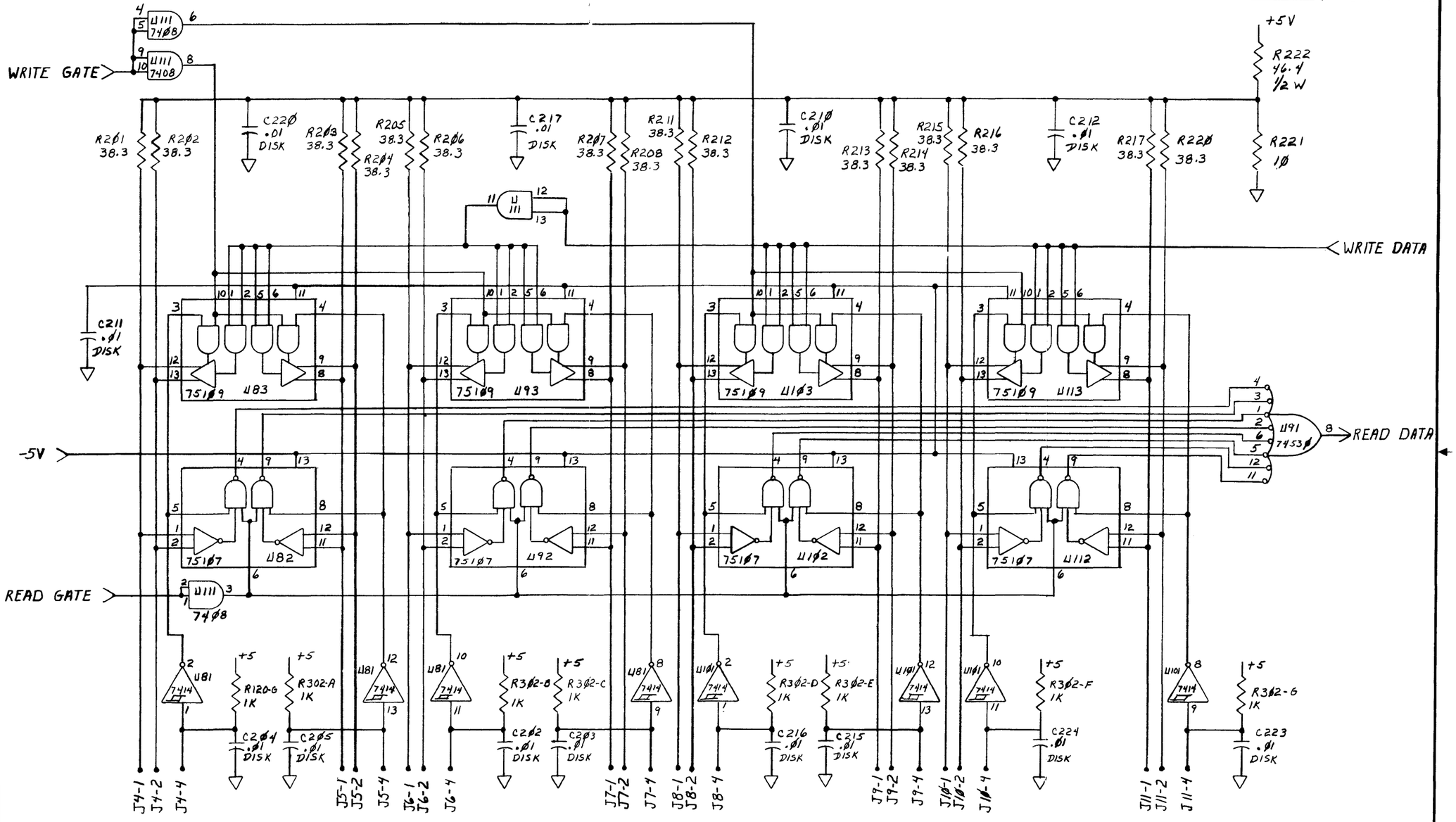
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY ▨ SEPIA ▨

0	1	2	3	4		6		8	9	11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	83	86		89 A	90 A	91 A		C A	C3	85		

C-13037-60028-54

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED. PC48-0457	ND/BC	4-24-78
B	CURRENT DATE CODE E-2135 PC48-3361	K.F./KS	11.20.81
C	CURRENT DATE CODE F-2135 PCO 48-3405	K.F./MSM	2.11.82



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

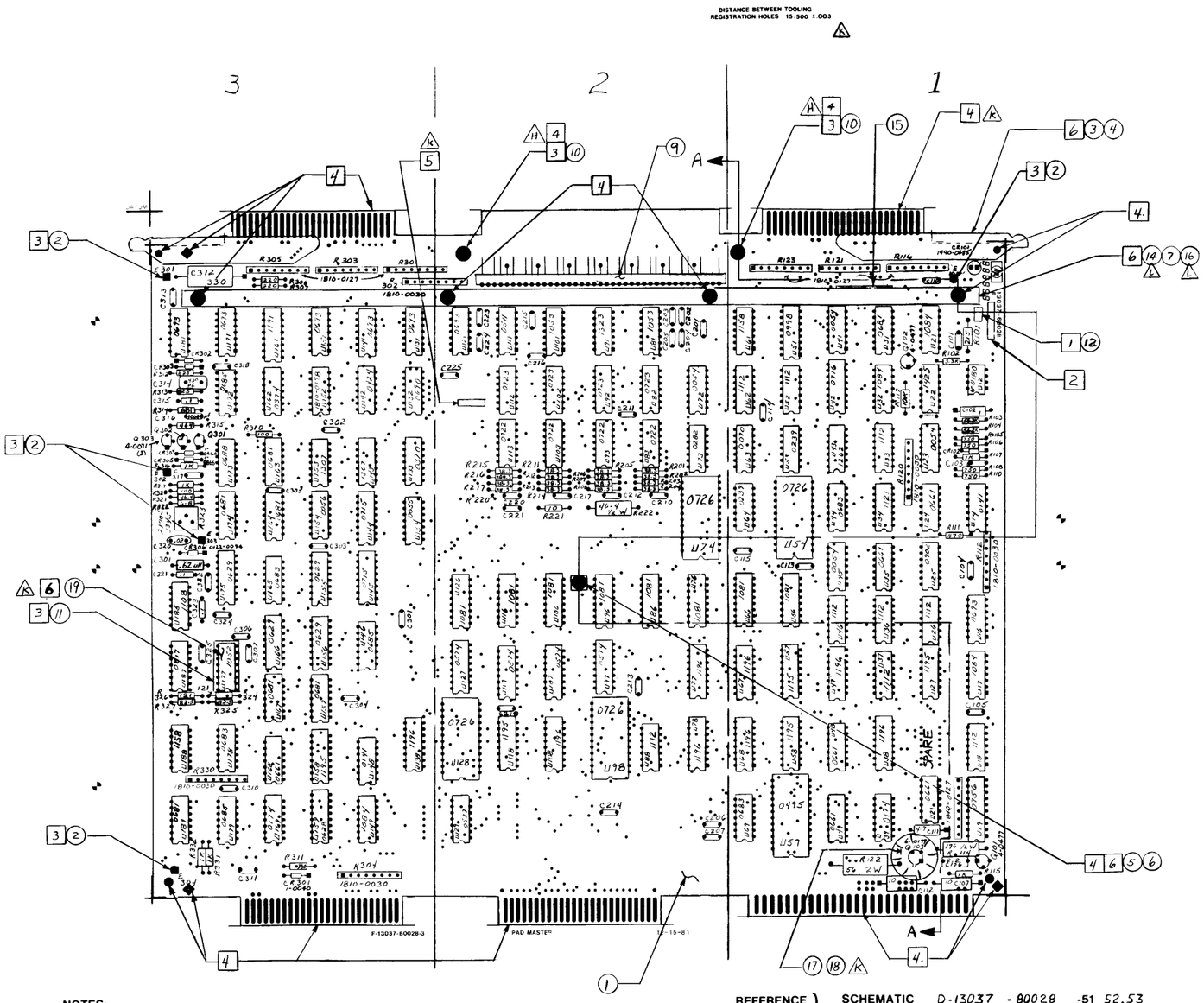
SEE CORP. STD. 608

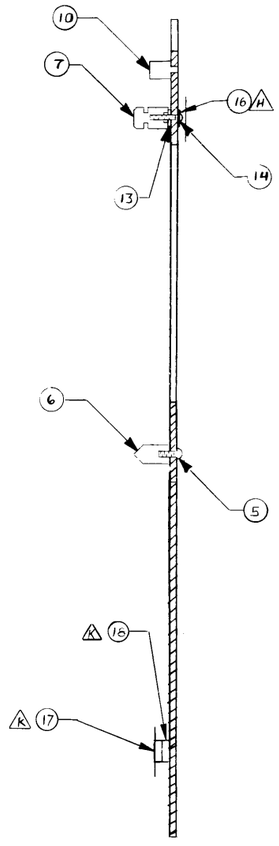
DRAWN BY	2-6-78 DATE	DEVICE CONTROLLER SCHEMATIC TITLE
ENGINEER	4-25-78	HEWLETT PACKARD
RELEASE TO PROD.	4-25-78	SEE WHERE USED NEXT ASSEMBLY
SUPERSEDES DWG.		FINISH SCALE NONE

PART NUMBER 13037-60028

C-13037-60028-54

SHEET 1 OF 1





NOTES:

1. INSTALL ITEM (12) AFTER LINE TEST.
2. MARK ASSEMBLY DATE CODE 2135
3. INSTALL ITEMS (2) 5PLCS, (10) 2PLCS, (11) 1PLC. BEFOR WAVE SOLDER
4. MASK PRIOR TO LOADING
5. P.C PRODUCTION: MARK WORK ORDER NUMBER COMPONENT SIDE.
6. TOUCH UP, INSTALL ITEMS (3) THRU (7), (19)
7. CLEAN CONNECTOR IN TOUCH UP.

REFERENCE DRAWINGS } SCHEMATIC D-13037-80028-51 52,53
C-13037-80028-54

UNLESS NOTED OTHERWISE:

ALL RESISTANCE IN OHMS
ALL RESISTORS 1/4 W ±1%
ALL CAPACITANCE IN MICROFARADS
ALL CAPACITORS .01 CER. DISC
ALL IC's 1820-____
ALL DIODES 1901-0518

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0457	WD/EC	4.18.78
B	SHOW U28 AS SPARE. U88 WAS 0686 PC48-0565	LO/EC	5-16-78
C	R314 WAS 464, DATE CODE WAS 1815. PC48-0926.	LO/EC	8-29-78
D	CR305 WAS 1901-0463. PC48-1247.	LO/EC	12-29-78
E	ADD SECTION A-A, ADD'L STIFFNER AND BUSHING, 0340-0500 DELETED 5040-6058 BRACE DATE CODE WAS 1835 PC48-1546	TTJ/A	3-9-79
F	DELETED ITEM 8 (7120-7348) AND NOTE 8 PC 48-1853	K.F./EC	8.20.79
G	ADDED ITEM 15. PC48-2031	LO/TAS	11.21.79
H	ADDED ITEM 16, 2190-0913, QTY 4; ADDED REF NOTE (4), 3 LOCATIONS PC 48-2963	WD/KB	2-25-81
J	REVISED PER PCO 48-3361	K.F./KB	11.20.81
K	REVISED PER PCO 48-3405	K.F./MJM	2.11.82
L	REV'D PER PER PC 48-3604	WD/MJM	4.5.83

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L PART NO.	MAT'L DWG. NO.	MAT'L SPEC.
19	1	IC MC10125 (U177)	1820-1052		
18	1	INSUL-XSTR	0340-0164		
17	1	HT DIS TO-5	1205-0011		
16	4	WASHER-LK HLCL	2190-0913		
15	1	LABEL-IDENTIFICATION	7120-4326		
14	4	4-40 x 0.375 SCREW	2200-0143		
13	4	INSUL-FLG-BSHG	0340-0500		
12	1	LABEL-INFO	7120-6830		
11	1	SOCKET 16 PIN	1200-0482		
10	2	STANDOFF 6-32X.312	0380-0198		
9	1	CONNECTOR	1251-4219		
8		DELETED			
7	1	BOARD STIFFENER	13037-20006		
6	1	SPACER	5020-7318		
5	1	SCREW	0624-0077		
4	2	EXTRACTOR	5040-6009		
3	2	PIN	1480-0116		
2	5	TERMINAL E101 + E301-E305	0360-0274		
1	1	BOARD ETCHED	13037-80028		

DO NOT SCALE THIS DRAWING	DRAWN BY	3-2-78 DATE	DEVICE CONTROLLER ASSY. DWG. TITLE
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES .XX ± .02 .XXX ± .005 SEE CORP. STD. 608	ENGINEER	4-18-78	HEWLETT PACKARD
	RELEASED TO PROD.	4-28-78	SEE WHERE USED NEXT ASSEMBLY
	SUPERSEDES DWG.		FINISH — SCALE 1:1

13037-60028 PART NUMBER

D-13037-60028-1

SHEET 1 OF 1

CONTENTS

Page

1.0 GENERAL DESCRIPTION 5-1
2.0 BLOCK DIAGRAM AND FUNCTIONAL DESCRIPTION 5-1
2.1 Write 1 Sector Operation 5-3
2.2 Read 1 Sector Operation 5-3
2.3 Error Correction 5-4
2.3.1 Burst Positioning 5-4
2.3.2 Matching the Positioned Burst 5-5
2.3.3 Adjusting the Pattern to Word Boundaries 5-5
2.4 Hardware 5-5
2.4.1 Data Buffer 5-5
2.4.2 Clock Suppressor 5-7
2.4.3 Timing of Read and Write Operations 5-7
3.0 Expanded Description 5-11
3.1 Firmware Commands 5-11
3.2 Write Operations 5-13
3.3 Read Operations 5-13
3.4 Error Recovery 5-14
3.4.1 Detection 5-14
3.4.2 Correction 5-16

ERROR CORRECTION PCA

1.0 GENERAL DESCRIPTION

The 13037-60024 error correction (ECC) PCA is a single 3000 I/O-type printed circuit board installed within the 13037 disc controller. This board requires 3.5 amps.

Serial binary data is supplied to the ECC hardware along with the data clock during a WRITE data operation, and at the end of the data, 95 bits of check information are retrieved from the ECC hardware, to be written in the last six word-fields of a sector on the disc. These six words contain useful information that enables the 13037 controller to ensure data integrity or recovery in case of errors on subsequent READ data operations.

Serial binary data along with the data clock is supplied to the ECC hardware during certain READ operations (VERIFY command or RECC), and in the event that possibly correctable data errors are detected during the transfer, the CPU interface may request the 13037 controller to attempt to correct the errors. This is accomplished by issuing a single command RQSYN to the controller, and at the end of its execution seven words are returned to the interface that pertain to the recovery from the erroneous data transfer.

Every single burst error of length $\leq$ 32 bits in a sector can be corrected; every single burst error of length $>$ 32 but $\leq$ 48 bits can be detected without being mis-corrected and 99.99% of all other errors will be detected.

2.0 BLOCK DIAGRAM AND FUNCTIONAL DESCRIPTION

The ECC hardware listens to the ECC firmware commands only; consequently, the proper execution of the ECC commands enables one to determine the proper functioning of the hardware. What follows is a general description and a command-by-command description of the hardware and its functions.

The ECC hardware basically consists of thirteen 8-bit 74199 shift registers (U23, U26, U53, U83, U106, U113, U126, U143, U146, U173, and U176) with appropriate feedback through XOR gates (U33, U34, U36, U37, U63, U64, U66, U67, U85, U86, U93, U94, U123, U136, U153, U156, U157, U183, U186, U187, and U168). The feedback is fanned out to the XOR gates or the 74199 D-inputs via two levels of 74S04 inverters U138, U158). There is a 74S157 multiplexer IC (U169) which, when applied with a "select" control signal (U108 pin 14), enables the thirteen 74199's to be interconnected to form two configurations:

A. The ENCODER. A single serial 95-bit shift register. This configuration is obtained for any WRITE data operations only.

B. The DECODER. Two serial-shift-registers: One 42 bits long, called the P-register (U113, U83, U53, U23, U173, and U143); and the other 53 bits long, called the C-register (U106, U76, U56, U26, U176, U146, and U126). Both have the serial DATA applied simultaneously to their inputs. This configuration is attained for any READ & VERIFY data operation only.

   See figure 1-A-B-C.

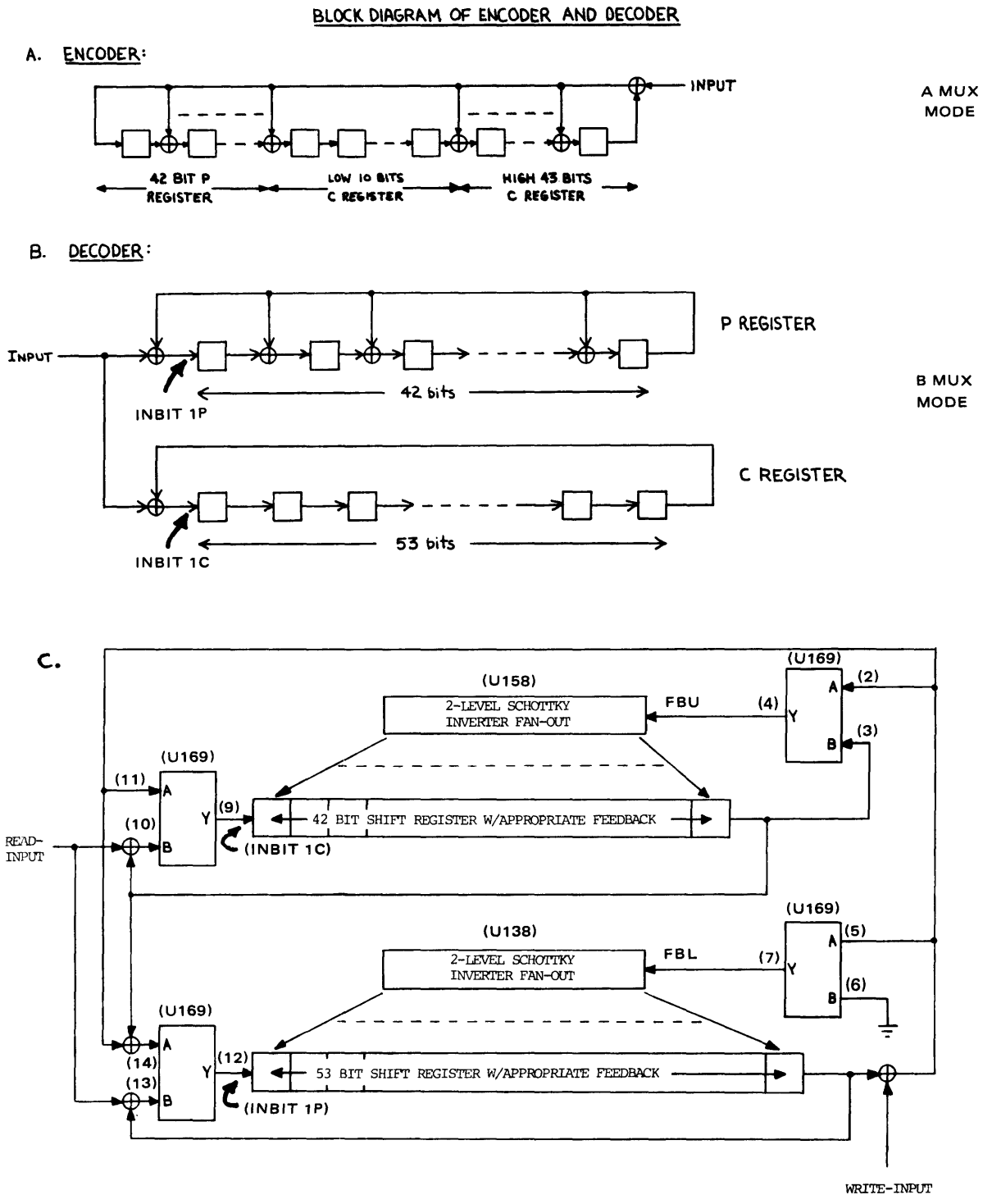


Figure 1. Block Diagram of ENCODER and DECODER

Functionally the ECC assembly can be organized into three different parts and corresponding modes of operation:

2.1 WRITE 1 SECTOR OPERATION

This is intiated by issuing the WECC firmware command, which produces an ECC internal control word (ECICW) interpreted as *WRITE with ECC* and subsequently latched into U108 for further decoding. The effect of the WECC command is:

a) To send out a low level to the multiplexer to select the encoder configuration.

b) To reset the 7493A end-of-word counter IC (U159), and to reset latches U88 and U129 so that the INHIBIT on the shift register is removed and the shift registers are put into "load" mode.

c) To clear the shift registers.

d) To clear the data buffer, U177 (explained later).

e) To clear the "clock-suppressor", U181 and U182 (explained later).

Recall that the data stream looks as follows:

SYNC WORD	CYLAD	HSAD	Data word # 0		Last data word	CRWD	6 words of ECC
is 100376_8 for valid ECC field and 100377_8 otherwise					# 127		

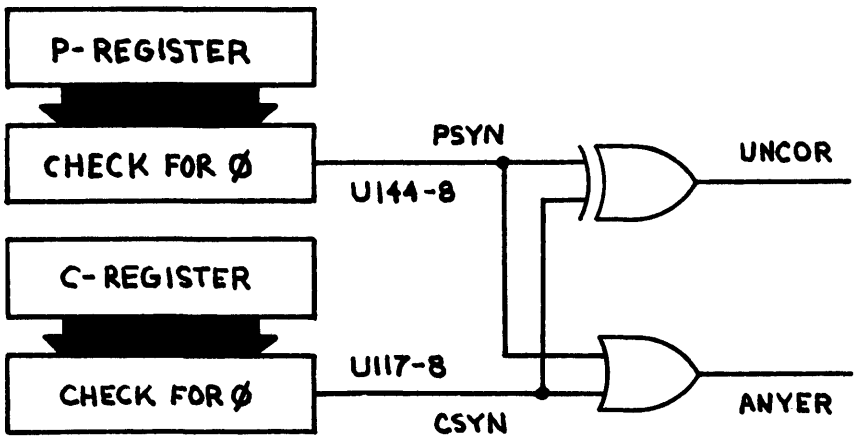
The last valid bit of "data" to be encoded by the ECC hardware during a WRITE operation is the last bit of the CRC word. Consequently after clocking in the last CRC bit, we must put the shift registers in "shift" mode. For this to happen, a firmware ECC command is executed during the transfer of the last data word (# 127). It is called ESC or "encoder sync control." Upon strobing this command into the ECICW latch (U108), the corresponding effect is the removal of the reset from the end-of-word counter (U159), and the initiation of the count of two EOW's (that of the last data word and that of the CRC word). Upon decoding this count, a latch (U88) is set so as to put the shift registers in shift mode, and the ensuing clock pulses will shift out six words of valid ECC information. This completes the description of the WRITE and the ENCODER's operation.

2.2 READ 1 SECTOR OPERATION

This is initiated by issuing a firmware command called RECC, which is interpreted by the ECICW as *READ with ECC*. The effect of this command is the same as that of the WECC command except that the multiplexer is selected in such a manner as to have the shift registers configured as a DECODER.

Again, analagous to the write operation, we must be able to control the mode of operation of the shift registers; however, in this case we continue to clock the registers in "load" mode only, being careful to INHIBIT clocking as soon as the last bit of the last ECC word has been clocked into the registers. To do this, a firmware ECC command is executed during the transfer of the

CRC word. It is called DSC or "decoder sync control." Upon validation of this command in the ECICW, the corresponding effect consists of the removal of the reset from the EOW counter and the initiation of the count of seven EOW's: that of the CRC word and each of the six ECC words. Upon decoding this count, a latch (U129) is set so as to INHIBIT the shift registers from clocking any further. The contents of the shift registers are examined in hardware by the check-for-0 logic, and the firmware examines two ground true flags (UNCOR and ANYER) to determine the integrity of the data transfer as follows:



If $\overline{\text{UNCOR}}$ is true, then an uncorrectable data error is reported. If $\overline{\text{ANYER}}$ is true, then a "possibly correctable data error" is reported. Otherwise, there was no error. This completes the description of the READ and the DECODER's error-detection process.

2.3 ERROR CORRECTION

Having detected a possibly correctable data error, the controller awaits a command from the corresponding CPU interface. In the case that it receives a RQSYN command (which is a request to find information required to correct the error), the controller now invokes the correction algorithm by calling the firmware subroutine RQSYN. Notice that in following read data operation we still have retained the contents of the shift registers, since it is these that contain the residue information required to find the error-patterns and the displacement.

The process consists of three parts, and each is described as follows:

2.3.1 BURST POSITIONING

This consists of positioning the error pattern in the lower leftmost 32 bits of the C-register, and is accomplished by executing these initial commands:

CLKHH — which takes the clock high and clears the data buffer (explained later), since we perform all the shifting with 0-input.

CLKHI — which insures that the clock is high while removing the INHIBIT from the registers and putting them in load mode.

At this point a hardware flag is checked to see if the burst is already positioned. If so, we go to seciton 2.3.2; otherwise we must shift the C-register until the burst is positioned or the shift-bound (54 shifts) expires. In order to shift the C-register exclusively, the command FRPSH (freeze P shift) is initially executed outside the burst positioning loop, which applies the INHIBIT on the P-register while maintaining the clock high. Through the use of a pair of

firmware instructions (namely CCLKH and CCLKL) the C-register clock is taken successively high and low to enable shifting with feedback, at each step adding an appropriate constant modulo to a displacement register until the burst is positioned or the shift-bound expires. If the shift-bound expires before retrieving the pattern, the error is uncorrectable.

2.3.2 MATCHING THE POSITIONED BURST

This consists of shifting the contents of the P-register with 0-input until its contents match those of the C-register, or until the shift-bound of the P-register (43 shifts) expires. The matching process is performed in IC comparator types 8130 and 8160 (U134, U74, U45, U174, and U164). The process is entirely analogous to burst positioning, using the analogous firmware instructions named PCLKH and PCLKL. If a match is not found, we return to section 2.3.1

2.3.3 ADJUSTING THE PATTERN TO WORD BOUNDARIES

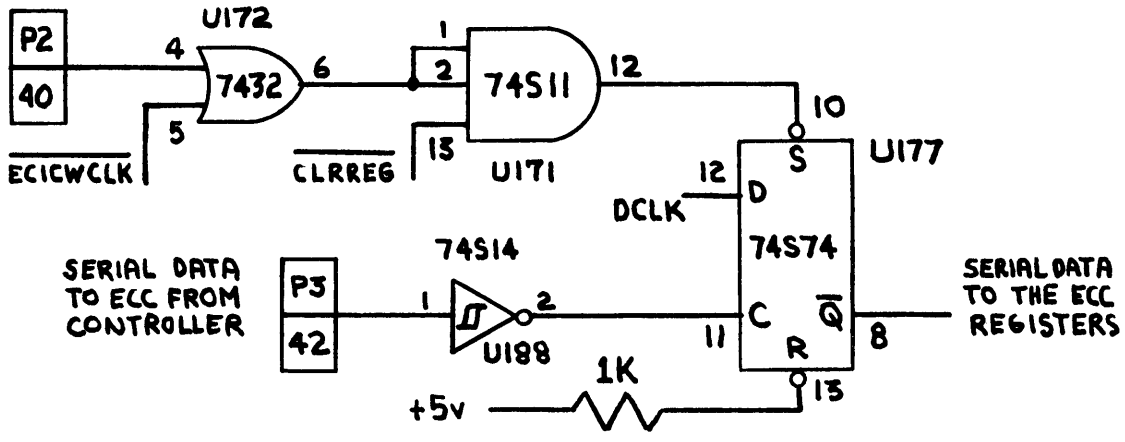
The displacements from the individual loops (previous two parts) are added together and reduced modulo a constant. The lower four bits are masked out and the scratch register shifted four bits to the right, thus performing a division by 16 so as to obtain the word displacement and bit-within-word displacement. This pattern is obtained from the shift registers via the MIO bus and is placed into two scratch registers; a third register is used along with the first two to contain three words of error pattern. The 32 bits are then left shifted in the three registers to adjust the patterns to word boundaries.

The patterns are retrieved from the shift registers onto the MIO bus via the 8123 quad two-input multiplexer IC's (U107, U97, U87, and U77). See figure 2.

2.4 HARDWARE

2.4.1 DATA BUFFER

The time interval between two successive bits of the data stream is only 133 nanoseconds; the propagation delay time for a data bit put out by the device controller before it reaches the ECC board, combined with the propagation delay through the ECC routing logic becomes prohibitive. Thus, it becomes necessary to buffer the data bit as soon as it enters the ECC board, synchronize it with the data clock, and then send it to the shift registers. The buffering is done with the following hardware:



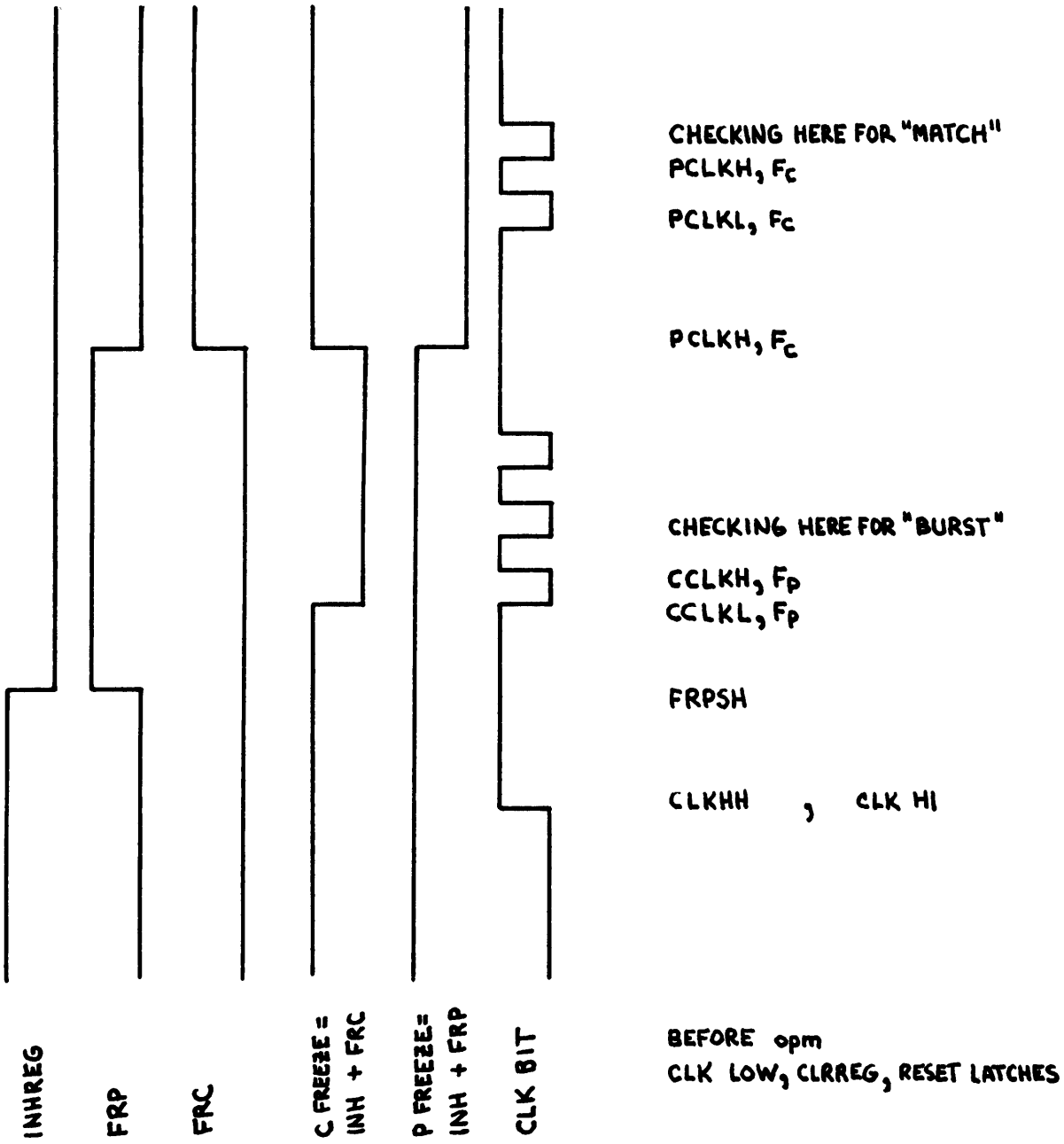


Figure 2. Error Correction Timing Diagram

This scheme has two effects:

1) The propagation delay due to the controller's routing logic is now eliminated, and consequently the delay that is due solely to the ECC logic is well within the bound of 133 ns.

2) When the last valid data bit (i.e., CRCLSB) comes out of the device controller, it is clocked into the data buffer, and is written onto the disc (it comes from the data FMTR/SPRTR); the ECC shift registers then clock in the second to the last CRC bit. An extra clock pulse is subsequently required to clock out the last CRC bit from the data buffer to the ECC registers. In so doing, an illegal bit of data gets written onto the disc occupying the MSB position of the first ECC word. This has the following repercussions:

   (i) In order to provide the extra clock pulse, the ENECC SHIFT latch must be set after a one-bit delay. This is an ENCODER related situation.

   (ii) On readback, we must suppress the clock pulse corresponding to the phony bit written in the ECC field. This situation is DECODER related.

2.4.2 CLOCK SUPPRESSOR

For ENCODER operations, the ECC hardware and the FMTR/SPRTR lag behind the device controller by one bit time. Thus all such control signals need to be delayed by one bit time. (Note: The device controller is accepting data from the CPU in "real time" — i.e., without delay.)

For READ operations, the device controller buffers the data coming from the FMTR/SPRTR for one bit time and then the ECC hardware again buffers it for one bit time. Nevertheless, since the ECC is synchronized with the device controller, the net delay with respect to the INHIBIT ECCCLK signal is only one bit time. The ECC, however, lags the FMTR/SPRTR in actual data bits by two bit times. This has to be taken into account in order to suppress the exact clock pulse corresponding to the phony bit as shown in the READ/WRITE timing diagram.

The clock suppressor hardware is on the following page:

2.4.3 TIMING OF READ AND WRITE OPERATIONS

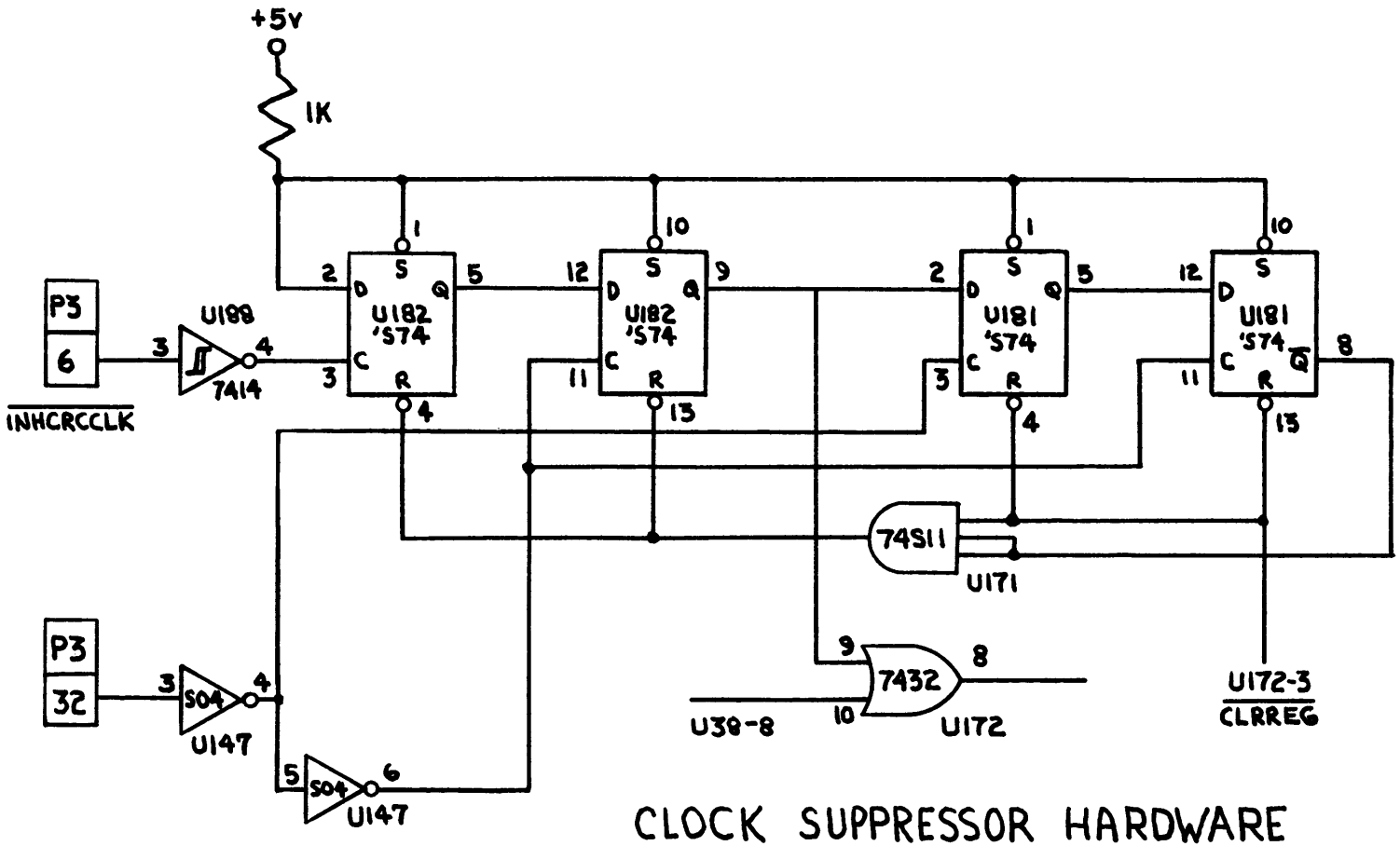
The timing sequence for WRITE and READ operations (see figure 3) is as follows.

WRITE operations:

(A1): SERDES → (puts out) bit 1
ECCSR (shift register) ← (accepts) dummy "0"
FMTR (formatter or data separator) ← bit 0
and ECCBUF (one-bit data buffer) ← bit 0

(A2): SERDES → bit 2
ECCSR ← bit 0
FMTR, ECCBUF ← bit 1

(A3): SERDES → bit 3
ECCSR ← bit 1
FMTR, ECCBUF ← bit 2



CLOCK SUPPRESSOR HARDWARE

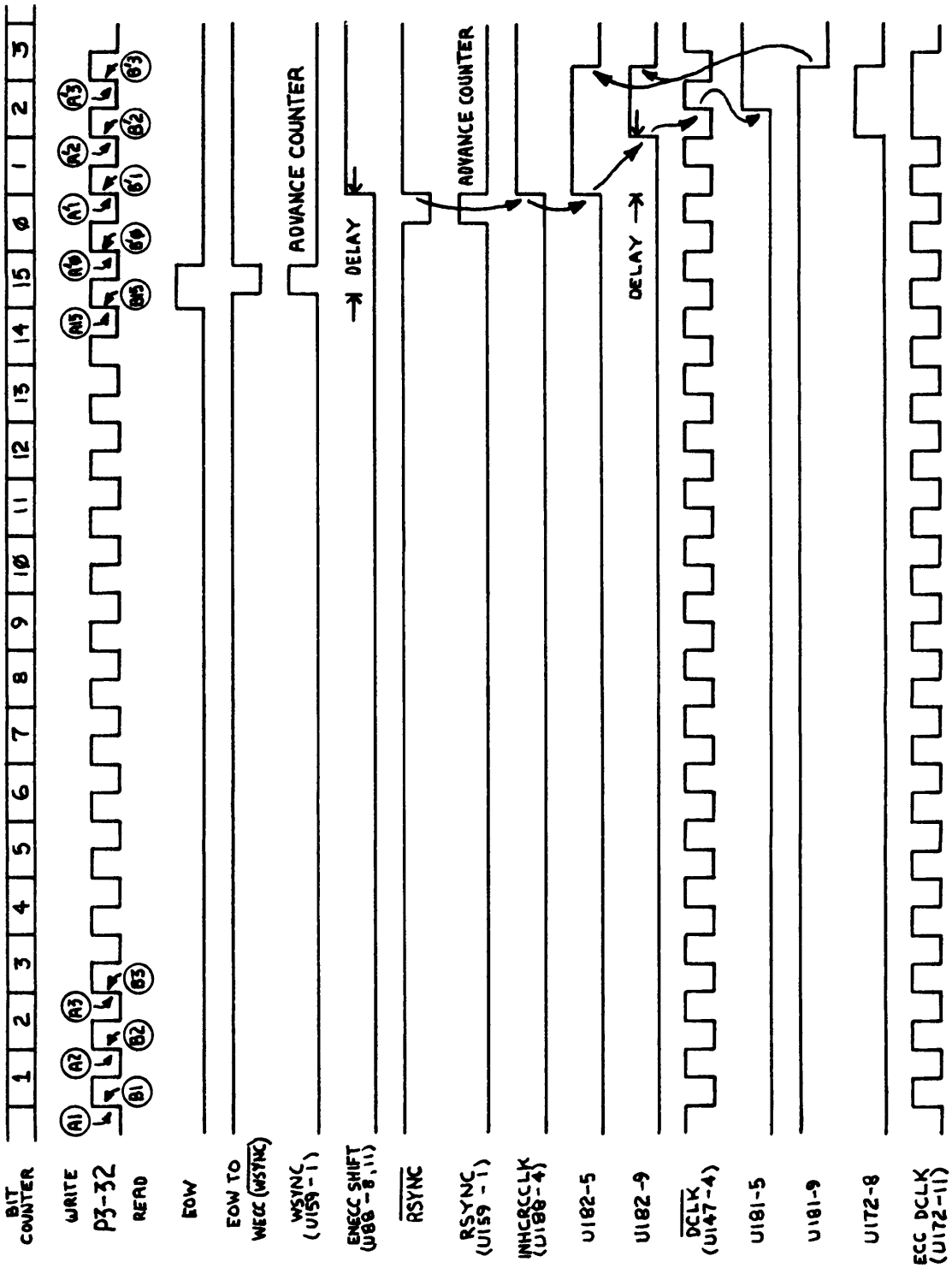


Figure 3. Timing Sequence for READ and WRITE Operations

(A15): SERDES → bit 15
ECCSR ← bit 13
FMTR, ECCBUF ← bit 14

(A'0): SERDES → bit 0
ECCSR ← bit 14
FMTR, ECCBUF ← bit 15

(A'1): SERDES → bit 1
ECCSR ← bit 15
FMTR, ECCBUF ← bit 0

Thus, if bit 15 was CRCLSB, then bit 0 here is the phony ECC MSB that gets unavoidably written and must be ignored on READ by suppressing the corresponding positive edge of the DCLK seen by ECC shift registers.

READ operations:

(B1): FMTR → bit 0
SERDES, ECCBUF ← dummy 0
ECCSR ← dummy 0

(B2): FMTR → bit 1
SERDES, ECCBUF ← bit 0
ECCSR ← dummy 0

(B3): FMTR → bit 2
SERDES, ECCBUF ← bit 1
ECCSR ← bit 0

(B15): FMTR → bit 14
SERDES, ECCBUF ← bit 13
ECCSR ← bit 12

(B'0): FMTR → bit 15
SERDES, ECCBUF ← bit 14
ECCSR ← bit 13

(B'1): FMTR → bit 0
SERDES, ECCBUF ← bit 15
ECCSR ← bit 14

(B'2): FMTR → bit 1
SERDES, ECCBUF ← bit 15
ECCSR ← bit 14

(B'3): FMTR → bit 2
SERDES, ECCBUF ← bit 1
ECCSR ← bit 0

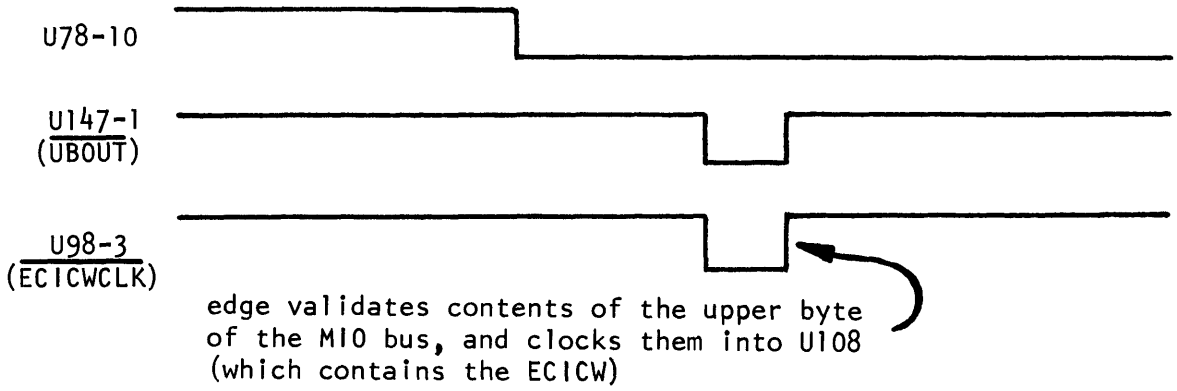
Thus, if bit 15 was CRCLSB, then bit 0 here is the phony ECC MSB that should not be clocked into the ECC shift registers, and the positive edge of clock pulse corresponding to it (shown in figure 3 at B'3) should be suppressed. This is accomplished by the "clock suppressor" made from U181, U183, U147, and U171.

3.0 EXPANDED DESCRIPTION

3.1 FIRMWARE COMMANDS

Presented below is a detailed description of the ECC hardware in conjunction with the firmware commands executed.

Whenever the ECICW is addressed in either a DO or DI (data out or data input) instruction, the address decoder (U78) puts out a low level on U78-10. This, combined with $\overline{\text{UBOUT}}$ (the signal for upper byte instructions on the MIO bus) provides the pulse $\overline{\text{ECICWCLK}}$ at U98-3 as follows:

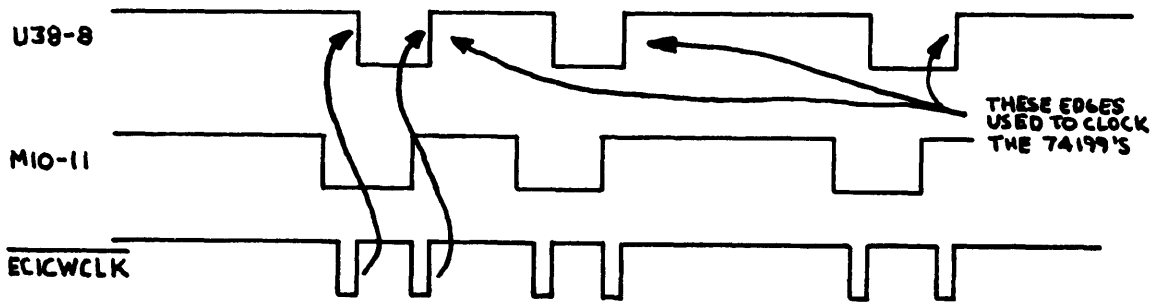


The ECC firmware commands are:

OCTAL	ECC Firmware Command	MIO Bus Contents							
		Bit 15	14	13	12	11	10	9	8
26	WECC	0/H	0/H	0/H	1/L	0/H	1/L	1/L	0/H
0	ESC	0/H	0/H	0/H	0/H	0/H	0/H	0/H	0/H
226	RECC	1/L	0/H	0/H	1/L	0/H	1/L	1/L	0/H
200	DSC	1/L	0/H	0/H	0/H	0/H	0/H	0/H	0/H
211	CLKHH	1/L	0/H	0/H	0/H	1/L	0/H	0/H	1/L
230	CLKHI	1/L	0/H	0/H	1/L	1/L	0/H	0/H	0/H
312	FRPSH	1/L	1/L	0/H	0/H	1/L	0/H	1/L	0/H
300	CCLKL	1/L	1/L	0/H	0/H	0/H	0/H	0/H	0/H
310	CCLKH	1/L	1/L	0/H	0/H	1/L	0/H	0/H	0/H
240	PCLKL	1/L	0/H	1/L	0/H	0/H	0/H	0/H	0/H
250	PCLKH	1/L	0/H	1/L	0/H	1/L	0/H	0/H	0/H

Since the MIO bus is ground true, a logical "0" will be a high level and a logical "1" will be a low level. It should also be pointed out what the various MIO bits 8 through 15 signify to the ECC assembly when validated into the ECICW by $\overline{\text{ECICWCLK}}$.

MIO Bus Bit Number	Description
15	If 0/H is on the input U108-13, the $\overline{Q}$ output U108-14 goes low, which helps to select the A-inputs on the mux U169 to provide the ENCODER configuration. If 1/L is on U108-13, we obtain a high at U108-14 which helps to select the B-inputs on U169, thus providing the DECODER configuration.
14	When 0/H is on the input U108-12, the $\overline{Q}$ output U108-11 goes low; when 1/L is on the input, this output goes high, enabling in this case to INHIBIT the clock on the P-register (this signal is called F_P or "freeze P).
13	When 0/H is on the input U108-4, the $\overline{Q}$ output U108-3 goes low; when 1/L is on the input, this output goes high, enabling in this case to INHIBIT the clock on the C-register (this signal is called F_C or "freeze C").
12	When 0/H is on the input U108-5, the Q output U108-7 goes high; the $\overline{Q}$ output U108-6 goes low, thus removing the reset from the EOW Counter U159 and enabling it to count. When 1/L on the input U108-5, the Q output U108-7 goes low, which helps to reset the ENECCSHIFT/LOAD latch U88 and also the INHREG latch U129; the $\overline{Q}$ output U108-6 goes high and resets the EOW counter U159 (the $\overline{Q}$ output is called "$\overline{SC}$" or "$\overline{\text{sync control}}$").
11	When 0/H is on the input U38-12, the Q output U38-8 goes low; when 1/L is on the input U38-12, the Q output U38-8 goes high. Successive applications of highs and lows enables us to provide "clock" pulses to the shift registers for shifting under firmware control (this signal is called "CLK" or clock).



10	When 1/L is at the inputs U172-2 and U98-4-12, the outputs are pulses at U172-3, U98-6-11, which are used to clear the data buffer, the clock suppressor, and the P and C registers (this signal is called "$\overline{\text{CLRREG}}$" or "$\overline{\text{clear the registers}}$").
9	This line is not used and as such has a "don't care" level.
8	When 1/L is at the input U172-4, its effect is to clear the one-bit data buffer U177 to enable the shifting with feedback of the P and C registers without input (this signal is called "$\overline{\text{CLRDATABUFFER}}$").

3.2 WRITE OPERATIONS

Let us consider what happens for write operations such as WRITE and INITIALIZE.

Initially the WECC command is put out on the upper byte of the MIO bus via the instruction D0: ECCICW ← WECC, U and the bus contents are validated by $\overline{\text{ECICWCLK}}$.

The effect of executing this instruction is as follows. U108-14 goes low so that the A-inputs are selected at mux U169 (i.e., the registers are in ENCODER configuration); also U139-8 is held high and thus prevents the INHIBIT-REG latch from being set. U108-15 goes high, thus removing the reset from U149-13 (whose function is to delay the count of two EOW's by one bit time).

U108-11 (F_P) goes low thus removing the inhibit from P-register.

U108-3 (F_C) goes low thus removing the inhibit from C-register.

U108-6 (SC) goes high thus resetting the EOW counter U159.

U108-7 (SC) goes low thus resetting the INHREG latch U129 and resetting the ENSHIFT/LOAD latch U88 (puts the shift registers into load mode). U38-8 goes low, thus allowing the data clock (as opposed to the firmware-supplied clock) to be passed to the shift registers via U172-11 and U118-3-8.

U172-3 and U98-6-11 put out a negative pulse which clears the one-bit data buffer (U177-8), the clock suppressor (U181), and the P and C registers.

After this command we execute the instruction DI BUF3 ← ESYNC, L which puts a logical "0" in the LSB of the sync word. See U28-1-2-3 and MIO 0.

During the transfer of the last data word we execute the instruction DO ECICW ← ESC, U and its effect is as follows:

U108-14 remains low for the ENCODER configuration.

U108-15 remains high.

U108-11 remains low.

U108-3 remains low.

U108-6 goes low, thus removing the reset from U159-2-3 and allowing it to count subsequent EOW's.

U108-7 goes high, thus removing the reset from the ENSHIFT/LOAD latch U88.

Now after counting two EOW pulses, U159-8 goes high and gets clocked onto U149-12 at the next positive edge of DDCLK; the output U149-9 goes high, U88-3 goes low, and the latch U88 gets set. Consequently, U88-8-11 both go high, putting the shift-registers into the shift mode; corresponding clocks applied to the shift-registers will cause the ECC parity bits to be written onto the disc. See figure 4.

Note that for all write operations U108-14 is low and U108-15 is high in order to maintain the ENCODER configuration.

3.3 READ OPERATIONS

Now let us consider read operations such as READ and VERIFY (in VERIFY, no data is passed to the CPU, yet the ECC hardware treats it just as if it were a READ command).

Throughout READ and VERIFY data operations in the controller the ECC board is maintained in the DECODER configuration; thus all ECC commands related to these operations

will maintain U108-14 high and U108-15 low. U108-15 being low prevents the ENSHIFT/ LOAD latch U88 from being set; thus the shift-registers will remain in the load mode throughout these operations.

Initially the RECC command is put out by executing a DO ECICW ← RECC, U instruction.

U108-3-11 both go low, so as to remove their individual INHIBIT's from the C and P registers, respectively.

U108-6 goes high and resets the U159 EOW counter as in WECC.

U108-7 goes low and resets the latches as in WECC.

U38-8 goes low to allow the data clock from P3-32 to pass through as in WECC.

U172-3 and U98-6-11 all issue a negative clear pulse as in WECC.

The next command executed is DO DSYNC ← REG0, L. The purpose of this instruction is to decode the LSB of the SYNC word in U38 to determine whether the sector being transferred or verified has valid data in the ECC field. See U38-2-3-6.

During the transfer of the CRC word, we execute the instruction DO ECICW ← DS, U and its effect is as follows.

Leaving everything else unchanged, U108-6 goes low, thus removing the reset from U159-2-3 and allowing it to count subsequent EOW's. U108-7 goes high thus removing the reset from the INHREG latch U129 and its one-bit delay buffer U149-2-3-5. Note that since U108-14 is high for read operations, it enables U139-8 to decode the count of seven EOW's; since U108-15 is low it disables the latch U88 from being set.

After counting seven EOW's U139-8 goes low; after the next data clock positive edge U149-5 goes low and sets the latch U129-8. The shift-registers are now inhibited and the operation is completed. See figure 5.

This completes the description of all data operations, and should be understood in conjunction with the timing diagram in figure 3.

3.4 ERROR RECOVERY

3.4.1 DETECTION

At the end of the data transfer or verification, the following instructions are executed to determine the integrity of the operation:

CC = UNCOR, RS	/Was there an uncorrectable data error? Check flag P2-5.
BR = UDTER	/Yes, set up appropriate status and interrupt.
CC = ANYER, RS	/No, was there a (possibly) correctable data error? Check flag P2-21.
BR: CDTER	/Yes, set up appropriate status and interrupt.
RT: 0	/No data error was detected.

Flag $\overline{\text{ANYER}}$ at P2-21 will be low if any data error (uncorrectable or possibly correctable) was detected at the end of the operation.

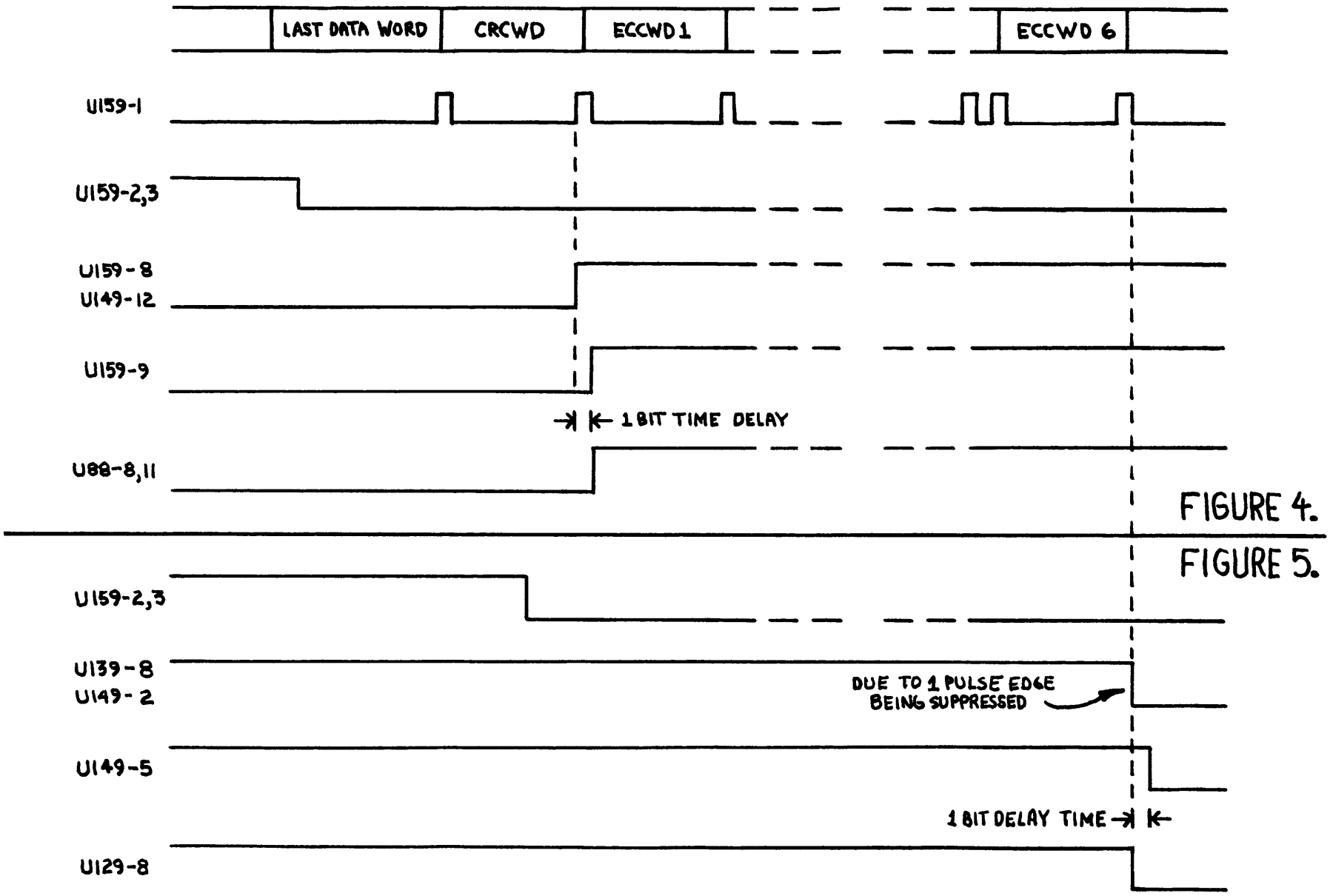


FIGURE 4.

FIGURE 5.

3.4.2 CORRECTION

Error correction is invoked by a branch to the RQSYN routine in the ROM. Again note, U108-14 is high throughout this routine to maintain the DECODER configuration.

A. Burst Positioning

Initially three instructions are executed — they are:

1) DO ECICW ← CLKHH, U

   U38-8 is taken high, so that the clock inputs on the shift-registers are high.

   U172-6 outputs a negative pulse to clear the data buffer so that the registers may be clocked with "0" input only.

2) DO ECICW ← CLKHI, U

   While the clock input to the registers is held high by maintaining U38-8 high, U108-7 goes low to reset latches U88 and U129 so as to permit the subsequent clocking of the shift-registes in load mode.

3) DO ECICW ← FRPSH, U

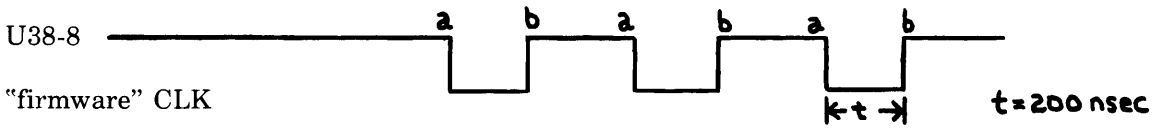
   While maintaining U38-8 high (line the clock inputs on the shift registers), U108-11 (F_P) goes high while U108-3 (F_C) goes low, thus relieving the inhibit on the C-register and applying the inhibit to the P-register to enable selective and exclusive clocking of the C-register.

Following this initial set-up, a set of instructions are conditionally executed as below:

```
C   CC = BURST, RS
    BR: PLOOP

    DO ECICW ← CCLKL, U
    DO ECICW ← CCLKH, U
```

This pair of instructions, when executed, provides the clocking mechanism required to clock the enabled (uninhibited) shift-register



After each "clocking" of the C-register the condition C is checked again, and if the flag called "BURST" at U119-9 goes low, we skip this set of instructions and branch to the next phase; otherwise, we continue until the shift bound (of 53) expires (at which point we report "uncorrectable error" status and exit from the RQSYN routine).

B. Burst Matching

The next phase consists of executing an initial instruction

DO ECICW ← PCLKH, U

which makes U108-11 (F_P) go low, thus removing the INHIBIT from the P-register; also U108-3 (F_C) goes high, thus applying the INHIBIT to the C-register.

Then a pair of similar clocking instructions are conditionally executed as follows:

```
P   CC = MATCH, RS
    BR:  GTPAT

    DO ECICW ← PCLKL, U
    DO ECICW ← PCLKH, U
```

which accomplish the same function as CCLKL and CCLKH on the P-register (which is not now inhibited).

After each "clocking" of the P-register the condition P is checked again, and if the flag called "MATCH" (at U119-13) goes low, we skip this set of instructions and branch to the next phase to obtain the error pattern; otherwise, we continue until the P-register shift bound (43) expires, at which point we return to the previous phase (Section A) again.

The flag "BURST" can be traced back to the shift registers, and employs some of the "check-for-0" circuitry. It is ground true and goes low whenever the Q output of U106-4 is high and all the Q outputs of U176, U146, and U126-4-6-8-10-15 are low.

The flag "MATCH" can also be traced back to the shift registers and employs the comparators U134, U74, U45, U174, and U164. It is also a ground true flag and goes low only when all the corresponding outputs of the P-register and the C-register match. Refer again to figure 2 for a general idea.

C. Pattern Retrieval

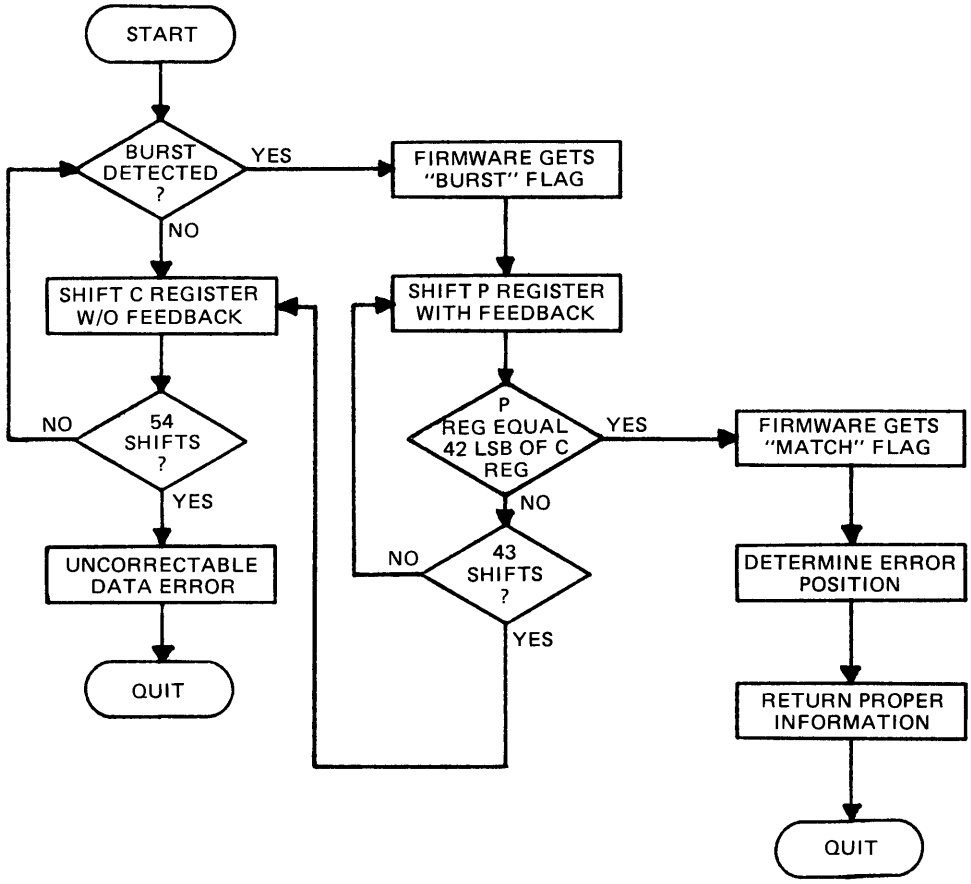
In this phase the main instructions executed are:

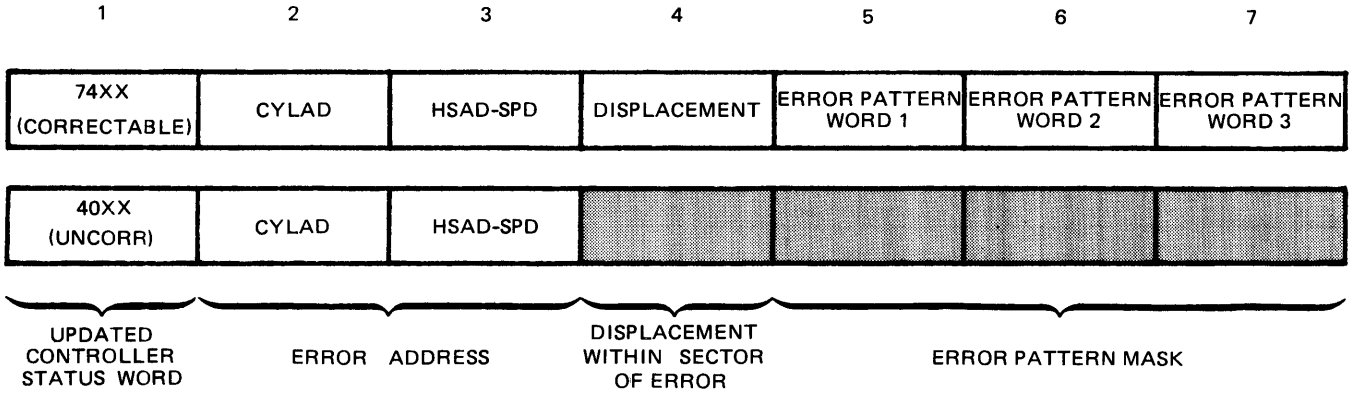
```
DI XREG ← WORD 1
DI YREG ← WORD 2
```

The address decoder U78 decodes the external addresses (WORD 1 and WORD 2) and enables the three-state multiplexers U107, U97, U87, and U77, selecting them successively so that the contents at their I_0 inputs are first put on the bus (then those at the I_1 inputs are put out).

D. Final Correction

This is the last phase of the entire operation and does not involve the ECC hardware at all. The patterns are now adjusted to word boundaries under firmware control and passed to the CPU interface for subsequent XORing with the original data (thus accomplishing the final error correction).





In actuality,

BIT DISP = [1591 X (# C SHIFTS) + 689 X (# P SHIFTS)] MOD 2279

Because there are 2208 bits in a sector if the sync field is excluded, 71 bits of the zero sync field must be shifted in to accommodate the 2279 bit modular arithmetic. Note that these 71 zero bits do not affect the initially cleared state of the registers until the actual data (beginning with the sync word) is shifted through. However, the required bit displacement calculation surpasses the capabilities of the 16 bit arithmetic logic, so the firmware employs a modified algorithm to keep intermediate calculations within the limits of the microprocessor logic.

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60024
13037-68024

DATE CODE : E-1650

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C1	0160-2055	CAP .01UF-20+80%
C10	0160-2055	CAP .01UF-20+80%
C11	0160-2055	CAP .01UF-20+80%
C12	0160-2055	CAP .01UF-20+80%
C13	0160-2055	CAP .01UF-20+80%
C14	0160-2055	CAP .01UF-20+80%
C15	0160-2055	CAP .01UF-20+80%
C16	0160-2055	CAP .01UF-20+80%
C17	0160-2055	CAP .01UF-20+80%
C18	0160-2055	CAP .01UF-20+80%
C19	0160-2055	CAP .01UF-20+80%
C2	0160-2055	CAP .01UF-20+80%
C20	0160-2055	CAP .01UF-20+80%
C21	0160-2055	CAP .01UF-20+80%
C22	0160-2055	CAP .01UF-20+80%
C23	0160-2055	CAP .01UF-20+80%
C24	0160-2055	CAP .01UF-20+80%
C25	0160-2055	CAP .01UF-20+80%
C26	0160-2055	CAP .01UF-20+80%
C27	0160-2055	CAP .01UF-20+80%
C28	0160-2055	CAP .01UF-20+80%
C29	0160-2055	CAP .01UF-20+80%
C3	0160-2055	CAP .01UF-20+80%
C30	0160-2055	CAP .01UF-20+80%
C31	0180-0374	CAP 10UF 10%
C4	0160-2055	CAP .01UF-20+80%
C5	0160-2055	CAP .01UF-20+80%
C6	0160-2055	CAP .01UF-20+80%
C7	0160-2055	CAP .01UF-20+80%
C8	0160-2055	CAP .01UF-20+80%
C9	0160-2055	CAP .01UF-20+80%
E1	0360-0294	TERM-SOLDER STUD
E2	0360-0294	TERM-SOLDER STUD
E3	0360-0294	TERM-SOLDER STUD
E4	0360-0294	TERM-SOLDER STUD
E5	0360-0294	TERM-SOLDER STUD
MP10	0624-0077	SCR TAP 4-40X.31
MP11	5020-7318	SPACER
MP11	5040-6009	EXTRACTOR PC
MP12	1480-0116	PIN GRV .062X.25
MP13	7120-5738	INFO LABEL
MP14	5020-7318	SPACER
MP9	5040-6058	BRACE-PC BOARD
R10	0757-0280	RES 1K 1%.125
R11	0757-0280	RES 1K 1%.125
R5	0757-0280	RES 1K 1%.125
R6	0757-0280	RES 1K 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60024
13037-68024

DATE CODE : E-1650

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R7	0757-0280	RES 1K 1%.125
R8	0757-0280	RES 1K 1%.125
R9	0757-0280	RES 1K 1%.125
U101	1820-0755	IC HP147A
U102	13037-80141	IC ROM
U102	1816-1293	IC-MEMORY
U103	1820-0328	IC SN7402N
U104	1820-0070	IC SN7430N
U106	1820-0726	IC N74199N
U107	1820-1294	IC DM8123N
U108	1820-1195	IC SN74LS175N
U111	13037-80129	IC ROM
U111	1816-1281	IC-MEMORY
U112	13037-80140	IC ROM
U112	1816-1292	IC-MEMORY
U113	1820-0726	IC N74199N
U116	1820-0683	IC SN74S04N
U117	1820-0070	IC SN7430N
U118	1820-0661	IC SN7432N
U119	1820-0072	IC SN7450N
U121	13037-80128	IC ROM
U121	1816-1280	IC-MEMORY
U122	13037-80139	IC ROM
U122	1816-1291	IC-MEMORY
U123	1820-0282	IC SN7486N
U126	1820-0726	IC N74199N
U128	1820-0683	IC SN74S04N
U129	1820-0054	IC SN7400N
U13	1820-0328	IC SN7402N
U131	13037-80127	IC ROM
U131	1816-1279	IC-MEMORY
U132	13037-80138	IC ROM
U132	1816-1290	IC-MEMORY
U133	1820-0328	IC SN7402N
U134	1820-1293	IC DM8130N
U135	1820-0328	IC SN7402N
U136	1820-0282	IC SN7486N
U137	1820-0070	IC SN7430N
U138	1820-0683	IC SN74S04N
U139	1820-0069	IC SN7420N
U141	13037-80126	IC ROM
U141	1816-1278	IC-MEMORY
U142	13037-80137	IC ROM
U142	1816-1289	IC-MEMORY
U143	1820-0726	IC N74199N
U144	1820-0070	IC SN7430N
U146	1820-0726	IC N74199N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60024
13037-68024

DATE CODE : E-1650

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U147	1820-0683	IC SN74S04N
U149	1820-0693	IC SN74S74N
U15	1820-0070	IC SN7430N
U151	13037-80125	IC ROM
U151	1816-1277	IC-MEMORY
U152	13037-80136	IC ROM
U152	1816-1288	IC-MEMORY
U153	1820-0282	IC SN7486N
U156	1820-0282	IC SN7486N
U157	1820-0282	IC SN7486N
U158	1820-0683	IC SN74S04N
U159	1820-0099	IC SN7493N
U16	1820-0328	IC SN7402N
U161	13037-80124	IC ROM
U161	1816-1161	IC-MEMORY
U163	1820-0328	IC SN7402N
U166	1820-0328	IC SN7402N
U167	1820-0070	IC SN7430N
U168	1820-0694	IC SN74S86N
U169	1820-1077	IC SN74S157N
U171	1820-0686	IC SN74S11N
U172	1820-0661	IC SN7432N
U173	1820-0726	IC N74199N
U174	1820-1131	IC DM8160N
U176	1820-0726	IC N74199N
U177	1820-0693	IC SN74S74N
U179	1820-0175	IC SN7405N
U181	1820-0693	IC SN74S74N
U182	1820-0693	IC SN74S74N
U183	1820-0282	IC SN7486N
U184	1820-0282	IC SN7486N
U186	1820-0282	IC SN7486N
U187	1820-0282	IC SN7486N
U188	1820-1053	IC SN7414N
U23	1820-0726	IC N74199N
U26	1820-0726	IC N74199N
U28	1820-1121	IC 8093N
U31	13037-80135	IC ROM
U31	1816-1287	IC-MEMORY
U33	1820-0282	IC SN7486N
U34	1820-0282	IC SN7486N
U36	1820-0282	IC SN7486N
U37	1820-0282	IC SN7486N
U38	1820-0077	IC SN7474N
U41	13037-80134	IC ROM
U41	1816-1286	IC-MEMORY
U42	13037-80147	IC ROM

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60024
13037-68024

DATE CODE : E-1650

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U42	1816-1312	IC-MEMORY
U43	1820-0070	IC SN7430N
U44	1820-0328	IC SN7402N
U45	1820-1293	IC DM8130N
U46	1820-0328	IC SN7402N
U48	1820-0661	IC SN7432N
U51	13037-80133	IC ROM
U51	1816-1285	IC-MEMORY
U52	13037-80146	IC ROM
U52	1816-1298	IC-MEMORY
U53	1820-0726	IC N74199N
U56	1820-0726	IC N74199N
U58	1820-0683	IC SN74S04N
U61	13037-80132	IC ROM
U61	1816-1284	IC-MEMORY
U62	13037-80145	IC ROM
U62	1816-1297	IC-MEMORY
U63	1820-0282	IC SN7486N
U64	1820-0282	IC SN7486N
U65	1820-0328	IC SN7402N
U66	1820-0282	IC SN7486N
U67	1820-0282	IC SN7486N
U68	1820-0511	IC SN7408N
U71	13037-80131	IC ROM
U71	1816-1283	IC-MEMORY
U72	13037-80144	IC ROM
U72	1816-1296	IC-MEMORY
U73	1820-0328	IC SN7402N
U74	1820-1293	IC DM8130N
U76	1820-0726	IC N74199N
U77	1820-1294	IC DM8123N
U78	1820-0608	IC MC4006P
U81	13037-80130	IC ROM
U81	1816-1282	IC-MEMORY
U82	13037-80143	IC ROM
U82	1816-1295	IC-MEMORY
U83	1820-0726	IC N74199N
U85	1820-0282	IC SN7486N
U86	1820-0282	IC SN7486N
U87	1820-1294	IC DM8123N
U88	1820-0054	IC SN7400N
U91	1820-1072	IC SN74S139N
U92	13037-80142	IC ROM
U92	1816-1294	IC-MEMORY
U93	1820-0282	IC SN7486N
U94	1820-0282	IC SN7486N
U95	1820-0070	IC SN7430N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60024
13037-68024

DATE CODE : E-1650

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U96	1820-0328	IC SN7402N
U97	1820-1294	IC DM8123N
U98	1820-0661	IC SN7432N
X102	1200-0482	SOCKET 16 DIP LO
X111	1200-0482	SOCKET 16 DIP LO
X112	1200-0482	SOCKET 16 DIP LO
X121	1200-0482	SOCKET 16 DIP LO
X122	1200-0482	SOCKET 16 DIP LO
X131	1200-0482	SOCKET 16 DIP LO
X132	1200-0482	SOCKET 16 DIP LO
X141	1200-0482	SOCKET 16 DIP LO
X142	1200-0482	SOCKET 16 DIP LO
X151	1200-0482	SOCKET 16 DIP LO
X152	1200-0482	SOCKET 16 DIP LO
X161	1200-0482	SOCKET 16 DIP LO
X31	1200-0482	SOCKET 16 DIP LO
X41	1200-0482	SOCKET 16 DIP LO
X42	1200-0482	SOCKET 16 DIP LO
X51	1200-0482	SOCKET 16 DIP LO
X52	1200-0482	SOCKET 16 DIP LO
X61	1200-0482	SOCKET 16 DIP LO
X62	1200-0482	SOCKET 16 DIP LO
X71	1200-0482	SOCKET 16 DIP LO
X72	1200-0482	SOCKET 16 DIP LO
X81	1200-0482	SOCKET 16 DIP LO
X82	1200-0482	SOCKET 16 DIP LO
X92	1200-0482	SOCKET 16 DIP LO

END OF MATERIAL LIST.

ENGINEERING RESPONSIBILITY																SEPIA															
0	1	2	3	4		6		8	9		11	12	14	15																	
16	17		19		21	22	23	25	29	30	32	33	38	43																	
45	46	61	63	99		99	99	99																							

SYM	REVISIONS	APPROVED	DATE
D	REVISED & REDRAWN PER CO 48-1890	AHL/KB	11-19-80
E	REVISED PER CO 48-0819	ME/RM	5-21-85

D-13037 -60024 -54

RAR 11 RAR 9 RAR 8 RAR 2 RAR 0 RAR 3 RAR 4 RAR 5 RAR 6 RAR 7

ROM 20 ROM 21 ROM 22 ROM 23 ROM 18 ROM 19 ROM 16 ROM 17 ROM 12 ROM 13 ROM 14 ROM 15 ROM 8 ROM 9 ROM 10 ROM 11 ROM 4 ROM 5 ROM 6 ROM 7 ROM 2 ROM 3

32 36 42 N.C. 46 39 31 33 23 22 24 17 47 45 43 42 4 3 10 9 41 39 37 35 11 12 13 15 8 7 6 5 26 27 24 25

74139 U91 1G 1B 1A 1Y3 1Y2 1Y1 1Y0 3 2 1 7 6 5 4

1820-0755 U101 E1 E2 +5V 12 13 14 15 16 17 18 9 8 7 6 5 4 3 2 1

ROM 1 13037-80124 U161
ROM 2 13037-80125 U151
ROM 3 13037-80126 U141
ROM 4 13037-80127 U131
ROM 5 13037-80128 U121
ROM 6 13037-80129 U111
ROM 7 13037-80130 U81
ROM 8 13037-80131 U71
ROM 9 13037-80132 U61
ROM 10 13037-80133 U51
ROM 11 13037-80134 U41
ROM 12 13037-80135 U31
ROM 13 13037-80136 U152
ROM 14 13037-80137 U142
ROM 15 13037-80138 U132
ROM 16 13037-80139 U122
ROM 17 13037-80140 U112
ROM 18 13037-80141 U102
ROM 19 13037-80142 U92
ROM 20 13037-80143 U82
ROM 21 13037-80144 U72
ROM 22 13037-80145 U62
ROM 23 13037-80146 U52
ROM 24 13037-80147 U42

+5V 31 C16-30 C1-15 10uF 01 .01

P1-1-4. J1-7.8.9.10.

P1- 12, 14, 15, 16, 17, 20, 29, 30, 42, 43, 48, 50, 54, 55.

P2-1

P3- 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 20, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 44, 45, 47, 49.

J1- 1, 2, 49, 50.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO.	MAT'L DWG. NO.	MAT'L SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

DRAWN BY	4-27-79 DATE	ECC / ROM SCHEMATIC TITLE
ENGINEER	11-19-80	HEWLETT PACKARD
RELEASE TO PROD.	11-19-80	NEXT ASSEMBLY
SUPERSEDES DWG.		FINISH SCALE

13037-60024 PART NUMBER

D-13037 -60024 -54

SHEET 1 OF 1

D-13037-60024-51

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15	
16 17 18 19 20 21 22 23 34 36 42 43	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PCO. 22.3486	JV	4/22/76

I_{NOW} 3Y of MUX

INBITSP

CLEAR REG

ENABLE SHIFT/LOAD

INHIBIT P

DATA-CLK

X_1 X_2 X_{20} X_{30} X_{150}

I_1 I_2 I_3 I_4 I_5 I_6 I_7 I_8 I_9 I_{10} I_{11} I_{12} I_{13} I_{14} I_{15} I_{16} I_{17} I_{18} I_{19} I_{20} I_{21} I_{22} I_{23} I_{24} I_{25} I_{26} I_{27} I_{28} I_{29} I_{30} I_{31}

74199 113 | 74199 83 | 74199 53 | 74199 23

8130 134 | 8130 74 | 8130 45

74199 106 | 74199 76 | 74199 56 | 74199 26

Q_G^H Q_H^H Z_3 Z_2 Z_1 Q_H^L Q_G^L

X^H X^L

ALSO CALLED BITSC

INHIBIT C

DATA-CLK

ENABLE SHIFT/LOAD

CLEAR REG

INBITSC

NOTES:

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING UNLESS OTHERWISE SPECIFIED. DIMENSIONS ARE IN INCHES. TOLERANCES .XX ± .02 .XXX ± .005

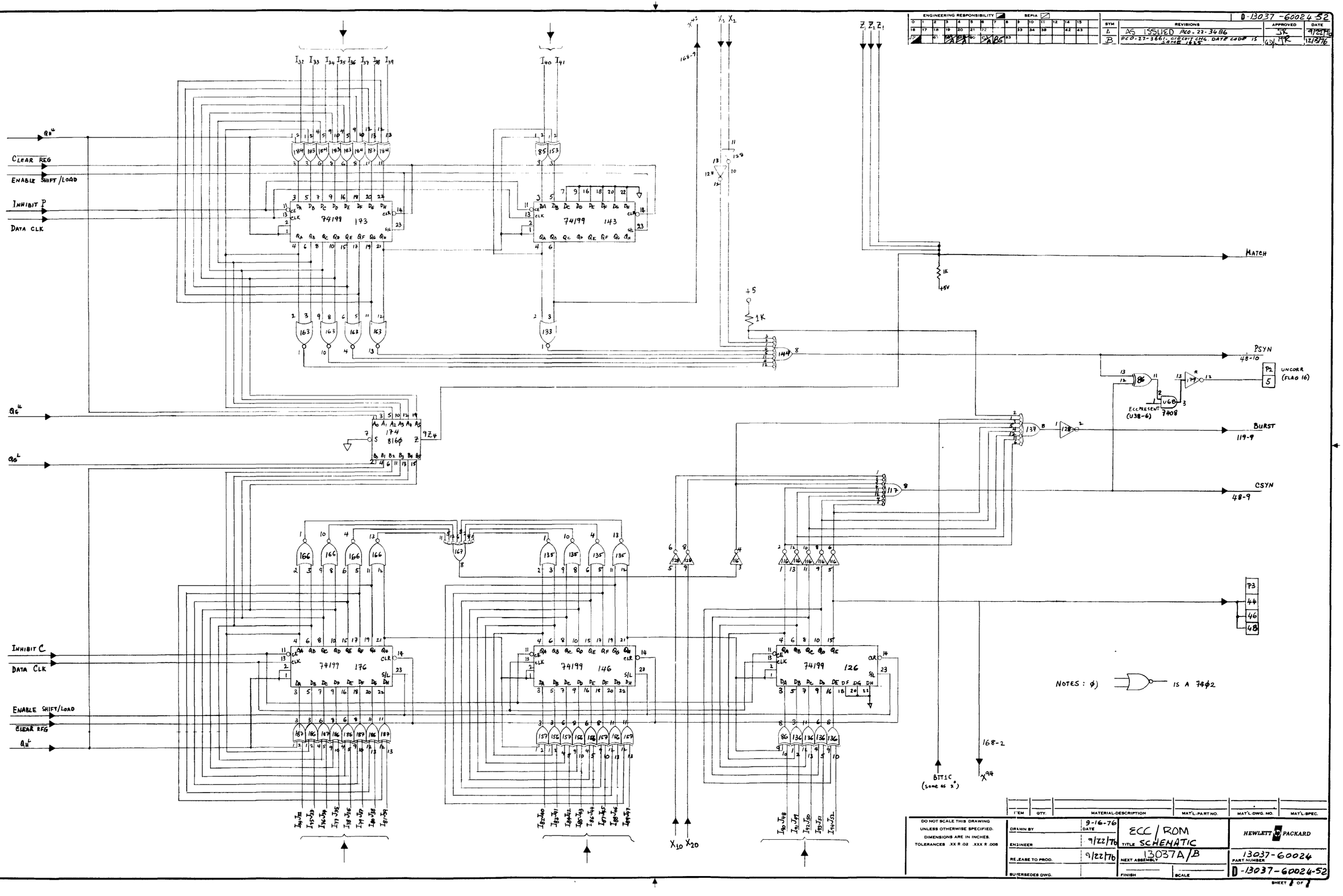
DRAWN BY	9-16-76	ECC / ROM	HEWLETT PACKARD
ENGINEER	9/22/76	TITLE SCHEMATIC	
RELEASE TO PROD.	9/22/76	13037A/B NEXT ASSEMBLY	13037-60024 PART NUMBER
SUPERSEDES DWG.		FINISH / SCALE	D-13037-60024-51

SHEET 1 OF 1

D-13037-60024-52

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15	
16 17 18 19 20 21 22 23 32 33 34 38 42 43	
LA LB LC LD LE LF LG LH LJ LK LL LM LN LP LR LS LT LU LV LW LX LY LZ MA MB MC MD ME MF MG MH MJ MK ML MM MN MP MR MS MT MU MV MW MX MY MZ NA NB NC ND NE NF NG NH NJ NK NL NM NN NP NR NS NT NU NV NW NX NY NZ PA PB PC PD PE PF PG PH PJ PK PL PM PN PP PR PS PT PU PV PW PX PY PZ QA QB QC QD QE QF QG QH QJ QK QL QM QN QP QR QS QT QU QV QW QX QY QZ RA RB RC RD RE RF RG RH RJ RK RL RM RN RP RR RS RT RU RV RW RX RY RZ SA SB SC SD SE SF SG SH SJ SK SL SM SN SP SR ST SU SV SW SX SY SZ TA TB TC TD TE TF TG TH TJ TK TL TM TN TP TR TS TT TU TV TW TX TY TZ UA UB UC UD UE UF UG UH UJ UK UL UM UN UP UR US UT UU UV UW UX UY UZ VA VB VC VD VE VF VG VH VJ VK VL VM VN VP VR VS VT VU VV VW VX VY VZ WA WB WC WD WE WF WG WH WJ WK WL WM WN WP WR WS WT WU WV WW WX WY WZ XA XB XC XD XE XF XG XH XJ XK XL XM XN XP XR XS XT XU XV XW XX XY XZ YA YB YC YD YE YF YG YH YJ YK YL YM YN YP YR YS YT YU YV YW YX YY YZ ZA ZB ZC ZD ZE ZF ZG ZH ZJ ZK ZL ZM ZN ZP ZR ZS ZT ZU ZV ZW ZX ZY ZZ	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PCO-22-3486	JK	9/22/76
B	PCO-22-3867; CIRCUIT CHG. DATE CODE 15 20 MAR 1976	MR	12/15/76



ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L PART NO.	MAT'L DWG. NO.	MAT'L SPEC.

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED.
DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY	9-16-76 DATE	ECC / ROM SCHEMATIC
ENGINEER	9/22/76	HEWLETT PACKARD
RELEASE TO PROD.	9/22/76	13037A/B NEXT ASSEMBLY
SUPERSEDES DWG.		FINISH / SCALE
		13037-60024 PART NUMBER
		D-13037-60024-52

SHEET 1 OF 7

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PCO-22-3886 PCO-22-3861-CIRCUIT ENG. DATA CODE 15 LARGE 1825	TR	9/22/76
B		TR	11/15/76
C	CORRECTED ERRORS, PC#4-0432	L.D.	4-20-77

D-13037-60024-53

P2 40 — P3 41 — DATA — 74H4 — 74S74 — CLRREG 172-3 — DCLR — +5V — R11 1K

FBU — FBL — 2MATCH — 2MATCH — 168 — 745157 169 — SEL — 1A 2A 3A 4A 1B 2B — 1Y 2Y 3Y 4Y 4D 3D — 15

P2 21 — ANYER — 74H4 — 74S74 — 74S38 — 74S08 — 68

ROM PRESENT — P2 49

ECC PRESENT — P3 40 — CSYN — PSYN — 74S38 — 74S08 — 68

+5V — R8 1K — 74S03 — 38 7474 — CLR — PR — 4

P2 32 — 18 — 1Ø — 6 — 2Ø — 17

74S08 — 74S32 — 74S08 — 74S32 — 74S08 — 74S32 — 74S08 — 74S32 — 1820-0608 MC 4006P 1-B DECODER

P2 49 — MIØ0 — MIØ1 — MIØ2 — MIØ3 — MIØ4 — MIØ5 — MIØ6 — MIØ7 — MIØ8 — MIØ9 — MIØ10 — MIØ11 — MIØ12 — MIØ13 — MIØ14 — MIØ15

P2 7 — 74S32 — 98 UBOUT

74LS175 108 — D D D D — CLR — Q Q Q Q Q Q — DE FE SE

+5 1K R

197-13-11, 181-4-13 — CLRREG — CLR REG to upper 6 — CLR REG to lower 7 — DDCLK — $ DATA-CLK to upper 6 — DATA-CLK to lower 7 — INHIBITC — INHIBITP

74S38 — R7 1K — 45 — 74S74 38 — 172 — 118

P3 36 — EOW — 74S93A 159 — R0 R1 — QD QC QB

74S20 — 74S00 — 129 — SC — 74S74 149 — DDCLK — +5V 1K

WALLY CLK — P3 32 30 28 — INHIBITP — INHIBITC — DATA-CLK — DATA-CLK

DDCLK 172-11 — 74S74 149 — 74S00 — 88 — EN SHIFT/LOAD to upper 6 — EN SHIFT/LOAD to lower 7 — SC

INNERCCLK — P3 6 — 74H4 — 74S04 147 — 74S74 182 — DCLK — 74S11 171 — CLRREG, 172-3

DMB123N SN74S257 P7-372 — 107 — 97 — 87 — 77 — SEL — 8123 — ZA ZB ZC ZD — IØA IØB IØC IØD I1A I1B I1C I1D

P3 147 — 13 12 — 1 — 2 — 3 — 4 — 5 — 6 — 7 — 9 — 10 — 11 — 12 — 13 — 14 — 15

FBU

158 — 13 — 12 — 10 — 1 — 9 — 7 — 5 — 3 — 2

123-13 123-12 123-11 123-5 123-10 123-13 123-5 123-10 — 94-2 94-5 63-2 63-13 64-2 64-5 64-10 64-13 33-2 33-5 33-10 33-13 34-2 34-5 34-10 34-13 63-5 63-10

FBL

138 — 13 12 — 11 10 — 9 8 — 5 6 — 3 4 — 2 1

186-2 186-5 186-10 187-2 187-5 187-10 187-13 156-2 156-5 156-10 156-12 157-2 157-5 159-10 159-13 — 85-10 86-2 136-5 136-10 136-13 85-13 85-1 86-4 — 85-10 85-5 66-2 66-13 67-2 67-5 67-10 67-13 36-2 36-5 36-10 86-13 37-2 37-5 37-10 37-13 66-5 66-10

Ø) IS A 7486

NOTES: 1) * IS AN OPEN-COLLECTOR INVERTER: 74Ø5

2) IS A 74S04

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING UNLESS OTHERWISE SPECIFIED. DIMENSIONS ARE IN INCHES. TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY	9-16-76 DATE
ENGINEER	9/22/76
RELEASE TO PROD.	9/22/76
SUPERSEDES DWG.	

ECC/ROM SCHEMATIC — TITLE

NEXT ASSEMBLY 13037A/B — FINISH — SCALE

HEWLETT PACKARD

13037-60024 PART NUMBER

D-13037-60024-53

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY																SEPIA														
	1	2	3	4		6		8	9		11	12	13	14	15															
16	17		19		21		22	23	25	28	30		32	37	38	43														
45	46	61	63																											

F-13037 -60024 -3

SYM	REVISIONS	APPROVED	DATE
H	REVISED & RELEASED PER ECO-1650 H.A.		
	A.H.S. / EC 48-2177	AHS	1-17-80
J	ADDED P&J MASTER DWG WITH NEW ARTWORK DATE PC 48-2177 REV C		2-26-81
K	[illegible]		
L	SUPERCEDES DWGS F-13037-2 EC 48-3569	KF	6-16-82
M	REVISED PER PCO 48-3239	KF	12-28-82

DATUM

(9) TYP. 24 PLCS.

(6)(3)(4) TYP. 2 PLCS.

(6)(5)(7)

(6)(7)(8)

DIRECTION THROUGH SOLDER WAVE

F-13037-60024

4-20-81

(6)(5)(6)(5)(4)

(4) TYP. 6 PLCS.

NOTES

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS
   ALL RESISTORS 1/8W, 1%
   ALL CAPACITANCE IN MICROFARADS
   ALL CAPACITORS .01 µf CERAMIC DISC
   ALL IC'S 1820-
2. STAMP DATE CODE (OPER 33).
3. INSTALL ITEM (2) 5 PLACES (OPER 35)
4. MASK AS INDICATED PRIOR TO LOADING.
5. USE SUPPORT FIXTURE DURING WAVE SOLDER
6. INSTALL ITEM (3) THRU (8) IN TOUCH-UP
7. INSTALL ITEM (8) PER DWG D-5951-4413-1.
8. SCHEMATIC D-13037-60024-54
9. CLEAN CONNECTORS WITH ALCOHOL IN TOUCH UP
10. ITEM (10) PRINTED WITH WEEK & YEAR & INSTALLED AFTER FINAL TEST.
11. IF PARTS 1816-1161 1816-1211 THRU 1816-1298 & 1816-1312 ARE NOT AVAILABLE USE SUBSTITUTE PARTS 5037-8024 THRU 5037-8047

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
10	1	PRINTED LABEL	7120-6830		
9	24	SOCKET, IC, 16 PIN	200-2482		
8	1	LABEL	7120-5138		
7	1	P.C. SPACE	5040-6058		
6	1	SPACER	5020-7318		
5	5	SCREW	0624-0077		
4	2	EXTRACTOR	5040-6009		
3	2	PIN	1980-0176		
2	5	TERMINAL E1-E5	0360-0284		
1	1	BOARD: ETCHED	13037-80024		

DO NOT SCALE THIS DRAWING	DRAWN BY GROOM 10-19-79 DATE	ECC / ROM ASSEMBLY DWG. TITLE	HEWLETT PACKARD
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: XX ± .02 XXX ± .005	ENGINEER 11-19-80		
	RELEASE TO PROD 11-19-80	NEXT ASSEMBLY SEE WHERE USED	13037-60024 PART NUMBER
	F-13037-60021-2 ⚠ 6-10-81 SUPERSEDES DWG REV C	FINISH — SCALE 2X	F-13037-60024-3
			SHEET 1 OF 1

CONTENTS

Page

1.0 BUS INTERFACE AND DECODE LOGIC 6-1
1.1 IBUS Channel Hardware 6-1
1.2 IFN Function Bus Hardware 6-1
1.2.1 Function Validation 6-1
1.2.2 Interface Selection and Deselection 6-2
1.2.3 Interface Busy Bit 6-2
1.2.4 Flag Functions 6-2
1.2.5 Data Direction Control 6-2
1.2.6 IFCLK Pulse Debouncing 6-2
2.0 FIRST-IN FIRST-OUT (FIFO) BUFFER 6-3
2.1 FIFO Hardware and Control 6-3
2.2 DTRY Flag Generation 6-4
2.3 FIFO I/O 6-4
2.4 Interface Clock 6-4
2.5 FIFO Synchronization and Sequencing 6-4
2.6 FIFO Pointer Logic 6-5
2.7 Overrun Detection 6-5
2.8 Service Request Generation 6-5
2.8.1 Read Mode SRQ Generation 6-6
2.8.2 Write Mode SRQ Generation 6-6
3.0 CPU FLAG LOGIC 6-6
3.1 Channel Selection 6-6
3.2 CPU Input Mode 6-6
3.3 Command Generation 6-6
3.4 Interface Flag Generation and Test 6-7
3.5 Interrupt Request Generation 6-7
3.6 End of Transfer 6-7
APPENDIX I: 2100 Interface Logic and Programming 6-9

21XX INTERFACE PCA

The following describes the operation of the 13037-60023 Disc Interface PCA. The schematic diagrams for this assembly are numbered C-13037-60023-51, 52, and 53; these should be referenced to fully understand this circuit description.

1.0 BUS INTERFACE AND DECODE LOGIC

(These functions are shown in schematic diagram page 13037-60023-52.

1.1 IBUS CHANNEL HARDWARE

The 16-bit bidirectional Interface Bus (IBUS) connecting the Interface PCA to the disc controller is shown at the bottom right of the page. The bus is driven by three-state logic and transmits data with ground-true coding (0 volts = logical 1). Four inverting bus transceiver IC's (U55, U65, U94, and U95) connect the IBUS to the interface data paths.

In the Read mode, controller data on the IBUS is received by these devices and placed on the transceiver OUTBUS, to be sent to the Select Code Comparator, Busy Bit FF, and the FIFO buffer. In the Write mode, data from the FIFO is taken from the transceiver INBUS and sent over the IBUS to the controller. The OUTBUS always contains IBUS data; with the IF-SELECTED line true and a true ENID signal, the 8T34 bus drivers then drive the IBUS with INBUS information (i.e., at this time U63-8 enables the 8T34 drivers at pins 7 and 9 of each chip). Note that the OUTBUS and INBUS are coded positive true (5 volts = logical 1).

1.2 IFN FUNCTION BUS HARDWARE

The unidirectional ground true four-bit Interface Function Bus (IFN0-3) and signals Interface Function Valid (IFVLD), Interface Clock (IFCLK), and Enable Interface Drivers (ENID) are received by 8T37 inverting gates U31 and U71. These devices have Schmidt-trigger hysteresis inputs for maximum noise rejection. The above signals, as well as the 16 IBUS lines, are terminated with resistor voltage dividers (R4, R7, R8, R11, R12, and R13) which provide the proper termination impedance (on the 13037-60025 add-on Interface PCA, these resistors are omitted). The terminator resistors are powered by the disc controller so that powering down the terminated CPU in a multiple-computer configuration will not affect the buses.

Note that the Enable Interface Receiver (ENIR) signal, while not used by this card, is still terminated. Also, the IFCLK signal must be terminated by one-half of the normal impedance (two dividers in parallel) for proper matching.

1.2.1 FUNCTION VALIDATION

The function placed on the IFN bus by the controller is decoded by U41. Functions are validated by the IFVLD signal which is used to enable the decoder via pins U41-18 and 19. The outputs of the decoder are normally high and will go low when the particular function is decoded. Note that this low state will persist only as long as the IFVLD signal is true (typically

600 nsec, though it can be as long as 350 μs; only during setting of the interrupt is IFVLD as short as 400 nanoseconds, due to the fact that we are interested only in the trailing edge to latch in this interrupt signal at the interface).

1.2.2 INTERFACE SELECTION AND DESELECTION

Since up to eight CPU's can be connected to one disc controller, most interface functions will not be executed unless the interface is selected (selection is the process by which the controller tells the interface whether it is to respond to an Interface Function). Flip-flop U72-4 indicates the state of interface selection (a "one" indicates the unselected state and a "zero" indicates selection). Note that this flip-flop enables all U41 decoded IFN bus instructions except those that select (IFSEL) and deselect (DSCIF) the interface.

The interface is deselected at CPU power-on by the backplane signal PON (U72-2), or by the reception of a Disconnect Interface (DSCIF) Function decoded by U41-10 and applied to U72-3.

To select an interface, the controller puts the binary address (0 – 7) on the three lowest bits of the IBUS and issues a Select Interface (IFSEL) on the IFN bus. There are three address selection jumpers on the PCA that determine the select address to which the card will respond. When the IFSEL function is decoded by U41-4, comparator U44 checks for a match between the jumper value and the controller's select address. If a match occurs, the "=OUT" pin (U44-6) will go high, placing the Select FF in the Selected state; this state is indicated by the Select LED CR1, which is driven by gates U32-1 and U32-13.

1.2.3 INTERFACE BUSY BIT

The Busy Bit FF at the upper right corner of the page is used by the controller to indicate to the CPU that a command is currently being executed. The BUSY signal (generated by U41-16) will clock the lowest bit of the IBUS into this FF. Note that when the interface is unselected, the FF is always cleared (U62-1).

1.2.4 FLAG FUNCTIONS

The function STINT, STDFL, and DVEND are logically OR'ed by U21-12 and conditioned by SELECTED (U12-8) to produce the SETFLAG signal, used by the CPU Flag Logic of the board (see section 3.4).

1.2.5 DATA DIRECTION CONTROL

The READ and WRITE signals developed by U51-4 and U51-1 are used to control the direction of data through the FIFO buffer (section 2.3). READ and WRSRQEN (U51-10) are used by the SRQ logic to request DMA transfer cycles (section 2.8).

1.2.6 IFCLK PULSE DEBOUNCING

In order to prevent ringing on the IFCLK signal from entering (or removing) a data word to (or from) the FIFO more than once, the IFCLK Debouncer circuit is included (shown at the upper left corner of the page). Quad flip-flop U102 is wired as a four-bit shift register; it is clocked by the 10 MHz on-card oscillator (section 2.5), and cleared at power on by the POPIO signal.

When an IFCLK pulse is received, FF U72-9 is set. This "one" is shifted four times by U102 (taking 400 nsec); when it reaches the fourth stage, FF U72 is reset by U102-14 (the "one" complemented), and further IFCLK transitions are prevented from setting the FF again by gate U63-11. (Note that IFCLK pulses validate individual IBUS word transfers.)

When the "zero" at U72-9 reaches the fourth stage (another 400 nsec), the debounce circuitry is again ready to accept another IFCLK pulse. Thus the first transition of IFCLK will produce a debounced IFCLK (DBIFCLK) that is 400 nsec long. This signal is then used to enter or remove data from the FIFO buffer (section 2.6). Note that almost all IFCLK signals are 400 nsec in duration; the exceptions are as follows: retry counter sets during cold load read and set file mask instructions, and controller busy bit sets during the setup or BSYST subroutines (each time these signals are 200 nsec). Note that these 200 nsec signals will not affect the FIFO.

RC filter R9-C12, with a delay of about 50 nsec, prevents random noise pulses that might appear on IFCLK from triggering the debounce circuitry. Since IFCLK is unsynchronized to the 10 MHz clock signal, the output of the debouncer could be skewed as much as 100 nsec from the input. Added to the 50 nsec RC filter delay, this means that DBIFCLK could trail IFCLK by as much as 150 nsec. This skew, however, will cause no problems in the transfer of data due to the long data hold time (greater than one microsecond) of the 13037 Controller.

2.0 FIRST-IN FIRST-OUT (FIFO) BUFFER

(The FIFO buffer and related logic is shown on schematic page 13037-60023-53.)

2.1 FIFO HARDWARE AND CONTROL

All data and commands exchanged by the disc controller and the interface pass through the FIFO buffer, shown at the right side of the schematic. Comprised of LSI IC's U45, U84, U75, and U105, this buffer can store up to 16 words. A four-bit slice of all 16-bit words is stored in each of the four FIFO IC's.

Three signals control the operation of the FIFO. Master Reset (MR) on pin 11 will clear all internal FIFO pointers, control logic and flags. Parallel Load (PL) on pin 2 will cause the word present at the D inputs to be loaded. Transfer Out Parallel (TOP) on pin 13 will pull the next word in the buffer to the outputs (if no new word is in the FIFO, the old value will remain).

Two flags are provided by the FIFO to indicate the level of fullness. Output Register Empty (ORE) indicates that no data words are in the buffer, and Input Register full (IRF) signals that no space is available for additional data words.

When the PL pin of the FIFO IC's is pulsed, the data is loaded into an internal input register. The IRF signal will go low to indicate that loading is occurring. IRF is passed from each FIFO IC to the next via the IES input (pin 9). When IRF of U105 goes low, this indicates that all four of the input registers are loaded. This signal then feeds Transfer To Stack (TTS, pin 10) of each FIFO IC, "dumping" the word into the fall-through stack to the first available level. If the stack is not full, IRF will then return to the high state.

In a similar manner, the ORE signal is cascaded between FIFO IC's via the OES input (pin 15). When ORE of U105 goes high, this indicates that all four IC's have valid data at their outputs.

2.2 DTRDY FLAG GENERATION

The ORE signal is used to drive the Data Ready (DTRDY) flag to the controller, indicating that data is valid to the FIFO. In all, five flags are driven by tri-state driver U82 onto the uni-directional Flag Bus. The outputs of U82 are enabled when the interface is selected. The remaining four flags will be mentioned in later sections.

2.3 FIFO I/O

The 16-bit output of the FIFO is sent to one of two destinations. During a Write operation, FIFO data is sent via the IBUS transceivers to the disc controller. For Read functions the FIFO word is placed on the CPU input bus (IOBI) by driver gates U46, U56, U76, U85, U86, U96, and U106. These backplane drivers are enabled by the computer signal IOISC, derived by the CPU Flag Logic (section 3.2).

Similarly, the input data to the FIFO can come from two sources: the IBUS transceivers during Read; or the CPU output bus (IOBO) during Write. Input multiplexer U54, U64, U74, and U104 select between these sources as directed by the decoded READ signal. These devices also contain data latches, which ensure that the data is stable before a PL pulse is applied to the FIFO. Note that the 16 IOBO signals, since they come from the computer's CTL backplane, require pull-down resistors to the −2 volt supply to ensure a proper logical zero voltage level.

2.4 INTERFACE CLOCK

The on-card 10 MHz oscillator is shown at the upper left area of the schematic. This crystal-controlled signal is used to clock the IFCLK Debouncer, the FIFO Synchronizer-Sequencer, and the FIFO pointer.

2.5 FIFO SYNCRHONIZATION AND SEQUENCING

The FIFO Synchronizer-Sequencer is used to control the loading and unloading of the FIFO buffer. Hex flip-flop U92 is connected to form two separate shift registers; the two-bit register on the left generates the TOP signal for unloading, and the three-bit register on the right generates PL for loading.

When the computer inputs a word from the FIFO (U83-4) or the controller sends an IFCLK in the Write mode (U83-8), gate U83-6 will send a "one" to shift register input U92-13. After the trailing edge of this input, gate U81-4 will generate a TOP pulse to remove a word from the FIFO and decrement the FIFO pointer.

Similarly, when the computer enters a word into the FIFO (U83-1) or the controller sends an IFCLK in the Read mode (U83-11), gate U83-3 will load the data into the Input Register and apply a "one" to shift register input U92-3. Some time (100 − 200 nsec) after the trailing edge of this input, gate U81-1 generates a PL pulse to load the FIFO and increment the pointer (the added delay for loading is necessary to ensure that the data has settled at the outputs of the input register before loading the FIFO).

When the computer and controller are transferring data (since the two devices are unsynchronized), it is quite possible that one device will try to load a word into the FIFO at the same time that the other is removing one. In this case the FIFO Synchronizer-Sequencer will generate a PL pulse and a TOP pulse at the same instant. The LSI FIFO devices are able to handle this situation with no resulting loss of data. This condition is also automatically handled by the FIFO pointer.

2.6 FIFO POINTER LOGIC

Shift register U101 functions as a pointer to indicate the number of words contained in the FIFO at any time. The register is configured as a Johnson ring counter, which has the following count sequence:

COUNT	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

The pointer is reset to zero whenever the FIFO is cleared by a Master Reset pulse. The 10 MHz oscillator continually clocks the register; mode inputs S0 and S1 determine the direction of data shift. In the quiescent case (no loading or unloading of the FIFO), both mode inputs are low and thus no shifting occurs. When a PL pulse is generated by U81-1, S0 goes high, causing the register to shift to the right, "increasing" the count. Similarly, a TOP pulse will set S1 high and a left shift "decrement" will occur. The PL and TOP pulses are present for only one clock period (100 nsec), so that only one count will be recorded per FIFO transaction.

If both PL and TOP pulses occur simultaneously, both mode inputs will be high. In this case, the register will perform a parallel load function. Since the inputs have been connected to the corresponding outputs, the present count value will be reloaded into the register. Thus a simultaneous loading and unloading of the FIFO will cause the pointer to be unchanged, which is exactly the desired result.

Two values of the counter are decoded for other circuit operation. Gate U81-10 generates the FIFO0 signal to indicate that the FIFO is empty, and U81-13 generates FIFO1 to signal that one word is present.

Note: The ORE signal can also indicate that the FIFO is empty. However, because this signal momentarily pulses every time that something is removed from the FIFO, gate U81-10 was required to achieve steady-state signal.

2.7 OVERRUN DETECTION

The Overrun Detector determines when data has been lost due to overflowing or underflowing of the FIFO. And-or-invert gate U73-6 is used to detect this condition, which is stored in the Overrun FF U62-8. When the interface is neither in the Read nor Write mode, gate U63-6 clears the overrun condition. If the FIFO Sequencer tries to load a word (PL, U73-4) when the FIFO is full (IRF, U93-6), or remove a word (TOP, U73-4) when the buffer is empty (ORE, U93-8), gate U73-6 will generate an UNDER/OVERFLOW pulse. If this occurs before the end of the block transfer (EOD1, U42-2), gate U42-1 will set the Overrun FF. Flag Bus driver U82-9 then forwards this condition to the controller.

2.8 SERVICE REQUEST GENERATION

The SRQ circuitry generates a Service Request to the CPU, telling the DMA channel to transfer a word to or from the interface. The SRQ flip-flop (U43-8) is clocked by CPU backplane signal ENF, which occurs at phase T2 of every instruction cycle.

2.8.1 READ MODE SRQ GENERATION

Gate U73-8 determines when an SRQ should be generated. In the Read mode, the SRQ logic will try to keep the FIFO empty. Thus whenever the ORE signal (U73-9) indicates that the FIFO is not empty, U73-8 will go low, causing a Service Request to occur. However, if the computer is currently reading the last word in the FIFO, no SRQ should be generated, since at the end of the current CPU read no words will be left. Gate U63-3 detects this condition and inhibits the SRQ signal for the current CPU cycle by clearing the SRQ FF (U43-10).

2.8.2 WRITE MODE SRQ GENERATION

In the Write mode the SRQ logic tries to keep the FIFO stocked with words for the controller. Although the FIFO can hold up to 16 words, the Write fullness level has been limited to five to prevent unnecessary hogging of CPU memory cycles. Gate U73-13 uses the rightmost bit of the FIFO pointer to determine when four words are in the buffer; when this level has been reached, SRQ is shut off. Since SRQ can be generated as the fourth word is arriving, a fifth word can be obtained, achieving the maximum Write level of five words.

3.0 CPU FLAG LOGIC

(These functions are shown in schematic diagram page 13037-60023-51.)

3.1 CHANNEL SELECTION

In the upper left corner of the schematic, gate U25-12 combines CPU backplane signals IOG, LSCL, and LSCM to produce the Channel Select (CHANSEL) signal. CHANSEL indicates that the current CPU instruction is addressed to this interface card, and therefore is used to qualify most of the other backplane signals shown on this schematic page (the suffix "SC" is appended to these signals to indicate that they have been qualified; e.g., CLC becomes CLCSC). Since the backplane signals are driven by CTL logic, pull-down resistors to the −2 volt supply are needed to insure a valid logical-zero level.

3.2 CPU INPUT MODE

The IOI signal indicates that the CPU is executing an input instruction. Flip-flop U43-5 (at the right of the page) conditions IOI with CHANSEL to eliminate backplane skew between these two signals. Gate U35-6 then reconstructs the IOISC signal, which is used to gate a FIFO word onto the CPU input bus.

3.3 COMMAND GENERATION

To send the controller a command, the CPU first sends a Clear Control (CLCSC) to the interface, which will reset the FIFO and set the COMMAND FOLLOWS FF, U33-5. On the following output instruction, IOOSC will cause gate U13-6 to place the CMRDY flip-flop (U23-4) in the "true" state. When the FIFO flag ORE indicates that the command is valid at the FIFO output, gate U42-10 and Flag Bus driver U82-7 will forward the CMRDY flag to the controller. The outputting of the command will also clear the COMMAND FOLLOWS FF by clocking in a zero. The CMRDY FF is cleared by the Power-on Preset signal (POPIO, U23-2), by the controller function Get Command (CLRCMRDY, U23-3), or by the CLRCMRDY signal generated at the BUS and Interface Decode Logic (previoulsy described).

3.4 INTERFACE FLAG GENERATION AND TEST

The FLAG BUFFER flip-flop (U14-9) latches the interface flag condition asynchronously to CPU backplane timing. This FF is reset by signals CLFSC (U26-6) or when an interrupt from the interface is acknowledged by the CPU (U26-3). Gate U26-8 logically OR's these conditions to reset this FF (U14-10). The FLAG BUFFER FF can be set by these signals: POPIO, STFSC, or the controller initiated CSETFLAG. Flip-flop U33-8 detects the trailing edge of the controller command; if the FLAG FF is not currently set, U42-4 will allow the controller to set the FLAG BUFFER FF via gate U25-8.

The contents of the FLAG BUFFER are loaded into the FLAG FF at time T2 by gate U13-11. The FLAG FF is cleared by the backplane signal CLFSC, which also clears the Trailing Edge Detect FF.

When the CPU executes an SFS (Skip on Flag Set) instruction, U34-6 will send the state of the FLAG FF over the backplane SKF signal. An SFC (Skip on Flag Clear) command will allow U34-12 to report the state of the Busy Bit FF (section 1.2.3).

3.5 INTERRUPT REQUEST GENERATION

The CONTROL FF (U14-13) acts as an interrupt mask for the interface card. It is set by a CPU STC instruction (U14-15) and cleared by the CLC instruction (U14-14). The state of the CONTROL FF is sent by Flag Bus driver U82-3 to the controller as the INTOK flag. If true, the controller can generate a subsequent interrupt.

The INT REQ flip-flop (U14-4) is used to generate interrupts to the CPU. It is reset at cycle T2 of each instruction by signal ENF (U14-1). INT REQ will be set at cycle T5 by signal SIR (U35-13) if all of the following conditions are met:

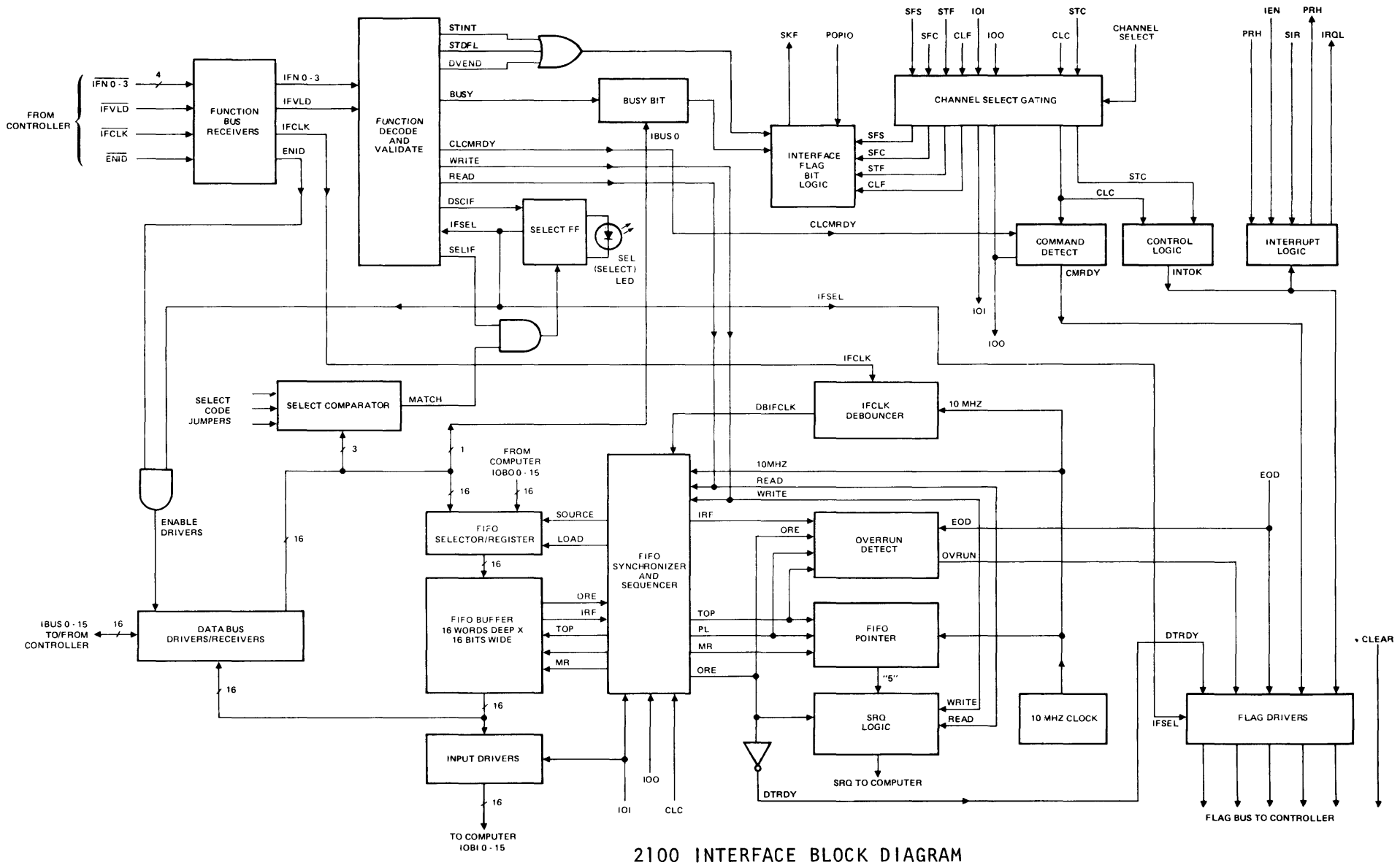
1) The PRH interrupt priority from other interface cards is true (U35-12).
2) The CONTROL FF is set (U25-5).
3) IEN is true (U25-3).
4) The FLAG FF is set (U25-4).
5) The FLAG BUFFER FF is set (U34-9).

The INT REQ signal is sent via backplane driver U15-9 and U16-9 to the CPU.

3.6 END OF TRANSFER

When the computer DMA channel has sent or received the last word of a block transfer, a pulse will appear on the EDT backplane signal. Gate U36-6 conditions this signal with CHANSEL and sets the EOD1 FF, U23-13. In the Read mode, the output of gate U22-3 will be high, allowing gate U22-11 to immediately set the EOD2 FF, U23-9. Flag Bus driver U82-5 forwards the End of Data flag to the controller. In the Write mode, however, there may still be words left in the FIFO to be sent to the controller before EOD can be signaled. Gate U22-6 uses the FIFO0 output of the FIFO pointer to detect when all words have been transferred. If the FIFO was empty at the time that the last word arrived, the FIFO pointer must be given time to update before the EOD flag is set: flip-flop U23-7 (at the right of the page) causes the EOD logic to wait until the next CPU cycle before gate U22-6 decides that the FIFO is empty. When the last word is finally removed by the controller, EOD will then be signaled.

The EOD2 is also set by signal CLCSC, which resets the FIFO and tells the interface that a COMMAND FOLLOWS. EOD2 is cleared whenever the controller fetches a command from the interface (CLRCMRDY, U23-10).



2100 INTERFACE BLOCK DIAGRAM

APPENDIX I
2100 INTERFACE LOGIC AND PROGRAMMING

A. CPU COMMANDS AND THE 2100 INTERFACE

Certain CPU commands work directly with the interface card in the selected channel that the command references. These commands are reproduced in table 6A-1 with the corresponding effects they have on the 2100 interface. Note that no select codes are shown.

Figure 6A-1 represents a simplified version of the 2100 interface's CPU flag logic. Certain CPU backplane signals (at the top of the illustration) correspond directly to entries in table 6A-1 (such signals are STC, CLC, STF, CLF, SFS, and SFC). Other signals are generated as a result of certain of the commands in the table (IOI becomes true for LIA/B and MIA/B instructions, while IOO becomes true for OTA/B instructions). Other signals govern interface channel selection and CPU/interface communications as will be described below.

B. 2100 INTERFACE HARDWARE

Figure 6A-1 is subdivided into numbered sections by broken lines and will be discussed separately. It should be noted that only the CPU flag logic is shown; FIFO logic, service request generation, and function decoding of 13037 bus signals are not shown.

Table 6A-1. CPU Commands to 2100 Interface

COMMAND	FUNCTION
STC	Sets control FF and turns on device on channel specified by S.C.
CLC	Clears control FF and turns off device (aborts data transfer if programmed).
STF	Sets when data transfer finished.
CLF	Clear flag FF on interface card.
SFS	Test if data transfer is completed.
SFC	Test if data transfer still in progress.
LIA/B	Transfer data from I/O interface buffer to A/B register.
MIA/B	Merge data from I/O interface buffer to A/B register.
OTA/B	Transfer data from A/B register to specified interface card.

Before any CPU signals can be recognized by the interface, the channel in which the interface card resides must be selected. The backplane signals necessary to do this (IOG, LSCL, and LSCM) are combined in section (2) to create the qualifying CHANSEL signal. This signal is used internally by the interface to qualify other CPU-generated control signals.

To input or output information through the interface, the FIFO circuitry must be told the fact that a transfer is to occur, and which direction that transfer is to take. This communication takes place via the IOISC (I/O input to CPU, with interface channel selected) and IOOSC (I/O output from CPU, with interface channel selected). These signals are generated directly by IOI and IOO, respectively.

When outputting information through the interface, the CPU must inform the controller of any words that are meant to represent one of the twenty-one 13037 instructions. Section (7) contains the required hardware to generate the necessary CMRDY flag. The CONTROL flip-flop (section (3)) is first cleared by the CLSC signal (generated by a CPU CLC command to the proper channel). The CLSC signal clears the output register of interface FIFO, and also presets the COMMAND FOLLOWS flip-flop of section (7), thus latching the fact that the next IOO from the CPU will correspond to a 13037 instruction. When that IOO is issued, the CMRDY flip-flop becomes reset, and when the FIFO acknowledges the receipt of the command word (ORE — output register empty — goes false), the CMRDY flag goes true. As the controller fetches the command (via the IFGTC function), CLRCMRDY sets the CMRDY flip-flop and causes the CMRDY flag to disappear. Further transfers will not be interpreted as commands unless preceded by a CLC. (Note that POPIO — power on preset I/O — also sets the CMRDY flip-flop to disable the CMRDY flag; additionally, a CRS — clear signal, not shown — will reset the COMMAND FOLLOWS flip-flop.)

Section (4) represents the actual flag logic, and interacts with section (3) during interrupt generation. STINT, DVEND, and STDFL generated by the 13037 are OR'ed at the interface so as to allow the FLAG DETECT flip-flop of section (4) to latch the occurrence of any of those signals. In order to detect any occurrence of these flags, the CPU must first generate the CLFSC signal (CLF to the proper channel) to reset the FLAG DETECT, FLAG BUFFER, and FLAG flip-flops. When a subsequent flag is detected by the FLAG DETECT flip-flop, the FLAG BUFFER flip-flop becomes set so that the following ENF signal (generated automatically at phase T2 of the CPU cycle) can update the FLAG flip-flop. The flag is then held for later interrupt generation by section (3), or flag test by section (5). Note that the FLAG BUFFER flip-flop is additionally set by POPIO or STFSC (though the latter is used only during diagnostic testing), and is additionally reset whenever a requested interrupt is acknowledged by the CPU IAK signal.

Actual interrupts are allowed whenever the CONTROL flip-flop of section (3) is in the true (set) state. Setting the CONTROL flip-flop is accomplished by the CPU's issuance of a STC instruction to the interface channel (STCSC). With the CONTROL flip-flop set, the INTOK flag to the 13037 goes true to inform the 13037 that an interrupt can be subsequently generated. Additionally, INTOK is combined with IEN (the CPU-generated interrupt enable signal) to qualify any 13037-generated flag detected by the 2100 interface as being an interrupt. This new signal will be used to set the IRQ (interrupt request) flip-flop whenever the FLAG BUFFER flip-flop is set and the daisy chain priority hardware of section (1) determines that this interface has the highest priority of those interfaces currently requesting an interrupt. The IRQ flip-flop then generates the IRQL and FLGR signals to the CPU.

After interrupt request receipt, the IAK signal from the CPU resets the FLAG BUFFER flip-flop as previously described. The IRQ flip-flop is automatically reset at the appropriate time (and the FLAG flip-flop of section (4) is set with any new flag held by the FLAG BUFFER flip-flop) by the CPU hardware-generated ENF signal.

In cases where flags are not to be interpreted as interrupts (i.e., during transfers of parameters as previously described), the CPU does not set the CONTROL flip-flop (recall that a CLCSC signal resets this flip-flop as the initial 13037 command is sent). Instead, the CPU monitors the condition of section (4)'s FLAG flip-flop by issuing a SFS instruction to the proper channel. The AND gate of section (5), when the channel is selected and the SFS instruction has been executed, will gate the contents of the FLAG flip-flop over the SKF (skip flag) line to the CPU. Note, however, that the AND gate of section (6) also can gate the status of the interface

NOT BUSY bit to the CPU over the SKF line. Thus, whenever the CPU executes a SFC instruction to the interface channel, the SKF line will inform the CPU as to the status of this bit (remember that this bit is true whenever the 13037 is currently executing an instruction; it should be noted, however, that because the 13037 accepts and executes most commands extremely fast, the SFC instruction is really only useful for the CPU to determine if a DMA transfer is still in progress). Hence, for the 2100 interface, SFS (skip if flag set) and SFC (skip if flag clear) test different functions, not complementary aspects of the same function.

C. BASIC 2100 INTERFACE PROGRAMMING EXAMPLE

Based on the above discussion of the 2100 interface hardware, it can be seen that certain instruction sequences must be generated by the CPU in order to obtain the expected results. To illustrate some of these sequences, the following example is included to illustrate the way in which a CPU could issue a VERIFY command to the 13037.

LDA	CMD	CPU updates the A and B registers with the VERIFY command (from CPU register CMD) and the sector
LDB	SCTC	count (from CPU register SCTC)
CLC,C		sets up first word transferred as being a 13037 instruction and clears the interface flag logic
OTA		outputs VERIFY command to interface
SFS		waits for 13037 to accept the command and subsequently request the sector count by issuing a STDFL
JMP	*-1	command to the interface
OTB,C		outputs sector count to interface and clears the previously detected flag
SFS		waits for the 13037 to indicate command completion (13037 issues either STINT, DVEND, or STDFL when
JMP	*-1	done)

Two important aspects of the above program segment should be recognized. First, command completion was tested by the second SFS instruction. Although current command execution could be tested by the SFC instuction, some commands are executed so quickly that only command completion can be tested; thus SFC should be used only to determine the state of any DMA transfers. Second, command completion does not indicate in what state the command had completed; recall that the interface OR's together STDFL (normal completion), DVEND (data transfer error), or STINT (any other error) to produce the single interface flag. Therefore a REQUEST STATUS command should be issued to determine the completion state of any transfer operation.

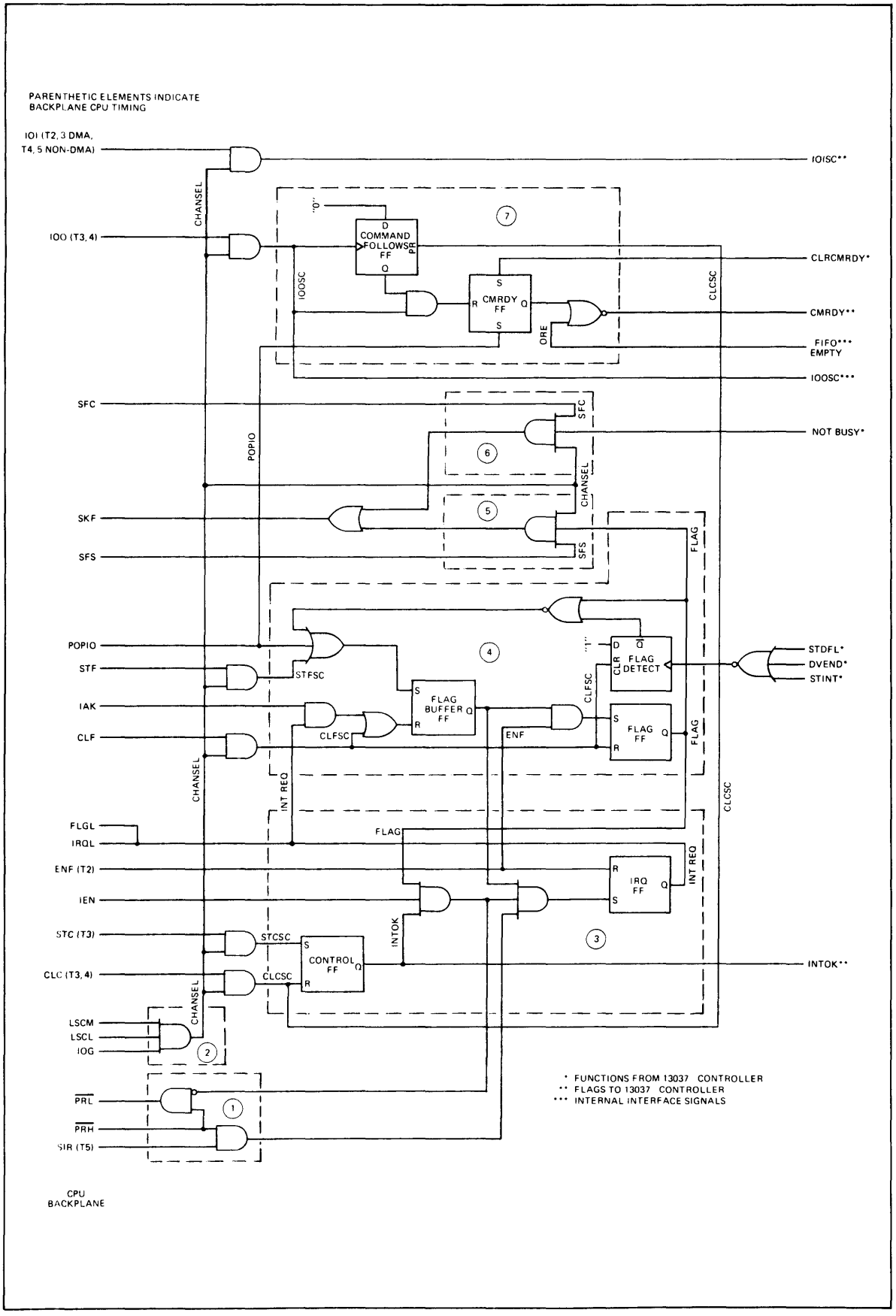


Figure 6A-1. 2100 Interface CPU Flag Logic

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60023
13037-68023

DATE CODE : C-1635

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C1	0160-2055	CAP .01UF-20+80%
C10	0160-2055	CAP .01UF-20+80%
C11	0180-0374	CAP 10UF 10%
C12	0140-0198	CAP 200PF 5%
C13	0160-2055	CAP .01UF-20+80%
C14	0180-0374	CAP 10UF 10%
C15	0160-2055	CAP .01UF-20+80%
C16	0160-2055	CAP .01UF-20+80%
C17	0160-2055	CAP .01UF-20+80%
C18	0160-2055	CAP .01UF-20+80%
C19	0160-2055	CAP .01UF-20+80%
C2	0160-2055	CAP .01UF-20+80%
C20	0160-2055	CAP .01UF-20+80%
C21	0140-0198	CAP 200PF 5%
C22	0160-2055	CAP .01UF-20+80%
C23	0160-2055	CAP .01UF-20+80%
C24	0160-2055	CAP .01UF-20+80%
C25	0160-2055	CAP .01UF-20+80%
C3	0160-2055	CAP .01UF-20+80%
C4	0160-2055	CAP .01UF-20+80%
C5	0160-2055	CAP .01UF-20+80%
C6	0160-2055	CAP .01UF-20+80%
C7	0160-2055	CAP .01UF-20+80%
C8	0180-0374	CAP 10UF 10%
C9	0160-2055	CAP .01UF-20+80%
CR1	1990-0327	DIODE-LIGHT EMIT
E1	0360-0294	TERM-SOLDER STUD
E3	0360-0294	TERM-SOLDER STUD
R1	1810-0280	NTWK RES 9X10K
R10	1810-0275	NTWK RES 9X1K
R11	0757-0417	RES 562 1%.125
R12	1810-0127	RES N 6(240+560)
R13	0698-3442	RES 237 1%.125
R14	1810-0275	NTWK RES 9X1K
R15	0757-0280	RES 1K 1%.125
R16	0757-0278	RES 1.78K 1%.125
R17	0757-0280	RES 1K 1%.125
R18	0757-0278	RES 1.78K 1%.125
R19	0757-0419	RES 681 1%.125
R2	1810-0275	NTWK RES 9X1K
R3	0757-0403	RES 121 1%.125
R4	1810-0127	RES N 6(240+560)
R5	0757-0280	RES 1K 1%.125
R6	1810-0275	NTWK RES 9X1K
R7	1810-0127	RES N 6(240+560)
R8	1810-0127	RES N 6(240+560)
R9	0698-3438	RES 147 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60023
13037-68023

DATE CODE : C-1635

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U101	1820-1304	IC SN74S194N
U102	1820-1195	IC SN74LS175N
U104	1820-1100	IC SN74298N
U105	1816-0934	IC 9403 PC
U106	1820-1080	IC 8T13B
U12	1820-0174	IC SN7404N
U13	1820-0054	IC SN7400N
U14	1820-1089	IC SN74279N
U15	1820-1080	IC 8T13B
U16	1820-1080	IC 8T13B
U21	1820-0068	IC SN7410N
U22	1820-0054	IC SN7400N
U23	1820-1089	IC SN74279N
U24	1820-0174	IC SN7404N
U25	1820-0686	IC SN74S11N
U26	1820-1197	IC SN74LS00N
U31	1820-1817	TC-DS8837N
U32	1820-0327	IC SN7401N
U33	1820-0077	IC SN7474N
U34	1820-0068	IC SN7410N
U35	1820-1367	IC SN74S08N
U36	1820-0054	IC SN7400N
U41	1820-0495	IC SN74154N
U42	1820-0328	IC SN7402N
U43	1820-0693	IC SN74S74N
U44	1820-0921	IC SN7485N
U45	1816-0934	IC 9403 PC
U46	1820-1080	IC 8T13B
U51	1820-0328	IC SN7402N
U52	1820-1080	IC 8T13B
U53	1820-0174	IC SN7404N
U54	1820-1100	IC SN74298N
U55	1820-1845	IC-DS8834N
U56	1820-1080	IC 8T13B
U62	1820-0077	IC SN7474N
U63	1820-0054	IC SN7400N
U64	1820-1100	IC SN74298N
U65	1820-1845	IC-DS8834N
U66	1820-1080	IC 8T13B
U71	1820-1817	TC-DS8837N
U72	1820-1089	IC SN74279N
U73	1820-0063	IC SN7451N
U74	1820-1100	IC SN74298N
U75	1816-0934	IC 9403 PC
U76	1820-1080	IC 8T13B
U81	1820-0328	IC SN7402N
U82	1820-1476	IC 8T96B

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60023
13037-68023

DATE CODE : C-1635

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U83	1820-0054	IC SN7400N
U84	1816-0934	IC 9403 PC
U85	1820-1080	IC 8T13B
U86	1820-1080	IC 8T13B
U91	1820-0174	IC SN7404N
U92	1820-0788	IC SN74174N
U93	1820-0174	IC SN7404N
U94	1820-1845	IC-DS8834N
U95	1820-1845	IC-DS8834N
U96	1820-1080	IC 8T13B
Y1	0410-0436	XTAL 10MHZ

END OF MATERIAL LIST.

C-13037 -60023 -52

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	JR	9/10/76
B	CURRENT DATE CODE C-1635 PC48-3521	MFM	10-12-81

ENGINEERING RESPONSIBILITY / SEPIA

0	1	2	3	4		6		8	9		11	12	14	16	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

DBIFCLK

IFCLK DEBOUNCER

POFIO

10MHz

U102 74LS175

74279 U72

U63

R9 147

200pf C12

FUNCTION DECODER

(OCTAL) Ø0 Ø1 Ø5 03 11 13 14 15 16

STINT STDFL DVEND IFSEL SCLF SFOUT IFIN SFGTC BUSY

74154 U41

A B C D

E1 E2

WRSRGEN

CSET FLAG

WRITE

READ

CLRMDRY

U22 SELECTED

U21

U51

U53

U10

7401 U32

SEL

R3 121

CR1 LED

+5

8T37 U31

IFCLK IFN0 IFN1 IFN2 IFN3 IFVLD

ENID

8T37 U71

U63

R8 240 R8 560 R12 560 240

C11 10µf

J1 16 2 3 B C 7 — IFCLK IFN0 IFN1 IFN2 IFN3 IFVLD

15 T 23 — ENID +5 FROM CNTRLR ENIR

PON

P1 66

.01 C20

IFSELECTED

SELECT FF U72 74279

SELECT CODE COMPARATOR

U53

=IN =OUT 7485 U44

B3 A3 B2 A2 B1 A1 BØ AØ

10K R21

Busy BIT FF

7474 U62

NOTBUSY

+5

1K R5

OUTBUS 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Positive True Data

INBUS Ø 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

8T34 BUS U55 (OUT 1, IN 2)

8T34 BUS U94

8T34 BUS U65

8T34 BUS U95

R7 240 560 — R4 240 560 — R9 240 560 — R11 240 560

Ground True Data

J1 11 12 13 14 — IBUS Ø IBUS 1 IBUS 2 IBUS 3

D E F H — IBUS 4 IBUS 5 IBUS 6 IBUS 7

19 20 21 22 — IBUS 8 IBUS 9 IBUS 10 IBUS 11

W X Y Z J1 — IBUS 12 IBUS 13 IBUS 14 IBUS 15

+5 P1 39 40 1,2 85 86 GND

C14 10µf .01µf

C1-7, 9, 10, 13, 15-20, 22-25

E1, E2, E3

1 9 10 17 18 A J K L M N P U V J1

For 13037-60025, omit R4, R7, R8, R11, R12, R13

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY	DATE 7/22	21XX-13037 Interface Schematic
ENGINEER	7/22/76	TITLE BUS Interface / Decode
RELEASE TO PROD.	9/10/76	13037A 002 / 13175A NEXT ASSEMBLY
SUPERSEDES DWG.		FINISH / SCALE

HEWLETT PACKARD

PART NUMBER C-13037-60023-52

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY ■ SEPIA ▨

0	1	2	3	4	5	6	7	8	9	10	11	12	14	15
16	17	18	19	20	21	22 A			33	34	38		42	43
HP ■	65	80 A		90	50B A		93				B5			

C-13037-60023-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	JTF	7/10/76
B	CURRENT DATE CODE C-1635 PC48-3521	USP MBTM	10/2·81

(DMA=T23)
(NDMA=T45)

EDT (T45) · -2V · LSCL · IOG · LSCM · SIR (T5) · PRH · PRL · CLC (T34) · CRS · STC IEN (T3) · ENF (T2) · IRQL · FLGL · CLF · IAK · STF · POPIO · SFS · SKF · SFC · IOO (T34) · IOI

P1 · 62 · 47 48 · 15 · 16 · 14 · 32 · 23 · 3 · 21 · 13 · 22 · 8 · 46 · 6 · 4 · 7 · 10 · 9 · 17 · 25 · 12 · 5 · 26 · 24 · P1

-2V

R14 1K · R3 1K · R2 1K · 10μf C8 · 74S11 U25 · CHANSEL

R19 681 · R6 1K · R6 1K · R2 1K · R14 1K

R6 1K · R2 1K · R6 1K · R6 1K · R2 1K · R2 1K · R2 1K · R6 1K

U15 8T13 · U16 8T13

R6 1K · R2 1K · R6 1K · 74S08 U35 · CHANSEL

+5 · R5 1K · 74S74 U43

U36 · U16 8T13 · U36 · U36 · U26 LS00 · U26 LS00 · U26 LS00 · 74S11 U25 · U36 · U36 · 74S08 U35 · 74S08

CLCSC · STCSC · CRS · ENF · CLFSC · POPIO · IOOSC · CRS · CLCSC

74279 U23 · EOD1 · READ · FIFO · U22 · U22 · U22

74279 U14 · CONTROL FF · 74S11 U25 · U26 LS00 · 74279 U14 · FLAG BUFFER

74279 U23 · CLRCMDRY · EOD2

7410 U34 · 7410 U34 · U13 · 74279 U14 · FLAG FF · FLAG

74279 U23 · COMMAND FOLLOWS · 7474 U33 · 74279 U23

74279 U23 · CMRDY FF

U13 · U42 · U42 · U83 · 8T96

74S01 U32 · PRESET ENABLE · R1 10K · 8T96

U82 · 8T96

IRQ FF · 74279 U14 · INT REQ

CONTROL · U82

CLFSC · 7474 U33 · TRAILING EDGE DETECT · +5 · R5 1K

SPARES

U13 7400 · U31 7410 · U31 7410 · U32 7401 · U42 7402 · U52 8T13 · U83 · U72 · U72 · 8T37 · HI-Z · O.C.

ALL NAND = 7400
NOR = 7402
INV = 7404

J1 6 EOD FLAG 6 · J1 R CLEAR · J1 8 INTOK FLAG 8 · J1 5 CMRDY

ENF · CSETFLAG · NOT BUSY · ORE · CMRDY · POPIO · IOOSC · IOISC

Unless Otherwise Specified

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING UNLESS OTHERWISE SPECIFIED.
DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY	DATE 7/22	21XX-13037 Interface Schematic	HEWLETT PACKARD
ENGINEER	7/22/76	TITLE CPU FLAG LOGIC	
RELEASE TO PROD.	9/0/76	13037A 002 / 13175A NEXT ASSEMBLY	PART NUMBER C-13037-60023-51
SUPERSEDES DWG.		FINISH · SCALE	SHEET 1 OF 1

ENGINEERING RESPONSIBILITY | SEPIA

0	1	2	3	4		6	8	9	11	12	14	15		
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	USE		50% A			50% B		B5			

C-13037 -60023 -53

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	TK	
B	CURRENT DATE CODE C-1635 PC 48-3521	MJM	10-12-81

IOOSC
READ
DBIFCLK
10MHz
POPIO
IOISC
READ
CLCSC
EOD1
WRITE
FIFOØ
WRSRGEN
IFSELECTED
ENF

U83 U83 U83 U83

FIFO SYNCHRONIZER AND SEQUENCER

74174 U92

U81 U81 U81

R16 1.78K
R15 1K
C21 200
Y1
R17 1K
R18 1.78K

8T37

UNDER/OVER FLOW

74 S1 U73

FIFO POINTER

74S194 U101

8T37

U63 U42 U62 7474 OVRUN FF

R5 1K +5

U81 U81 FIFO1 U63

74 S1 U73

GEN SRQ

INH SRQ

R5 1K +5

74S74 CLR U43 SRQ FF

8T13 U52

SRQ

J1 AA OVRUN FLAG 7

8T96 U82

INBUS Ø 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

(Positive True)

IOØI Ø IOØI 1 IOØI 2 IOØI 3 IOØI 4 IOØI 5 IOØI 6 IOØI 7 IOØI 8 IOØI 9 IOØI 10 IOØI 11 IOØI 12 IOØI 13 IOØI 14 IOØI 15

P1 35 38 41 45 | 42 51 53 52 | 54 56 58 55 | 57 61 65 74

R10 1K R10 1K R10 1K R14 1K R14 1K R14 1K -2V

(Positive True)

OUTBUS Ø 1 2 3 | OUTBUS 4 5 6 7 | OUTBUS 8 9 10 11 | OUTBUS 12 13 14 15

74298 U54 | 74298 U74 | 74298 U64 | 74298 U104

A1 B1 C1 D1 A2 B2 C2 D2 CLK WS QA QB QC QD

INPUT REGISTER/ SELECTOR

ORE

9403 U45 | 9403 U84 | 9403 U75 | 9403 U105

MR D PL CPSI IES EO CPSO OES TOS TTS IRF ORE TOP

FIFO BUFFER

8T13 U46 | 8T13 U86 | 8T13 U66 | 8T13 U106

8T96 U82

P1 26 29 30 64 | 77 80 81 84 | 27 28 31 60 | 78 79 82 83

IOØI 4 IOØI 5 IOØI 6 IOØI 7 IOØI 8 IOØI 9 IOØI 10 IOØI 11 IOØI 12 IOØI 13 IOØI 14 IOØI 15

J1 24 DTRDY FLAG1

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY	DATE	7/26
ENGINEER		7/26/76
RELEASE TO PROD.		9/10/76
SUPERSEDES DWG.		

21XX-13037 Interface Schematic

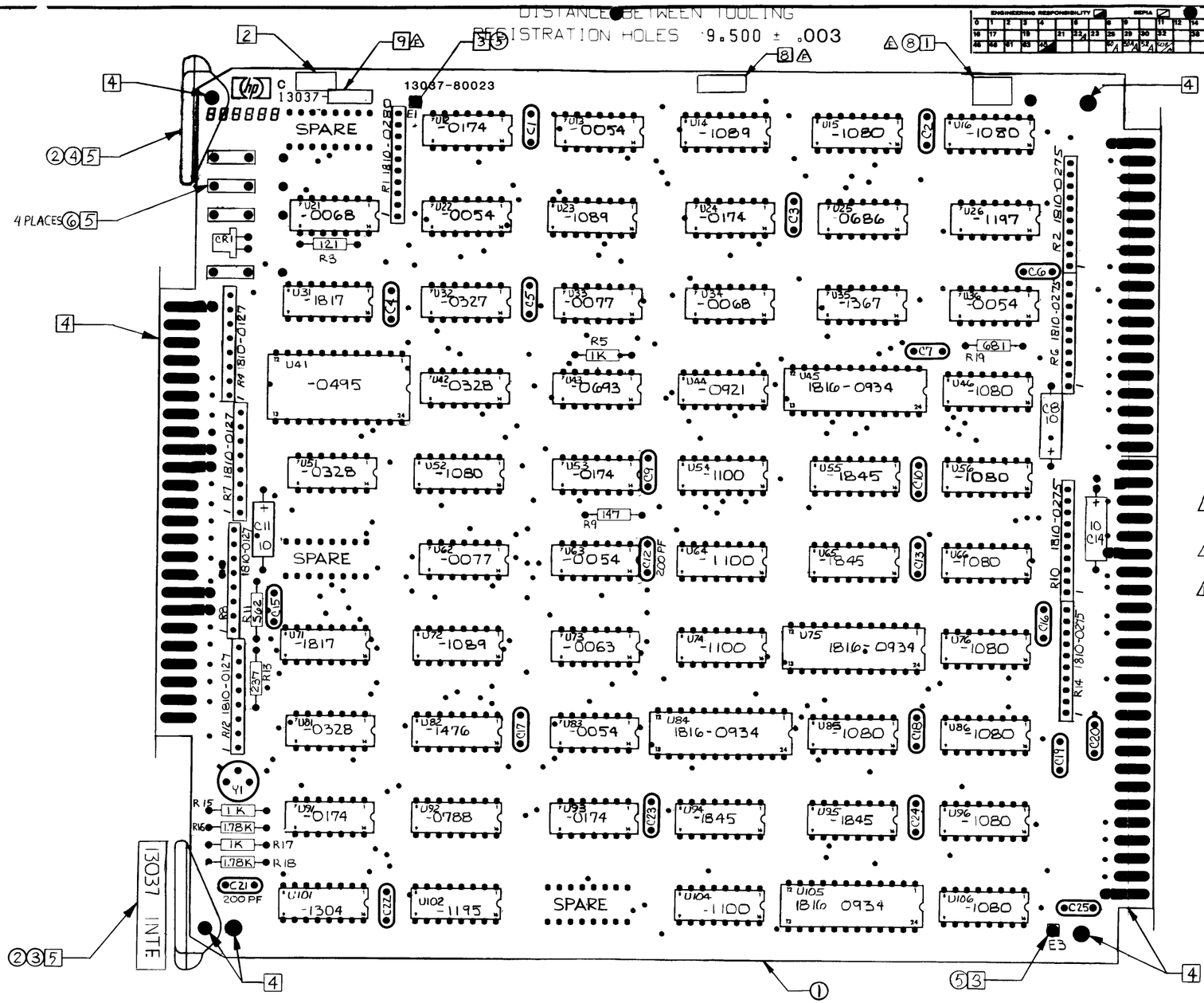
TITLE FIFO BUFFER

13037A 002 / 13175A
NEXT ASSEMBLY

FINISH | SCALE

HEWLETT PACKARD

PART NUMBER C-13037 -60023 -53



D-13037-80023-1

COMPONENT SIDE 1 OF 4

12-16-81

SYM	REVISIONS	APPROVED	DATE
E	REVISED & REDRAWN TO SPECS, BOARD REV. WAS A. 48-2472	KF/PS	4.23.81
F	BD REV WAS B PC 48-3521	MSM	10.12.81
G	CHANGED DIAZO FOR NEW ART WORK DATE PC 48-3521/A	MSM	10.28.81
H	CHANGED DIAZO FOR NEW ARTWORK DATE PC 48-3521/B	MSM	12.3.81
J	CHANGED DIAZO FOR NEW ART WORK DATE PC 48-3521/C	MSM	12.15.81

D-13037-60023-

REFERENCE DRAWINGS } SCHEMATIC C-13037-60023-51,52,53

UNLESS NOTED OTHERWISE:

ALL RESISTANCE IN OHMS
ALL RESISTORS 1/8W 1%
ALL CAPACITANCE IN µF
ALL CAPACITORS .01 CERAMIC DISC
ALL IC's ARE 1820
ALL DIODES ARE 1990-0327

NOTES: UNLESS OTHERWISE SPECIFIED

1. INSTALL ITEM (8) AFTER LINE TEST.
2. OPR.264; MARK ASSEMBLY DATE CODE 1635
3. OPR.265; INSTALL ITEMS (5)
4. OPR.265; MASK PRIOR TO LOADING.
5. OPR.266; TOUCH UP, INSTALL ITEMS (2)(3)(4)(6)
6. CLEAN CONNECTORS IN TOUCH-UP.
7. MARK ITEM (3) PER DWG A-5950-5668-1
8. P.C. PRODUCTION: MARK ASSEMBLY NUMBER, ORDER NUMBER, COMPONENT SIDE ONLY.
9. P.C. PRODUCTION: MARK E... ASSEMBLY NUMBER, COMPONENT SIDE ONLY.
10. THIS BOARD IS NOT ONE-TEST... TESTABLE.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
8	1	ORIGIN LABEL	7120-6830		
7		DELETED			
6	4	JUMPER PLUG	1258-0129		
5	2	TERMINAL	0360-0294		
4	1	EXTRACTOR	5040-6001		
3	1	EXTRACTOR RED	5040-6005		
2	2	PIN	1480-0160		
1	1	BOARD ETCHED	13037-80023		

DO NOT SCALE THIS DRAWING	DRAWN BY	12-27-79 DATE	21XX INTERFACE ASSY DWG
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.	ENGINEER	5-14-81	HEWLETT PACKARD
TOLERANCES ~~XX ± .02 XXX ± .005~~	RELEASE TO PROD.	5-14-81	NEXT ASSEMBLY
SEE CORP. STD. 608	SUPERSEDES DWG		FINISH SCALE 2X

13037-60023 PART NUMBER
D-13037-60023-1

SHEET 1 OF 1

CONTENTS

		Page
1.0	+5 VOLT REGULATOR	7-1
	1.1 Overall Concept	7-1
	1.2 Voltage Reference and Voltage Stability	7-1
2.0	POWER AMPLIFIER	7-2
3.0	FREQUENCY RESPONSE AND LOOP STABILITY	7-3
	3.1 Voltage Control Loop	7-3
	3.2 Frequency Response	7-3
4.0	OVER CURRENT PROTECTION	7-4
	4.1 Circuit Details	7-4
5.0	OVERVOLTAGE PROTECTION	7-4
	5.1 Circuitry	7-4
6.0	THERMAL DESIGN DATA	7-5
7.0	+12 VOLT UNREGULATED SUPPLY	7-5
8.0	−20 VOLT UNREGULATED SUPPLY	7-5
9.0	+20 VOLT UNREGULATED SUPPLY	7-6
10.0	−12 VOLT UNREGULATED SUPPLY	7-6
11.0	−5 VOLT REGULATOR	7-6
12.0	POWER-ON CIRCUIT	7-6
	12.1 Circuit Operation	7-6
Appendix I: Output Specifications		7-7
Appendix II: Troubleshooting Aids at Turn-On		7-9

POWER REGULATOR PCA

1.0 +5 VOLT REGULATOR

1.1 OVERALL CONCEPT

A simplified block diagram of the +5 regulator is shown in figure 1. Unregulated 12 volt DC power is delivered through a "unity" gain power amplifier to the logic board "load" via the Power Distribution circuit board. A unity gain differential amplifier U3D senses the load voltage right at the distribution board output and provides a "single-ended" replica to the minus input of the 723 comparison amplifier. The 723's high gain error amplifier compares the "load voltage" to a stable 5 volt reference (derived from the 723's internal reference) and drives the Power Amplifier to achieve an error null: the negative feedback thus maintains the load voltage essentially equal to the 5 volt reference source, independent of load current and unregulated +12 and +20 volt power variations.

1.2 VOLTAGE REFERENCE AND VOLTAGE STABILITY

The 723 contains an internal temperature compensated zener circuit which provides a stable 7.15 ±5% reference output at pin 6. This voltage is divided down to 5 volts by the R27, R10, R26 string. Potentiometer R10 provides a limited adjustment range to compensate for the 723 and U3D offset voltages, as well as the tolerance on the reference voltage, divider string, and R22-R24. Resistors R33 and R34 connect the sense amplifier to the 5 volt outputs on the regulator PCA for use with earlier Power Distribution boards that do not have remote sensing (13037-60020). When remote sensing is present, R33 and R34 are effectively shorted to the *remote* nodes by traces on the Power Distribution PCA so that the remote voltage is sensed. Note that adjustment of R10 is made with voltmeter connected to the *sense* test points (+5 and COM) rather than at the output of U3D, to avoid errors introduced by the sense amplifier.

The input characteristics of the 723 and U3D amplifiers and the voltage reference stability are such that the major contribution to voltage drift with temperature comes from thermal coefficient of the divider string and differential amplifier resistors; overall worst case performance is ± 0.04%/°C maximum, with typical performance on the order of ± 0.01%/°C (± 70 mv worst case over the temperature range). Long term stability will also be primarily determined by these resistors; 25 mv/1000 hrs. (0.5%) is the expected upper limit.

Ripple rejection to the reference output from the unregulated +20 volts on the 723 is typically 100 microvolts/volts; C14 attenuates high frequency noise and improves rejection at high frequency.

Resistor R25 provides impedance match for the input bias current of the 723 amplifier, and in combination with C12 provides filtering (82 KC) to reject high frequency noise and extraneous signals which could disturb loop operation.

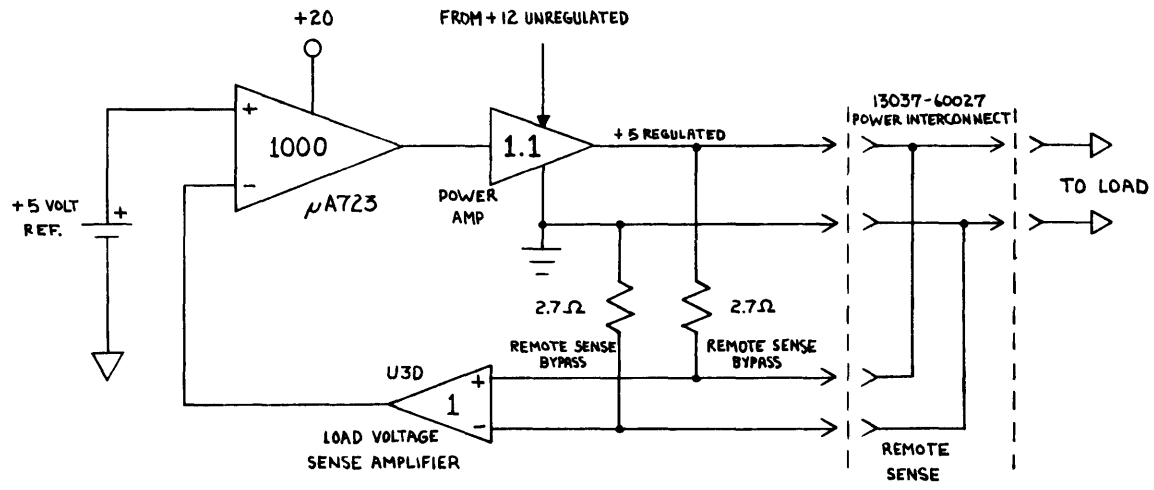
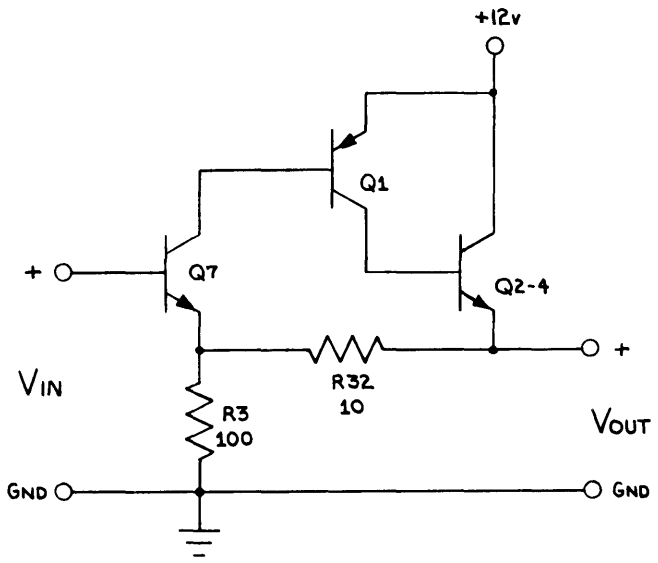


Figure 1

2.0 POWER AMPLIFIER

Transistors Q7, Q1, and Q2-Q4 are the active elements of a power amplifier shown below in simplified form.



Q2-Q4 and Q1 comprise a complimentary Darlington pair drive by Q7; series feedback (R3 and R32) provides a stabilized voltage gain of 1.1, independent of the transistor betas. Since this amplifier is in turn part of the overall negative feedback loop maintaining the load voltage, the local feedback employed here desensitizes the gain of the overall loop with respect to the Q7, Q1, and Q2-Q4 parameters.

Referring to the schematic, Q2, Q3, and Q4 are power transistors driven in parallel by Q1. Resistors R4-R6 give local emitter degeneration to insure that the output current splits equally among the three (as well as to provide current sense information). R40 and R35 set the DC operating point of Q7 and Q1.

3.0 FREQUENCY RESPONSE AND LOOP STABILITY

The closed loop bandwidth of the power amp is nominally 100KC, but is slightly dependent on load current. The 650 microfarad output capacitor C13 plays an important role in determining the magnitude of the high frequency response. Above 3KC, C13 becomes resistive with R5 (approximately 0.1Ω). Minimum DC level impedance is 0.25Ω and as a practical matter will not get much lower than that below 200KC with normal (0.01 – 20 microfarad) bypassing on the logic cards. C13 thus becomes the "load" at the higher frequencies and serves to desensitize the open loop response to variations in actual load impedance. C13 is chosen a wet-slug tantalum which has fairly predictable series resistance characteristics. R9 assures a minimum load current of 185 ma.

The high frequency open loop gain is further controlled by local "Miller" feedback around Q1 via C21 and R36, making the high frequency transimpedance of Q1 independent of beta. In addition, the negative feedback lowers the output impedance of the Q1 stage, which serves to broad-band the Q2-Q4 output transistors. R36 introduces a "zero" at 60 KC and above that, the gain roll-off comes from the transistors (primarily Q2-Q4, which have a low f_t). C20 introduces a "zero" at 300 KC to give additional phase margin.

To summarize, the high frequency open loop gain characteristics of the power amp are determined largely by the fixed elements employed, rather than the transistor parameters; and since the closed loop bandwidth of this stage is much higher than that of the primary voltage control loop, variations in actual gain crossover frequency (attendant with temperature dependence of C13's series resistance) will not affect overall operation of the regulator.

3.1 VOLTAGE CONTROL LOOP

The 723's error amp is a single differential pair (biased at 160 microamps each) driving the double emitter follower pair shown on the schematic; minimum DC voltage gain will be 1000 (B = 18). Zener diode CR5 assures sufficient collector-base bias for the input pair over the temperature range. The combination of R5 and CR4 limit the maximum 723 output current to a safe value: loss of +12 volt power to the output amp causes the 723 to attempt to drive the load through R32, as opposed to AC coupling R32. The clamp transistor (pins 2 and 3) is for over-current protection and is normally cut off.

3.2 FREQUENCY RESPONSE

The closed loop bandwidth of the voltage control loop is 10KC and is again determined by fixed elements. C18 sets the AC gain in the 100 cps – 60KC range (gm of the input pair is relatively fixed) since the power amp and sense amp are broad band. R29 introduces a "zero" at 60KC which roughly matches the pole at 100KC from the power amplifier. C19 provides roll-off above 500KC. The resultant curve thus has a constant 6 db/octave roll-off for at least a decade above and below gain crossover, to yield plenty of phase margin in the face of small variations introduced by component tolerances, input amplifier bias current, and power amplifier frequency response.

The following is true of the measured output impedance vs. frequency from 1KC on up. At the lower frequencies, the decreasing reactance of C13 is offset by the falling loop gain (in both loops) so the curve is fairly flat; above 10KC the impedance rises to 0.1Ω (the series R of C13) as the power amp runs out of loop gain. At frequencies below 1kC the output impedance will be much lower (theoretically $0.02 \times 10^{-3}\Omega$ at 10 CPS with minimum beta transistors) and will be determined largely by the resistance of current traces leading from the remote voltage sensing point.

4.0 OVER CURRENT PROTECTION

The +5 regulator is protected against load faults by an over current detect circuit which latches the 723 output to zero volts for current surges lasting longer than 100 microseconds. When the fault is removed, the +5 output can be restored by turning AC power switch Off and then On.

During that course of the design, current fold-back circuitry was implemented. It was determined, however, that some *transient* fault conditions can result in instantaneous over voltage transients; latching the output to zero was felt to be a safer approach, and therefore subsequently implemented.

4.1 CIRCUIT DETAILS

The current through each output transistor is sensed via R4, R5, R6 voltage drops, and applied to differential amplifier U3A via the R37, R38, R39 summing resistors. The gain setting resistors R45, R46, R47 are chosen to yield 5 volts output for 21 amps output current (the values depart from ideal due to I-R drops on the circuit board and the position of R47 sense lead). The amplifier output is filtered via R44 and C22 (τ = 500 microseconds) and applied to the input of comparator U3B. The reference for this comparator is the 5.0 volts output voltage reference at R10. For input voltages less than 5 volts, the comparator output is low (< 0.5 volt); for inputs above 5.0 volts (> 21.5 amps) the U3B output swings positive, coupling positive feedback to the input via CR12 and R42; the output thus drives itself to the +20 volt supply. Should the input signal return below 5 volts, the output stays latched at +20 volts. Dividers R41 and R28 apply the comparator signal to the 723's clamp transistor; clamping occurs nominally at an 8.5 volt comparator output.

Experimentally, the output current transient following the application of a short circuit is a pulse, peaking at 40 amps and lasting about 100 seconds. C22 was chosen to be the largest value that did not increase the pulse duration.

5.0 OVERVOLTAGE PROTECTION

The regulated +5 volt output is protected against overvoltage conditions which could damage TTL logic. Such conditions could arise from component failure within the regulator, or accidental short circuits while servicing.

A sensing amplifier compares the output voltage to an independent 6.2 volt reference, and triggers an SCR crowbar circuit when overvoltage occurs. The crowbar instantly clamps the output to ground via a power rectifier diode, and in the longer term interrupts the power to the power amplifier by blowing the 25 amp secondary fuse. This latter step is necessary to limit the power dissipation in the crowbar itself, since the currents attendant with collector-base shorts in the output stage can be enormous.

5.1 CIRCUITRY

Transistor Q5 compares the +5 volt output on the regulator board to the 5.62 $\pm$5% reference provided by CR3. R13 and C8 provide filtering for transients lasting less than 1 microsecond. For voltages above 6.2 volts (nominal), Q5 conducts, triggering the triac amplifier SCR2 at about 2 ma. The triac in turn quickly shorts R1 to the +20 volt supply delivering the 100 ma of current necessary to trigger the crowbar SCR1. C7 is for speedup and provides 1.5 amp instantaneous trigger current to assure uniform current flow within the SCR.

Once triggered, the SCR1 anode current builds up rapidly and anode voltage drops to 2 volts. CR15 is now forward biased, and clamps the regulator output at 3.5 volts. R7 protects the SCR by limiting the average current to 70 – 90 amps (depending on line voltage), and the 25 amp fuse blows after 0.6 second (±50%) nominally.

Typical dynamic performance following application of a direct short from +12 to the regulator output is that the overvoltage circuit will respond within 3 microseconds to limit the maximum output voltage rise to 7.0 volts; thus the output voltage is greater than 5.0 volts for less than 10 microseconds total.

6.0 THERMAL DESIGN DATA

The power amp output transistors Q2-Q4 are mounted directly to the head sink using Wakefield 120 Thermal compound. The heat sink runs at 12 volts DC, avoiding the requirement for insulating washers. This saves up to 16°C on maximum junction temperature, and a more reliable thermal contact is established.

The worst case power dissipation for the output transistors occurs at hi-line 60 Hz with the unregulated filter capacitor C17 at its maximum value. Total worst case dissipation at 20 amps is 111 watts, but due to possible current unbalance the power handled by an individual device could be 8% above the average for the three. Also note that at hi-line *50 Hz,* the dissipation is only 1 – 2% lower than 60 Hz; 50 Hz will be the worst case cooling situation if fan output is frequency dependent.

7.0 +12 VOLT UNREGULATED SUPPLY

The +12 volt unregulated supply provides the DC power to the +5 volt regulator power amplifier, which in turn controls the flow of power to the logic board load. The transformer center-tapped secondary voltage is full-wave rectified by power rectifier diodes CR1 and CR2 and filtered by the 80K microfarad (+80 −10%) capacitor C17. Power output to the regulator is taken through the 25 amp fuse.

Rectifier dissipation at 20 amps load is 15 watts each, worst case; allowing 1.7°C/W from junction to heat sink, the maximum allowed heat sink temperature for 170° junction is 140°C at 20 amps.

The power transformer has a 12:43:1 primary-secondary turns ratio, and at 25°C has an equivalent secondary resistance of 13 mΩ for each leg (3 mΩ reflected from primary). Allowing 80° winding temperature rise, transformer I -R dissipation will be 13 watts maximum at 20 amps.

8.0 −20 VOLT UNREGULATED SUPPLY

The −20 volt unregulated supply provides unregulated power to the Device Controller logic board via the Power Distribution board. Nominal load current taken from this supply is 115 ma.

CR16, CR17 and C15, C3 comprise the negative voltage doubler operating from one side of the transformer secondary.

9.0 +20 VOLT UNREGULATED SUPPLY

The +20 volt unregulated supply is used to power the 723 regulator chip, the LM 320 op-amp, and the overvoltage trigger circuit. Nominal load current is 25 ma.

The circuit comprising CR6, CR8, C4, and C6 is identical to that for the −20 volt supply.

10.0 −12 VOLT UNREGULATED SUPPLY

The −12 volt unregulated supply provides power to the −5 volt regulator for distribution to the Device Controller board. Nominal load current is 310 ma. CR7 and CR9 full wave rectify the transformer output and C5 provides filtering.

11.0 −5 VOLT REGULATOR

The −5 volt regulator is an LM 320K T03 package mounted on the heat sink, providing an output of −5 volts ±5%. This device is short-circuit proof and contains internal overtemperature shut down. At 500 ma, maximum allowed heat sink temperature is 115°C, based on T_j maximum of 125°C and 3.8°C/W thermal resistance (0.8°C/W for insulating washer).

12.0 POWER-ON CIRCUIT

In addition to the regulated and unregulated output voltages, the Power Regulator board provides a Power-On logic signal output (PON) to the logic cards to provide initialization during power up/down sequencing.

At power turn-on, an internal time delay keeps PON low until 150 msec (nominal) after the +5 volt output has stabilized. At power turn-off PON goes low when the −5 volt regulator output drops, typically 6 msec before the loss of +5 volts. At very low input line voltage (brown-out) PON goes low whenever the 5 volt regulator output drops more than 0.25 volts below the reference (loss of regulation) or when the −5 volt output drops below 4.0 volts ±0.5; the line voltage at which this occurs depends on the 5 volt DC load current being taken (number of boards in controller), but is typically 92 VAC with a 20 amp load.

12.1 CIRCUIT OPERATION

Differential amplifier U3C compares the +5 volt output (sensed by R14) to a voltage that is 5% less than the 5 volt regulator reference (via the R15 − R48 divider). Pin 8 will be low as long as the 5 volt output exceeds the divided reference. Should the +5 output drop more than 0.25 volt below the reference, pin 8 swings rapidly high to the +20 volt supply, charging C9 through CR10. If the loss of regulation is due to low line, the +5 output will go in and out of regulation on the peaks and valleys of the +12 volt ripple. CR11 connects C9 as an integrating capacitor for negative-going excursions of pin 8, so that pin 8 stays high despite the ripple. R16 provides 0.1 volt hysteresis to assure clean hi-to-low transition at pin 8 as the line voltage is restored.

At power turn-on, the reference voltage comes up before the +5 output, so that U3 pin 8 comes on high. After regulation is achieved, pin 8 ramps to its low state via the C9 integration delay (150 ms typical).

The turn-on delay circuit is interfaced to a TTL logic level by transistor Q6 and R20. R19 and R18 bias the base slightly negative, but R18 turns Q6 on in the event of loss of −5 volts. CR13 and CR14 protect pin 8 from being pulled negative (op-amp requirement).

APPENDIX I
OUTPUT SPECIFICATIONS

+5 Volts regulated	−0 to 20 amps
Voltage accuracy:	±1% — adjustable
Ripple and noise:	less than 1 millivolt RMS
Output impedance:	less than 1 mv/amp
Line regulation:	less than 10 mvolts change, hi to low line
Current limit:	shut down protected at 23 amps ±2 amps
Overvoltage:	crowbar clamp at 6.2 volts ±0.2 volt
Remote voltage sense:	when used with 13037-60027
−5 Volts regulated	−0 to 350 ma
Voltage accuracy:	±5%
Ripple and noise:	less than 5 mv RMS
Output impedance:	less than 70 mΩ
Line regulation:	less than 20 mv change, hi to low line
−20 Volts unregulated	0 − 150 ma
DC output voltage:	18 volts nominal at 120 ma (nominal line)
Output impedance:	50 volts/amp
Ripple:	3.1 volts pp at 150 ma (lower line — 50 CPS)

PON — A logic signal to initialize remote logic at power turn-on; transistor to ground with 1K pull-up. Low, until 60 msec ±40 msec after +5 volts stabilizes at power turn-on.

APPENDIX II
TROUBLESHOOTING AIDS AT TURN-ON

1. Secondary Fuse Blows

It is suggested at this point that an external +7 volt power supply be used to supply +12 unregulated power. Disconnect fuse, and connect external +7 volts to heat sink side of fuse clip, and set *current* limit to 300 ma. This will save a lot of fuses while you are fixing the problem.

Ground the gate of SCR1 with a clip lead and see if +5 output really does go above 6 volts. If not, the problem is in the overvoltage circuit.

A. Overvoltage Circuit Problems

Check the CR3 zener voltage. Look carefully to see that SCR2 and Q1 are loaded correctly.

B. Overvoltage Really Occurring

First, verify that CR4 and CR15 are loaded correctly and the +20v is okay. Then, disable Q5 with a clip lead from base to ground; this disables the overvoltage clamp. Now check that the reference voltage at pin 5 of U2 is 5.0 volts ±0.5 volt.

If it's okay, place a short from U2 pin 13 to ground (available at R29-CR4 anode). Verify that voltage drop across R5 is less than 50 millivolts. If it isn't, CR4 is marked backwards or U2 is faulty.

If that looks okay, check Q7 base voltage. It should be less than 10 mv; if not, Q7 is faulty. If Q7 base is zero, verify that +5 output is less than 0.5 volt. If it is, proceed to next paragraph; if it isn't, check V_{be} of Q1 (across R40).

If it isn't less than 0.2 volt, look for faulty Q7 or shorted C23 or C21. If Q1 looks okay, determine which of Q2, Q3, or Q4 is carrying current by measuring the drop across R4, R6, and R8. If all three are on, look for external shorts and then replace Q1. If just one is on, replace it. If none are on, the problem is CR15. Note: A likely problem to occur is shorts from burrs or shavings in the transistor mounting holes on heat sink.

If +5 volt output is less than 0.5 volt with a short introduced at U2 pin 11, check error amp U3D as follows.

Remove shorts at U2 pins 11 and 13 and let the +5 output rise to the 7 volt limit of the external supply. Verify that the voltage difference from +5 output to U3 pin 14 (and U2 pin 4) is less than 50 millivolts. If not, check R21-R24 before replacing U3. If error amp output looks okay, replace U2.

2. No +5 Output

First, check +12 volt fuse and the +20 supply; then verify that CL test point (U3 pin 7) is low. If CL is high, the problem is in the overcurrent circuit U3A and B. To verify this, short a clip lead from U2 pin 2 to ground; this should restore the +5 output. If it doesn't, trace the voltage through the regulator loop using techniques similar to those employed in section 1.

For example, a clip lead to ground at U2 pin 4 should cause the +5 output to limit on the unregulated supply. If it doesn't, check voltages at U2 pin 10 and the base of Q7 with the clip lead in place.

Alternately, check to see that the error amp output is zero when the output is zero.

3. PON Problems

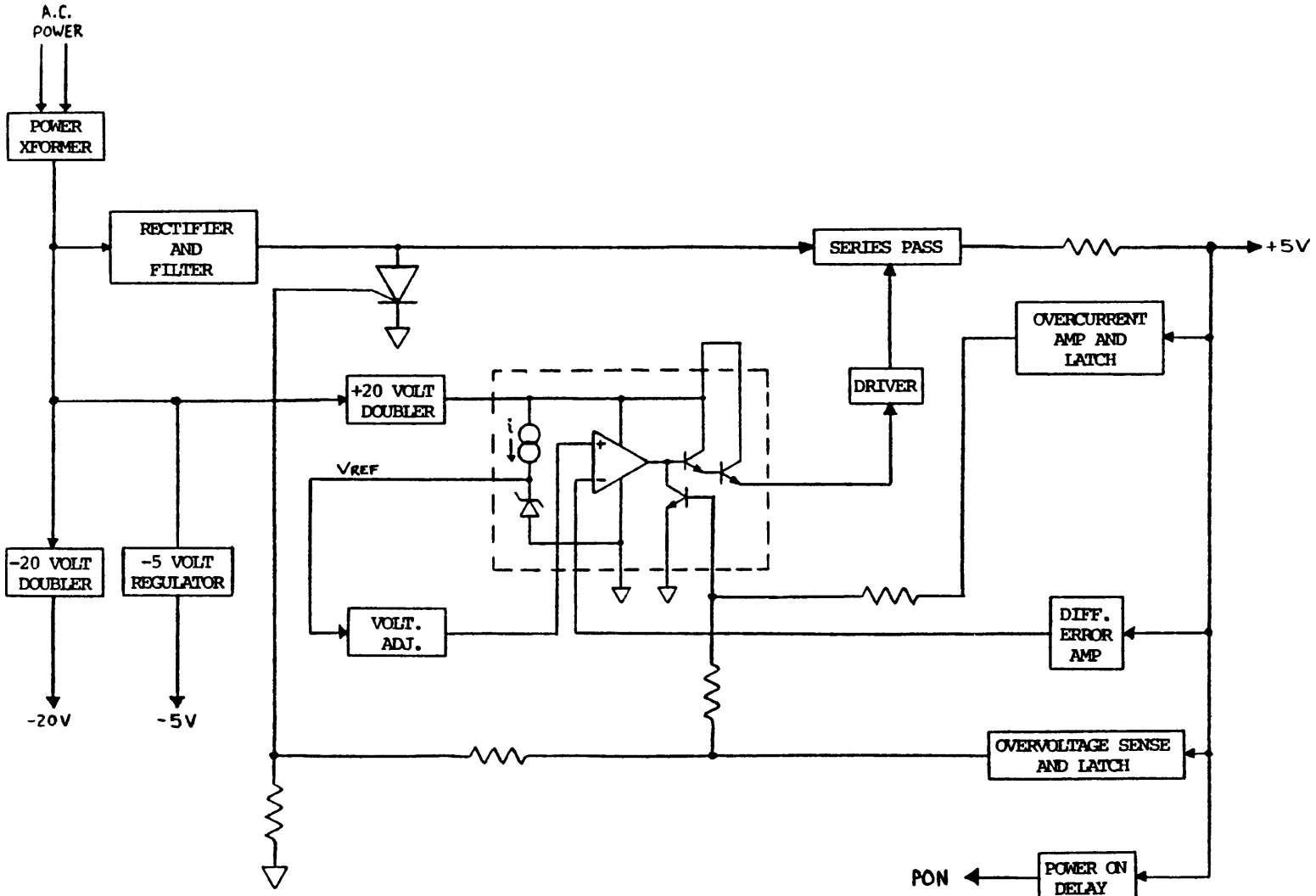
First, be sure +5 and −5 are okay.

A. PON Low All the Time

Verify that U3 pin 8 is low — it should be if the +5 volt regulator is working.

B. PON High All the Time

Check CR14 loading; check to see that U3 pin 8 is high at power turn-on and then ramps low (trigger scope from +5 start-up transient).



POWER SUPPLY BLOCK DIAGRAM

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60026
13037-66026
13037-68026

DATE CODE : D-2241

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C1	0180-0100	CAP 4.7UF 10%
C10	0160-2055	CAP .01UF-20+80%
C11	0160-0263	CAP .22UF 20%
C12	0160-4299	CAP 2200PF 20%
C13	0180-2338	CAP 650UF 20%
C14	0160-0263	CAP .22UF 20%
C15	0180-3206	CAP 470UF 35V
C16	0160-0263	CAP .22UF 20%
C18	0180-1743	CAP .1UF 10%
C19	0160-2055	CAP .01UF-20+80%
C2	0160-0127	CAP 1UF 20%
C20	0160-0575	CAP .047UF 20%
C21	0160-0575	CAP .047UF 20%
C22	0180-1743	CAP .1UF 10%
C23	0160-3466	CAP 100PF 10%
C3	0180-2373	CAP 580UF-10+150
C4	0180-3206	CAP 470UF 35V
C48	0698-3454	RES 215K 1%.125
C5	0180-3208	CAP. 1000UF 16V
C6	0180-2373	CAP 580UF-10+150
C7	0160-0574	CAP .022UF 20%
C8	0160-3456	CAP 1000PF 10%
C9	0160-0263	CAP .22UF 20%
CR1	1901-0318	DIODE
CR10	1901-0033	RECTIFIER SIL
CR11	1901-0033	RECTIFIER SIL
CR12	1901-0033	RECTIFIER SIL
CR13	1901-0033	RECTIFIER SIL
CR14	1901-0033	RECTIFIER SIL
CR15	1901-0416	DIODE
CR16	1901-0731	DIO-PWR RECT
CR17	1901-0731	DIO-PWR RECT
CR2	1901-0318	DIODE
CR3	1902-3104	DIODE BD 5.62V
CR4	1901-0033	RECTIFIER SIL
CR5	1902-3059	DIODE 3.83V
CR6	1901-0731	DIO-PWR RECT
CR7	1901-0731	DIO-PWR RECT
CR8	1901-0731	DIO-PWR RECT
CR9	1901-0731	DIO-PWR RECT
E1	0360-0124	CONN-SGL CONTACT
E2	0360-0124	CONN-SGL CONTACT
E3	0360-0124	CONN-SGL CONTACT
E4	0360-0124	CONN-SGL CONTACT
E5	0360-0124	CONN-SGL CONTACT
E6	0360-0124	CONN-SGL CONTACT
J1	1251-3852	CONN POST 15 F

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60026
13037-66026
13037-68026

DATE CODE : D-2241

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
Q1	1853-0305	XSTR 2N5875 TO3
Q2	1854-0519	XSTR 2N3772 TO3
Q3	1854-0519	XSTR 2N3772 TO3
Q4	1854-0519	XSTR 2N3772 TO3
Q5	1854-0215	XSTR 2N3904 PL5
Q6	1854-0215	XSTR 2N3904 PL5
Q7	1854-0013	XSTR 2N2218A TO5
R1	0698-3628	RES 220 5% 2W
R10	2100-3351	RES VAR 500 OHM
R11	0757-0280	RES 1K 1%.125
R12	0757-0280	RES 1K 1%.125
R13	0757-0280	RES 1K 1%.125
R14	0757-0442	RES 10K 1%.125
R15	0757-0442	RES 10K 1%.125
R16	0683-1855	RES 1.8M 5% .25W
R17	0757-0442	RES 10K 1%.125
R18	0757-0442	RES 10K 1%.125
R19	0757-0438	RES 5.11K 1%.125
R2	0757-0873	RES 1.62K 1% .50
R20	0757-0280	RES 1K 1%.125
R21	0757-0438	RES 5.11K 1%.125
R22	0757-0438	RES 5.11K 1%.125
R23	0757-0438	RES 5.11K 1%.125
R24	0757-0438	RES 5.11K 1%.125
R25	0757-0280	RES 1K 1%.125
R26	0698-3151	RES 2.87K 1%.125
R27	0757-0424	RES 1.1K 1%.125
R28	0698-3155	RES 4.64K 1%.125
R29	0698-3432	RES 26.1 1%
R3	0757-0198	RES 100 1% .50
R30	0757-0461	RES 68.1K 1%.125
R31	0698-0082	RES 464 1%.125
R32	0757-0346	RES 10 1%.125
R33	0683-0275	RES 2.7 5% .25
R34	0683-0275	RES 2.7 5% .25
R35	0698-0082	RES 464 1%.125
R36	0757-0395	RES 56.2 1%.125
R37	0757-0444	RES 12.1K 1%.125
R38	0757-0444	RES 12.1K 1%.125
R39	0757-0444	RES 12.1K 1%.125
R4	0811-0659	RES .05 5% 5W PW
R40	0757-0401	RES 100 1%.125
R41	0757-0461	RES 68.1K 1%.125
R42	0757-0442	RES 10K 1%.125
R43	0757-0438	RES 5.11K 1%.125
R44	0757-0438	RES 5.11K 1%.125
R45	0757-0458	RES 51.1K 1%.125

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 13037-60026
13037-66026
13037-68026

DATE CODE : D-2241

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R46	0757-0458	RES 51.1K 1%.125
R47	0698-3558	RES 4.02K 1%.125
R49	0757-0438	RES 5.11K 1%.125
R5	0698-3634	RES 470 5% 2W
R6	0811-0659	RES .05 5% 5W PW
R7	0811-0659	RES .05 5% 5W PW
R8	0811-0659	RES .05 5% 5W PW
R9	0698-3611	RES 27 5% 2W MO
U1	1826-0202	IC V REG -5V
U2	1826-0049	IC 723 CERAMIC
U3	1826-0161	IC QUAD OP AMP

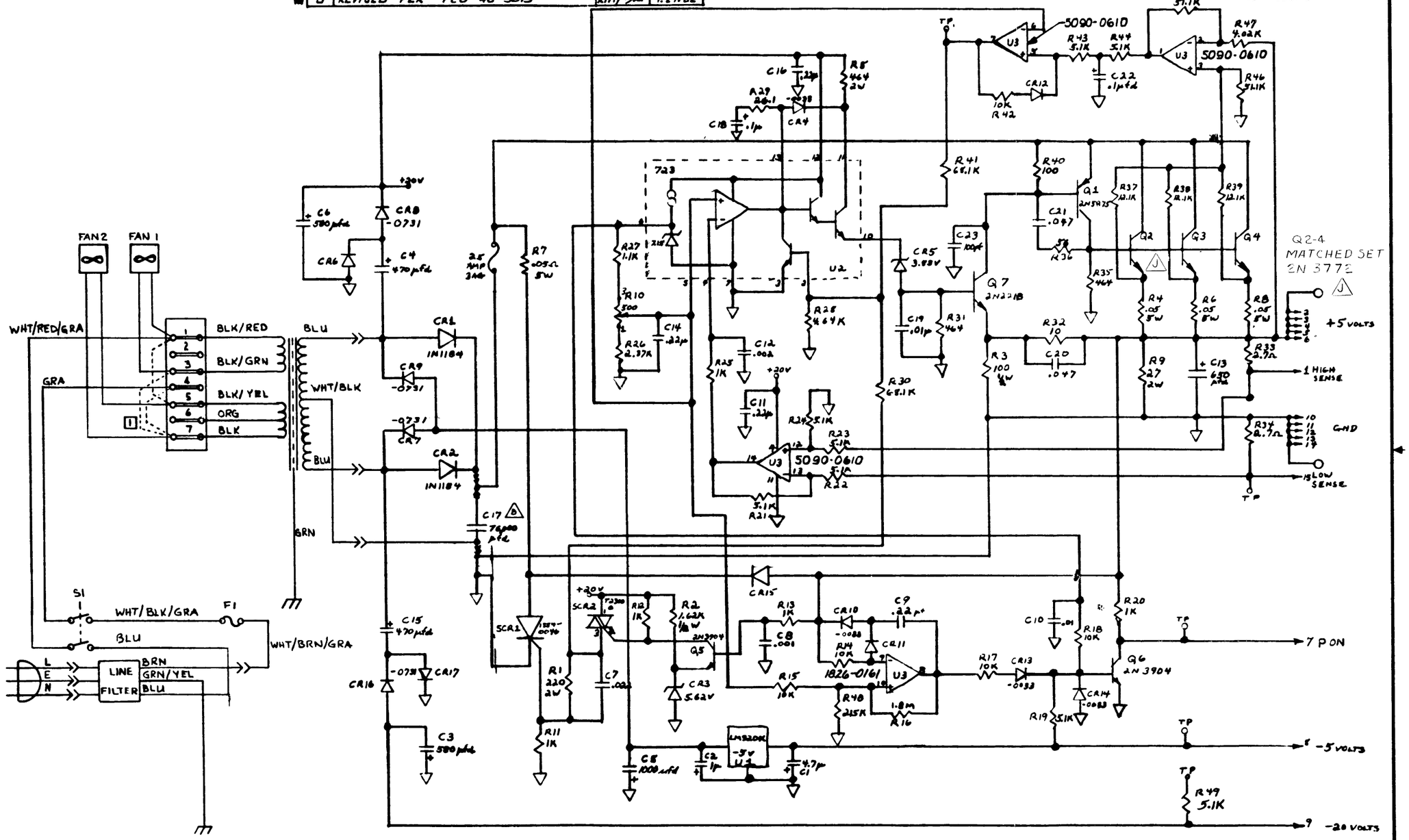
END OF MATERIAL LIST.

SYM	REVISIONS	APPROVED	DATE
H	CURRENT DATE CODE D-2241 PCO 48-5160	ME/DM	11-5-82
J	MATCHED SET XSTRS Q2-4 PER CO 48-1157	JJ/DM	12-12-84
D	REDRAWN INPUT PC 48-1733	K.F./DM	6.15.79
E	CURRENT DATE CODE B-2204 PCO 48-3648	K.F./DM	4.23.82
F	CURRENT DATE CODE C-2204 PCO 48-3977	K.F./DM	6.16.82
G	REVISED PER PCO 48-5013	K.F./	7.27.82

C-13037-60026-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PER PC48-0660	SR	6/29/77
B	CHANGED VALUE OF FILTER CAPACITOR PC48-0050 K1	K.LARSON	10-8-77
C	5090-0610 WAS 1826-0161 PC48-1130	TT/SR	12-18-78

CONT'D



NOTE:

[1] STRAPPED FOR 120V OPERATION (SEE C-13037-60031-51 FOR OTHER VOLTAGE INPUTS.)

DO NOT SCALE THIS DRAWING	DRAWN BY	12/2/76 DATE	POWER REGULATOR BD 13037 TITLE SCHEMATIC
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES .XX ± .02 .XXX ± .005 SEE CORP. STD. 608	ENGINEER	12/2/76	HEWLETT PACKARD
	RELEASED TO PROD.	6/29/77	NEXT ASSEMBLY: SEE WHERE USED
	SUPERSEDES DWG.		PART NUMBER: 13037-60026
			C-13037-60026-51

ENGINEERING RESPONSIBILITY — SEPIA

0	1	2	3	4		6		8	9	11	12	14	15	
16	17	21	19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	40	20									

F-13037-60026-1

SYM	REVISIONS	APPROVED	DATE
J	REVISED & REDRAWN PCO 48-3648	K.F.	4.23.82
K	BOARD REV WAS "B" PCO 48-3977	K.F.	6.16.82
L	REVISED PER PCO 48-3855	K.F.	7.27.82
M	REVISED PER PCO 48-5013	K.F.	7.29.82
N	REVISED PER P.C.O 48-5160	MEJ	11-5-82
P	REVISED PER PCO 48-5160A	MEJ	2-25-83
R	REV'D. PER PCO 48-0009	JJ	8-18-83
S	REVISED PER C048-0630	JJ	2-14-84
T	MATCH SET OF XSTRS PER C048-115"	JJ	12-12-84

CAUTION

HEAT SINK IS AT +12 VOLTS

DISTANCE BETWEEN REGISTRATION TARGETS 16.000 ± .003

SEE DETAIL A

TYP 32 PLCS

TYP 3 PLCS

TYP 2 PLCS

FARSIDE

PAD MASTER

TYP 3 PLCS

11-2-82

F-13037-80026-3

F-13037-80026-7
F-13037-80026-8

GRAPHICS-COMPONENT SIDE
TARGET MASTER

VIEW A-A

DETAIL A

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L PART NO.	MAT'L DWG. NO.	MAT'L SPEC.
29	1	LABEL-	7120-6830		
28	5	RIVET	0361-0662		
27	2	LUG CRIMP	0362-0539	REF.	7
26	A/R	INSUL. TUBING	0890-0334		
25	2	STANDOFF	0380-1085		
24	2	WASHER INT #8	2190-0009		
23	6	SCREW 8-32 X .312	2510-0101		
22	1	WIRE #12AWG RED	8150-2154	REF.	7
21	10	NUT SELF-LOCK 6-32	2420-0001		
20	10	WASHER FLY #6	2190-0464		
19	10	SCREW 6-32 X .562	2360-0229		
18	6	LK WASHER #8	2190-0073		
17	5	WASHER FLAT	3050-0891		
16	2	INSULATOR XSTR	1200-0077		
15	2	WASHER INS.	1200-0088		
14	3	LK WASHER 1/4	2190-0740		
13	3	NUT 1/4-28	2950-0036		
12	1	WIRE #24AWG BLK.	8150-0447	REF.	7
11	1	WIRE #14 AWG GRN/YEL	8150-2624	REF.	
10	3	TERMINAL .250 TAB 1	0360-1263		
9	2	TERMINAL .250 TAB 2	0360-1264		
8	1	FUSE 25A	2110-0250		
7	2	FUSE CLIP	2110-0551		
6	1	CONNECTOR 15 PIN F. JI	1251-3852		
5	A/R	COMPOUND THERMAL	6040-0239		
4	1	INSULATOR H.S.	13037-00007		
3	1	HEAT SINK	13037-20005		
2	6	CONN-5GL CONTACT	0360-0174		
1	1	PC B, ETCHED	13037-80026		

NOTES:

11-2-82

11-2-82

1. UNLESS OTHERWISE SPECIFIED ALL:
   RESISTANCE IN OHMS.
   ALL RESISTORS 1/4W, 1% MF.
   ALL CAPACITANCE IS IN MICROFARADS.
2. MARK ASSEMBLY DATE CODE 2241
3. PC PRODUCTION: MARK ASSEMBLY WORK ORDER.
4. SEE ASSEMBLY PROCEDURES A-13037-60026-2.
5. MASK PRIOR TO LOADING.
6. WIRE CONTAINED IN PWR REG WIRE PACK 13037-60041.
7. ITEMS (11), (12), (22) & (27) ARE ON M/L 13037-68041.

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L PART NO.
30	1	WIRE PACK - PWR REG	13037-60041

DRAWN BY	1-19-82	BOARD ASSEMBLY, REGULATOR, POWER	HEWLETT PACKARD
ENGINEER	6-18-82	TITLE	
RELEASE TO PROD.	6-18-82	SEE WHERE USED	13037-60026
D-13037-60026-1	5-8-77	NEXT ASSEMBLY	PART NUMBER
SUPERSEDES DWG. REV. G.		FINISH —— SCALE 2:1	F-13037-60026-1

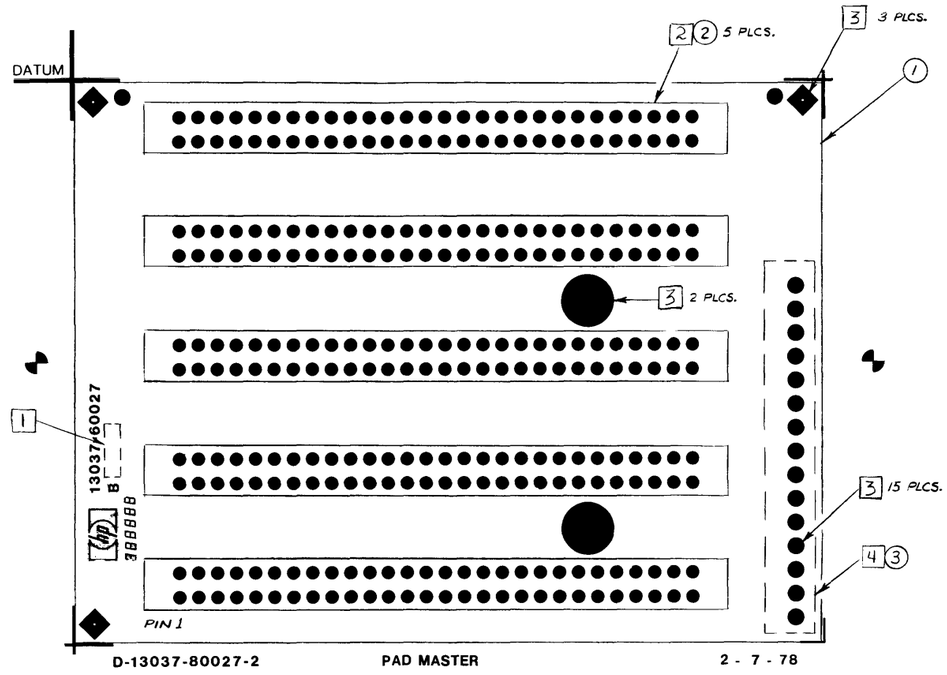
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 6 8 9 11 12 14 15	
16 17 19 21 22 23 25 29 30 32 35 38 43	
45 48 61 63 65	

D-13037-60027-1

SYM	REVISIONS	APPROVED	DATE
C	REDRAWN PER PCH8-0631	L.O.LEE	6-23-78

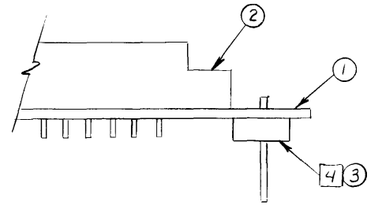
DISTANCE BETWEEN TOOLING REGISTRATION HOLES 5 . 500 ±.005



D-13037-80027-2 PAD MASTER 2 - 7 - 78

NOTES:

1. OPR. 264 , MARK ASSEMBLY DATE CODE 1735
2. OPR. 265 ; INSTALL ITEMS (2)
3. OPR. 265 ; MASK PRIOR TO LOADING.
4. OPR. 266 ; TOUCH UP, INSTALL ITEMS (3)



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
3	1	CONNECTOR, 15 PIN	1251-3243		
2	5	CONNECTOR, 56 PIN	1251-3856		
1	1	BOARD, ETCHED	13037-80027		

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

TITLE PWR. INTERCONNECT BD. ASSLY. DRAWING

NEXT ASSEMBLY SEE KARDEX

FINISH

SCALE 2x

HEWLETT PACKARD

PART NUMBER 13037-60027

D-13037-60027-1

CONTENTS

Page

Introduction 8-1
External Addresses 8-2
External Flags 8-2
Disc and Interface Commands 8-3
Register Assignments 8-4
Constants 8-5
Power On Clear, Time-Out Processor 8-6
Poll Loop 8-7
Set Attention and Interrupt 8-8
Command Formats 8-9
Obtaining Command and Executing Branch Vector 8-10
WAKEUP, COLD LOAD READ (BOOT) Commands 8-11
RECALIBRATE, SEEK Commands, SEEK1, SEEK2, SEEK3 8-12
ADDRESS RECORD Command, TERM, RCORD 8-13
STATUS Command Formats 8-14
STATUS Command 8-14
Subroutine GDTYP 8-15
REQUEST SECTOR Command 8-16
READ, RNVFY Commands, Subroutines DSTRT, DSTR1, CKXFR, REDE1 8-17
Subroutines VCHK, CLROF; Retryable Error Status Sieve 8-18
READ WITH OFFSET Command 8-19
VERIFY Command, Subroutines VRFY, VRFY1, VRFY2, READ3 8-20
Subroutines VRFY, VRFY1, VRFY2 8-21
READ FULL SECTOR Command 8-22
INITIALIZE Command 8-23
Write One Sector Subroutine 8-24
Write One Sector Subroutine, EWRFS, CKWRT 8-25
WRITE Command, Subroutines WSTA1, WSTA2 8-26
WRITE FULL SECTOR, LOAD TIO Commands 8-27
REQUEST SYNDROME Command 8-28
SET FILE MASK, CLEAR Commands 8-31
REQUEST DISC ADDRESS Command, Subroutine PUT 8-32
Drive Number Verification and Select Routine 8-33
Track Sparing Routine 8-35
Increment Head-Sector 8-37
Subroutines: INCHS, SECTR 8-38
Subroutines: DECS, DECS2 8-39
Subroutines: SWAIT, GSTAT, SWAT3, CST 8-40
Subroutines: SETUP, BSYST, FLUSH, STPCL, SRQ, IFDSC, IFSEL 8-41
Subroutines: ICLCK, DISCO, STROB, CLRST 8-42
Subroutines: GET, PRFCH, WTIO, TRNOF, BSYCL 8-43
Subroutines: STRT1, STRT2, INCS 8-44
Subroutines: SBTCK, USTAT, Controller Error Status Sieve 8-45
Appendix I: Microassembler Instruction Description 8-47
Appendix II: Label Call Addresses 8-51

LABEL CROSS REFERENCE

Label	Page
ACMOD	8-30
ACRER	8-45
ADJX	8-30
ATTN1	8-8
ATTN2	8-8
ATTN3	8-8
ATTN4	8-8
BOOT	8-11
BSYCL	8-43
BSYER	8-45
BSYST	8-41
CDERI	8-29
CDTER	8-18
CKWRT	8-25
CKXFR	8-17
CLHLD	8-6
CLOOP	8-29
CLR	8-31
CLRAM	8-6
CLROF	8-18
CLRST	8-42
CLR1	8-6
CMDWT	8-8
CMDW1	8-8
COMP1	8-29
COMP2	8-29
COMP3	8-30
CST	8-40
CVECT	8-10
CYLER	8-36
CYLRT	8-36
CYLR1	8-36
CYLR2	8-45
DECS	8-39
DECS1	8-39
DECS2	8-39
DECS3	8-39
DEFER	8-45
DFLST	8-32
DFTRK	8-36
DFTR1	8-36
DISCO	8-42
DRVOK	8-34
DSTRT	8-17
DSTR1	8-17
DTERR	8-35
DTER2	8-35
DVECT	8-15
EOCER	8-45
EWRFS	8-25
EWRF1	8-25
EXEC	8-10
EXEC1	8-10
EXEC2	8-10
FLUSH	8-41
GDTYP	8-15
GET	8-43
GET1	8-43
GSTAT	8-40
GTPAT	8-30
HSER	8-36
HSER1	8-45
ICLK	8-42
ICLK1	8-42
ICLK2	8-42
ICLK3	8-42
IFDSC	8-41
IFSEL	8-41
ILLGL	8-10
INCHS	8-38
INCS	8-44
INCS1	8-40
INIT	8-23
INIT1	8-23
INIT2	8-23
INIT3	8-23
INIT4	8-23
INTRP	8-31
IOPER	8-45
LAST	8-44
LTIO	8-27
MOREC	8-29
MOREP	8-29
NDERR	8-14
NRTER	8-18
NTEQL	8-6
NTLST	8-44
NXTAD	8-6
OPCER	8-45
OUTAD	8-44
OUTA1	8-44
OUTA2	8-44
OUTSC	8-44
OVERR	8-18
PLOOP	8-29
POLL	8-7
POLL1	8-7
POLL2	8-7
POLL3	8-7
PRFCH	8-43
PUT	8-32
PUT1	8-32
PWRON	8-6
RBOOT	8-17
RCORD	8-13
READ	8-17
READ1	8-17
READ2	8-17
READ3	8-21
RECAL	8-12
RECRD	8-13
REDE1	8-17
REQAD	8-32
RFDAT	8-22
RFS	8-22
RFULL	8-22
RNVFY	8-17
ROFST	8-19
ROFS1	8-19
ROFS2	8-19
ROFS3	8-19
RQAD1	8-32
RQAD2	8-32
RQAD3	8-32
RQSCT	8-16
RQSC1	8-16
RQSC2	8-16
RQSC3	8-16
RQSC4	8-16
RQSC5	8-16
RQSYN	8-29
SBTCK	8-45
SECTR	8-38
SEEK	8-12
SEEK1	8-12
SEEK2	8-12
SEEK3	8-12
SETUP	8-41
SFMSK	8-31
SHFTX	8-30
SPARE	8-35
SPAR1	8-36
SPER	8-45
SRQ	8-41
STATS	8-14
STER	8-45
STPCL	8-41
STPC1	8-41
STRB1	8-42
STRB2	8-42
STROB	8-42
STRT1	8-44
STRT2	8-44
STRT3	8-44
SURFC	8-38
SVRAM	8-34
SWAIT	8-40
SWAT1	8-40
SWAT2	8-40
SWAT3	8-40
TERM	8-13
TRNOF	8-43
UDTER	8-18
UNIT	8-34
UNIT1	8-34
UNIT2	8-34
USTAT	8-45
VCHK	8-18
VCYLD	8-21
VDATA	8-21
VDTA1	8-21
VERWD	8-21
VHSAD	8-21
VLOOP	8-20
VRFCM	8-20
VRFY	8-21
VRFY1	8-21
VRFY2	8-21
VRFY3	8-21
VSYNC	8-21
WAKUP	8-11
WCYLD	8-24
WDATA	8-24
WDTA2	8-24
WFDAT	8-27
WFS	8-27
WFSYN	8-27
WFULL	8-27
WFWAT	8-27
WFWA2	8-27
WHSAD	8-24
WLOOP	8-30
WPER	8-45
WRITE	8-26
WRLWD	8-25
WRONE	8-24
WRTOK	8-26
WSTA1	8-26
WSTA2	8-26
WSYNC	8-24
WSYN1	8-24
WTATN	8-18
WTEWD	8-25
WTIO	8-43
WTIO1	8-43

```
1
2               /
3               /
4               /
5               /
6               /
7               /
8               /
9               /
10              /
11              /
12              /              1       333333      0000 0    333333    777777777
13              /            11      3       3    0    0    3       3           7
14              /           1 1              3   0     0 0           3          7
15              /          1  1              3   0    0  0           3         7
16              /             1        33333    0    0   0     33333         7
17              /             1              3   0  0    0           3       7
18              /             1              3   0  0    0           3      7
19              /             1              3   0 0     0           3     7
20              /             1      3       3    0     0    3       3    7
21              /           1111111    333333    0 0000      333333    7
22              /
23              /
24              /
25              /
26              /
27              /       CCCCC    N       N   TTTTTTTTT RRRRRR     L           RRRRRR
28              /      C     C   N       N       T     R     RR   L           R     RR
29              /     C          NN      N       T     R       R  L           R       R
30              /     C          N N     N       T     R     RR   L           R     RR
31              /     C          N  N    N       T     RRRRRR     L           RRRRRR
32              /     C          N   N   N       T     R  R       L           R  R
33              /     C          N    N  N       T     R   R      L           R   R
34              /     C          N     NN       T     R    R     L           R    R
35              /      C     C   N      N       T     R     R    L           R     R
36              /       CCCCC    N      N       T     R      R   LLLLLLLLL   R      R
37              /
38              /
39              /    ************************************************************
40              /    * (C) COPYRIGHT HEWLETT-PACKARD COMPANY 1978.  ALL RIGHTS    *
41              /    * RESERVED   NO PART OF THIS PROGRAM MAY BE PHOTOCOPIED,     *
42              /    * REPRODUCED OR TRANSLATED TO ANOTHER PROGRAM LANGUAGE WITHOUT *
43              /    * THE PRIOR WRITTEN CONSENT OF HEWLETT-PACKARD COMPANY      *
44              /    ************************************************************
```

INTRODUCTION

```
45
46              /
47              /
48              /
49              /
50              /    THIS MICROPROGRAM CONTROLS THE OPERATION OF THE 13037  EXPANDED
51              /  CAPACITY DISC CONTROLLER.  THE PROGRAM SUPPORTS OPERATION IN
52              /  EITHER A 3000 OR 2100 CPU ENVIRONMENT
53              /    CONTROLLER ARCHITECTURE IS SUCH THAT ANY ONE OF 8 CPU'S CAN
54              /  ADDRESS ANY ONE OF 11 DISC DRIVES   THE CPU CAN, UNDER SOFTWARE
55              /  CONTROL, HOLD OR RELEASE ITS SELECTED DRIVE FOLLOWING COMPLETION
56              /  OF THE CURRENT DISC OPERATION.  WHILE A CPU HOLDS A DRIVE, NO
57              /  OTHER CPU MAY ACCESS IT   SUBJECT TO THIS RESTRICTION, OVERLAPPING
58              /  SEEKS ARE SUPPORTED BY THIS CONTROLLER
59              /    DRIVE ATTENTION BITS ARE SET WHENEVER A SEEK COMPLETES, WHEN
60              /  THE DRIVE IS LOADED OR UNLOADED, OR WHEN THE DRIVE FAULTS.
61              /  DURING A CONTROLLER WAIT LOOP, THE DRIVES ARE POLLED TO CHECK
62              /  THESE BITS.  THE LOWEST-NUMBERED DRIVE WHOSE ATTENTION BIT IS
63              /  SET GENERATES A CPU INTERRUPT
64              /    CPU ADDRESSING IS SIMILAR WHEN CHECKING FOR A PENDING COMMAND,
65              /  EXCEPT THAT THE CPU'S ARE POLLED STARTING WITH THE NEXT CPU ABOVE
66              /  THE ONE WHOSE COMMAND HAS JUST COMPLETED (INSTEAD OF STARTING WITH
67              /  CPU 0).  THIS REQUIRES A HARDWARE MEMORY, BUT INSURES THAT HIGHER-
68              /  NUMBERED CPU'S WILL NOT BE SHUT OUT BECAUSE OF MULTIPLE OPERATIONS
69              /  ON LOWER-NUMBERED CPU'S
70              /    MICROPROGRAM STRUCTURE ASSUMES A 469 KWORD DISC TRANSFER RATE
71              /  (7.5 MHZ BIT RATE) AND A MICROINSTRUCTION CYCLE OF 200 NS.  THIS
72              /  ALLOWS A MAXIMUM OF 10 MICROINSTRUCTIONS BETWEEN EACH DISC WORD I-O.
```

```
                        EXTERNAL ADDRESSES
/
/
/
/
        EQU : CBSIN  <-   4          / COMMAND BUS INPUT BUFFER.
        EQU : CBUF   <-   2          / CONTROL BUS OUTPUT BUFFER.
        EQU : CLKOF  <-   5          / READ CLOCK OFFSET BUFFER.
        EQU : DSYNC  <-  25          / READ-DECODE ECC SYNCWORD MARK.
        EQU : ECICW  <-  20          / ECC INTERNAL CONTROL WORD
        EQU : EOC    <-  13          / END-OF-CYLINDER INDICATOR.
        EQU : ESYNC  <-  23          / WRITE-ENCODE ECC SYNCWORD MARK.
        EQU : FLMSK  <-  13          / CONTROLLER MODE (FILE) MASK:
                                     /   BIT 0 ==> ALLOW INCREMENTAL SEEK
                                     /  AT END OF PLATTER OR CYLINDER.
                                     /   BIT 1 ==> CYLINDER MODE (SET),
                                     /                PLATTER MODE (RESET)
                                     /   BIT 2 ==> ENABLE TRACK SPARING
        EQU : IDTBF  <-   3          / CPU INTERFACE DATA BUFFER
        EQU : IFNBF  <-   5          / CPU INTERFACE FUNCTION BUFFER.
        EQU : IFVLD  <-  14          / INTERFACE COMMAND VALIDATION CLOCK
        EQU : INITL  <-   6          / FLAG SET DURING INITIALIZE.
        EQU : INTCW  <-  11          / CONTROLLER INTERNAL CONTROL WORD
        EQU : NWTRK  <-   7          / NEW TRACK FLAG -- SET WHENEVER
                                     /   CONTROLLER SWITCHES TO NEW TRACK
        EQU : RAM    <-   1          / INTERFACE-CPU ASSOCIATION RAM (4X8)
        EQU : RAMAD  <-   0          / ADDRESS REGISTER FOR ABOVE RAM.
        EQU : RETRY  <-   6          / ADDRESS RECORD RETRY BIT (MID 0)
        EQU : SKDIR  <-   1          / AUTO SEEK DIRECTION FLAG, BIT 14:
                                     /   1 = DECREMENTAL SEEK,
                                     /   0 = INCREMENTAL SEEK.
        EQU : SPIBF  <-  16          / CONTROLLER <- SERIAL-PARALLEL CONVERTER.
        EQU : SPOBF  <-  15          / PARALLEL-SERIAL CONVERTER <- CONTROLLER.
        EQU : TGBUS  <-  10          / CONTROLLER-TO-DISC TAG BUS.
        EQU : TIMER  <-   1          / TIME-OUT CIRCUIT TO AVOID
                                     /   CONTROLLER HANG-UPS.
        EQU : WORD1  <-  26          / 1ST WORD OF ERROR PATTERN, MSB'S
        EQU : WORD2  <-  27          / 2ND WORD OF ERROR PATTERN, LSB'S
```

```
                        EXTERNAL FLAGS
/
/
/
/
        EQU : ACRDY  <-   4          / ACCESS READY (HEADS OVER VALID TRACK)
        EQU : ANYER  <-  13          / ANY DATA ERROR -- TRUE IF CSYN OR
                                     /   PSYN <> 0.
        EQU : AUTSK  <-  17          / AUTO INCR-DECR SEEK ENABLED
        EQU : BURST  <-  12          / C-LOOP CONTROL FLAG.
        EQU : CMRDY  <-   0          / COMMAND READY (AVAILABLE)
        EQU : CYSRF  <-  16          / CYLINDER MODE (1) OR SURFACE MODE (0)
        EQU : DTRDY  <-   1          / DATA READY (AVAILABLE)
        EQU : EOCF   <-  14          / "END-OF-CYLINDER" FLAG.
        EQU : EOD    <-   6          / END OF DATA TRANSFER.
        EQU : EOW    <-   2          / END OF DATA WORD
        EQU : INITF  <-  11          / SET DURING INIT, WFS, RFS TO
                                     /   PREVENT VRFY-SPARE WHEN
                                     /   SWITCHING TRACKS.
        EQU : INTOK  <-  10          / O.K. TO INTERRUPT CPU WITH
                                     /   DRIVE ATTENTION STATUS
        EQU : MATCH  <-  12          / P-LOOP CONTROL FLAG.
        EQU : NWTRF  <-   5          / NEW TRACK FLAG -- SET WHENEVER
                                     /   CONTROLLER SWITCHES TO NEW TRACK
        EQU : OVRUN  <-   7          / DATA OVERRUN.
        EQU : RTRYF  <-  11          / RETRY FLAG -- ALLOWS ONE SEEK
                                     /   TO LOGICAL ADDRESS WHEN AN
                                     /   ADDRESS ERROR IS DETECTED
        EQU : SPREN  <-  15          / TRACK SPARING ENABLED
        EQU : UNCOR  <-  20          / UNCORRECTABLE DATA ERROR -- TRUE
                                     /   IF CSYN OR PSYN = 0.
        EQU : XFRNG  <-   3          / 3000 I-O CHANNEL ERROR FLAG.
```

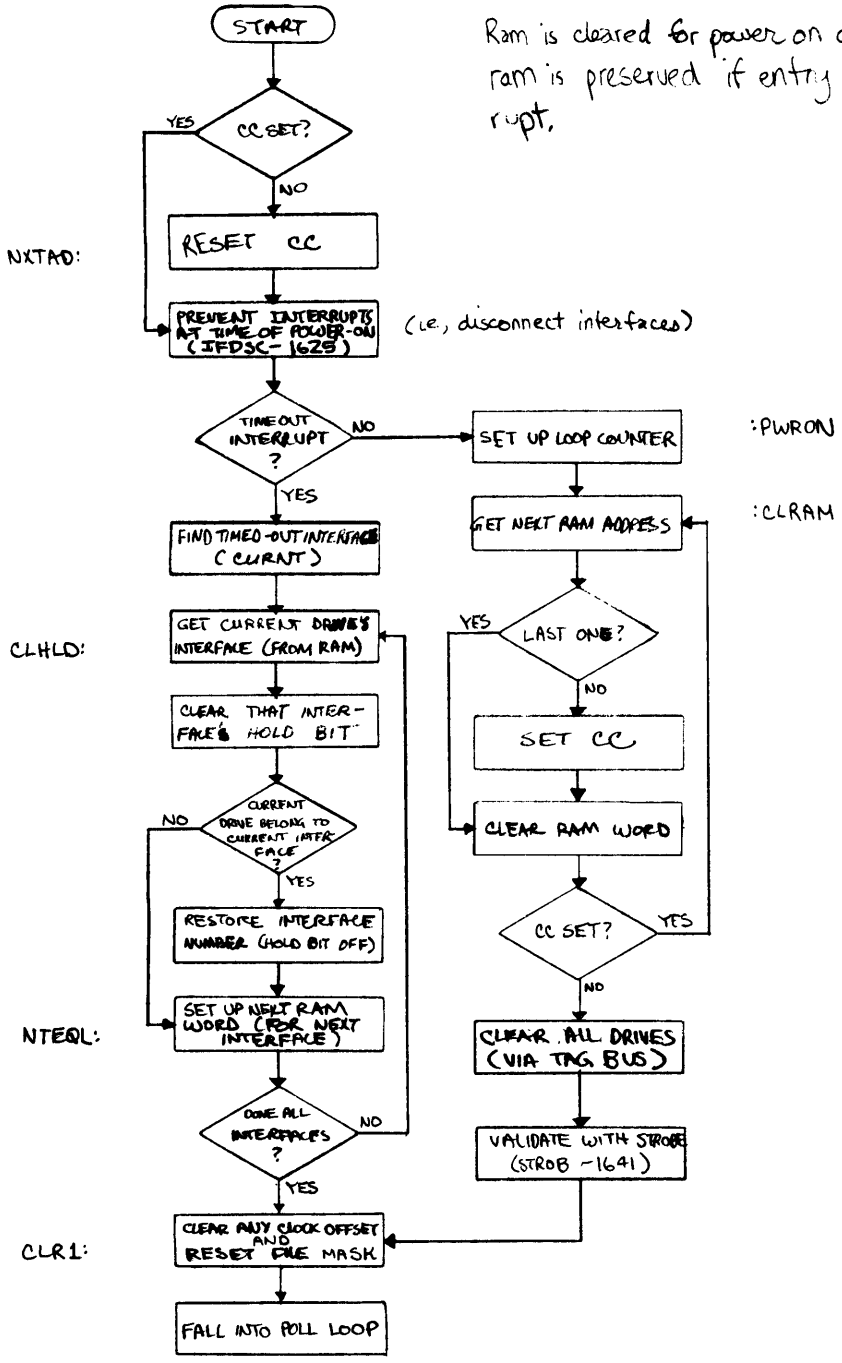
```
143                     DISC AND INTERFACE COMMANDS
144             /
145             /
146             /
147             /
148             /  DISC COMMANDS:
149             /  EQU VALUE SHOWN IS INVERTED FOR GROUND TRUE LOGIC
150             /
151                   EQU : ADREC  ←   6          / ADDRESS RECORD COMMAND
152                   EQU : CLRCM  ←   12         / CLEAR COMMAND
153                   EQU : CLST   ←   1          / CLEAR SELECTED STATUS.
154                   EQU : DCCOM  ←   13         / DISCONNECT COMMAND
155                   EQU : OFFST  ←   2          / CYLINDER OFFSET COMMAND.
156                   EQU : RCCOM  ←   4          / RECALIBRATE COMMAND
157                   EQU : RDCOM  ←   17         / READ COMMAND
158                   EQU : REQAT  ←   14         / REQUEST ATTENTION COMMAND
159                   EQU : RSCOM  ←   11         / REQUEST SECTOR ADDRESS COMMAND.
160                   EQU : SEEKC  ←   7          / SEEK COMMAND
161                   EQU : SLECT  ←   5          / SELECT COMMAND
162                   EQU : STATC  ←   15         / STATUS COMMAND
163                   EQU : WRTCM  ←   16         / WRITE COMMAND
164                   EQU : XSECT  ←   3          / TRANSMIT SECTOR COMMAND.
165             /
166             /
167             /  INTERFACE COMMANDS:
168             /  EQU VALUES SHOWN INCLUDE BITS TO ENABLE-DISABLE THE COMMAND AND
169             /  DATA BUS BUFFERS TO THE INTERFACE AS WELL AS BITS TO ENABLE THE
170             /  LINE DRIVERS OR RECEIVERS ON THE INTERFACE.
171             /
172             /
173             /        7 6  5 4 3  2 1 0
174             /        - -  - - -  - - -
175             /      ! E    E E F  F F F !
176             /      ! C    I I N  N N N !
177             /      ! D    D R 3  2 1 0 !
178             /        - -  - - -  - - -
179             /
180             /
181             /    WHERE ECD     = ENABLE CONTROLLER-INTERFACE DATA BUS DRIVERS.
182             /          EID     = ENABLE DATA BUS DRIVERS ON INTERFACE.
183             /          EIR     = ENABLE DATA AND COMMAND BUS RECEIVERS ON INTERFACE
184             /          FN3-FN0 = CONTROLLER FUNCTION (COMMAND) TO INTERFACE.
185             /
186             /  ALL VALUES SHOWN ARE GROUND TRUE (0 SIGNIFIES AN ACTIVE BIT).
187             /                     -----------
188             /
189                   EQU : BUSY   ←   41         / SET-CLEAR CONTROLLER BUSY STATUS BIT
190                   EQU : DSCIF  ←   266        / DISCONNECT INTERFACE.
191                   EQU . DVEND  ←   272        / INCREMENT RETRY COUNTER.
192                   EQU : IFIN   ←   43         / DATA IN (DISC TO INTERFACE)
193                   EQU : IFGTC  ←   222        / GET COMMAND FROM INTERFACE.
194                   EQU : IFOUT  ←   224        / DATA OUT (INTERFACE TO DISC)
195                   EQU : IFPRF  ←   235        / PREFETCH COMMAND FROM INTERFACE.
196                   EQU : RQSRV  ←   270        / SERVICE REQUEST (3000 ONLY)
197                   EQU : SELIF  ←   54         / SELECT INTERFACE.
198                   EQU : SRTRY  ←   53         / SET RETRY COUNTER.
199                   EQU : STDFL  ←   276        / SET DATA FLAG (2100)
200                   EQU : STINT  ←   277        / SET INTERRUPT REQUEST (ERROR OR ATTENTION
201                   EQU : WRTIO  ←   45         / WRITE TIO COMMAND
```

```
                    REGISTER ASSIGNMENTS
/
/
/
/
          REG : ACC    <-   A0        / DISPLACEMENT ACCUMULATOR FOR ECC
          REG : ATTN   <-   A0        / ATTENTION BITS FROM DISC DRIVES.
          REG : BIAS   <-   B0        / SHORTENED CODE BIAS
          REG : BUF1   <-   A1        / USED
          REG : BUF2   <-   B0        /   FOR TEMPORARY
          REG : BUF3   <-   B3        /   QUANTITIES.
          REG : CACC   <-   A0        / C-DISPLACEMENT ACCUMULATOR.
          REG : CCONS  <-   B3        / HOLDS CHINESE REMAINDER THEOREM
                                      /   CONSTANT FOR C-REGISTER.
          REG : CAPM   <-   B0        / CODE LENGTH MODULUS
          REG : CLIM   <-   A1        / COUNTER FOR C-LOOP CONTROL.
          REG : COMAD  <-   B0        / COMMAND ADDRESS FOR EXEC ROUTINE.
          REG : COMWD  <-   A3        / COMMAND WORD - USED BY EXEC ROUTINE.
          REG : COUNT  <-   A1        / TEMP CNTR FOR POWER-ON, RQSYN ROUTINES.
          REG : CYLAD  <-   B2        / CYLINDER ADDRESS REGISTER.
          REG : DUMMY  <-   1         / NOT ASSIGNED TO A OR B GROUP -- USED
                                      /   FOR DUMMY I-O TO CLEAR EOW FLAG,
                                      /   AND TO SET T-REG FOR COND BRNCH.
          REG : EWDCT  <-   A1        / TEMPORARY - ERROR WORD COUNTER.
          REG : HSAD   <-   A2        / HEAD-SECTOR ADDRESS REGISTER.
          REG : HSADB  <-   B3        / TEMPORARY B-REGISTER HSAD
          REG : IFCNO  <-   A0        / INTERFACE (CPU PORT) NUMBER.
          REG : PACC   <-   A3        / P-DISPLACEMENT ACCUMULATOR.
          REG : PCONS  <-   B3        / HOLDS CHINESE REMAINDER THEOREM
                                      /   CONSTANT FOR P-REGISTER
          REG : PLHED  <-   A3        / SAVES PHYSICAL HEAD AND LOGICAL
                                      /   HEAD DURING INITIALIZE.
          REG : PLIM   <-   A1        / COUNTER FOR P-LOOP CONTROL.
          REG : REGO   <-   A0        / TEMPORARY REGISTER.
          REG : SCNT   <-   A3        / SECTOR COUNT FOR VERIFY ROUTINE.
          REG : STATR  <-   B1        / CONTROLLER STATUS REGISTER.
          REG : TCYLD  <-   A0        / SAVES CYLINDER ADDR DURING VERIFY
          REG : THSAD  <-   B0        / SAVES HEAD-SECTOR ADDR -- VERIFY
          REG : TSTTM  <-   A3        / TEMP TO TEST FOR TIME-OUT INTRPT
          REG : WCNT   <-   A1        / SECTOR WORD COUNTER.
          REG : XREG   <-   A3        / LEAST SIGNIF  WORD OF ERROR PATTERN.
          REG : YREG   <-   B0        / NEXT  SIGNIF  WORD OF ERROR PATTERN.
          REG : ZREG   <-   B3        / MOST  SIGNIF  WORD OF ERROR PATTERN.
```

```
                    CONSTANTS (SOME ARE 1'S COMPLEMENT)
/
/
/
/
          EQU  :  BIT3    ←    10          / BIT 3 MASK.
          EQU  :  CAPMU   ←    10          / NATURAL CODE LENGTH = 2279
          EQU  :  CAPML   ←    347         /   (DEC), UPPER & LOWER BYTES.
          EQU  :  CATN    ←    376         / CLEAR SELECTED ATTENTION
          EQU  :  CCLKH   ←    310         / FREEZE P, CLOCK HI FOR C SHIFT
          EQU  :  CCLKL   ←    300         / FREEZE P, CLOCK LO FOR C SHIFT
          EQU  :  CCONU   ←    6           / CHINESE REMAINDER THEOREM CONSTANT
          EQU  :  CCONL   ←    67          /   FOR C, UPPER AND LOWER BYTES.
          EQU  :  CFST    ←    375         / CLEAR SELECTED FIRST STATUS.
          EQU  :  CLBSY   ←    1           / CLEAR CONTROLLER BUSY BIT
          EQU  :  CLICW   ←    37          / CLEAR INTERNAL CONTROL WORD
          EQU  :  CLKHH   ←    211         / TAKE CLOCK HIGH ONCE.
          EQU  :  CLKHI   ←    230         / TAKE CLOCK HI FOR INHIBITS.
          EQU  :  CLRCL   ←    1           / CLEAR INTERFACE FUNCTION CLOCK.
          EQU  :  CSTRB   ←    37          / CLEAR DISC COMMAND STROBE.
          EQU  :  CURNT   ←    16          / ADDRESS OF CURRENT I'FACE IN RAM.
          EQU  :  DRTYP   ←    14          / ADDR OF DRIVE TYPE WORD IN RAM.
          EQU  :  DSC     ←    200         / START COUNT OF 7 EOWS TO FREEZE.
          EQU  :  ERWCT   ←    371         / # OF CHECK WORDS (TWO'S COMP )
          EQU  :  ESC     ←    0           / START COUNT OF 2 EOWS TO SHIFT
          EQU  :  FALSE   ←    377         / POSITIVE-TRUE FALSE.
          EQU  :  FRPSH   ←    312         / CLOCK HI, CLEAR INHREG, FREEZE P
          EQU  :  FULSC   ←    166         / FULL SECTOR WDCNT, TWO'S COMP
                                           /   (INCLUDES SYNC, CYLAD, HSAD,
                                           /   CRC, AND ECC WORDS).
          EQU  :  MXDRV   ←    365         / MAX # OF DRIVES, TWO'S COMP.
          EQU  :  NSEC    ←    15          / RAM ADDR. OF VERIFY RETRY COUNTER.
          EQU  :  PCLKH   ←    250         / FREEZE C, CLOCK HI FOR SHIFT P
          EQU  :  PCLKL   ←    240         / FREEZE C CLOCK LO FOR SHIFT P
          EQU  :  PCONU   ←    2           / CHINESE REMAINDER THEOREM CONSTANT
          EQU  :  PCONL   ←    261         /   FOR P, UPPER AND LOWER BYTES
          EQU  :  RDONL   ←    13          / ADDRESS OF READ-ONLY
                                           /   SWITCH STATUS IN RAM.
          EQU  :  POLIF   ←    17          / ADDRESS OF LAST INTERFACE POLLED
          EQU  :  PRVAT   ←    10          / RAM ADDR OF DRV WITH PREV ATTN.
          EQU  :  RCC1    ←    76          / READ AND CYCLIC CHECK.
          EQU  :  RCC2    ←    72          / SAME WITH ACRDY CHECK ENABLED
          EQU  :  RDWRT   ←    13          / CLR ICW, KEEP RD-WRT BIT, CRCC
          EQU  :  RECC    ←    226         / READ WITH ECC.
          EQU  :  RERWD   ←    52          / READ (SHIFT IN) ERROR WORDS
          EQU  :  RWCT    ←    201         / DATA WORD COUNT - 1, TWO'S COMP
          EQU  :  SETCL   ←    0           / SET INTERFACE FUNCTION CLOCK.
          EQU  :  START   ←    100         / START CONTROLLER TIME-OUT CKT
          EQU  :  STBSY   ←    0           / SET CONTROLLER BUSY BIT
          EQU  :  STOP    ←    200         / STOP CONTROLLER TIME-OUT CKT
          EQU  :  STRB    ←    77          / SET DISC COMMAND STROBE.
          EQU  :  TRUE    ←    0           / POSITIVE-TRUE TRUE.
          EQU  :  WAKST   ←    2           / DRIVE AVAILABLE STATUS
          EQU  :  WCC1    ←    75          / WRITE AND CYCLIC CHECK.
          EQU  :  WCC2    ←    71          / SAME WITH ACRDY CHECK ENABLED
          EQU  :  WCT     ←    200         / DATA WORD COUNT, TWO'S COMP
          EQU  :  WECC    ←    26          / WRITE WITH ECC
          EQU  :  WERWD   ←    61          / WRITE (SHIFT OUT) ERROR WORDS
          EQU  :  WKUPC   ←    26          / WAKEUP COMMAND CODE.
```

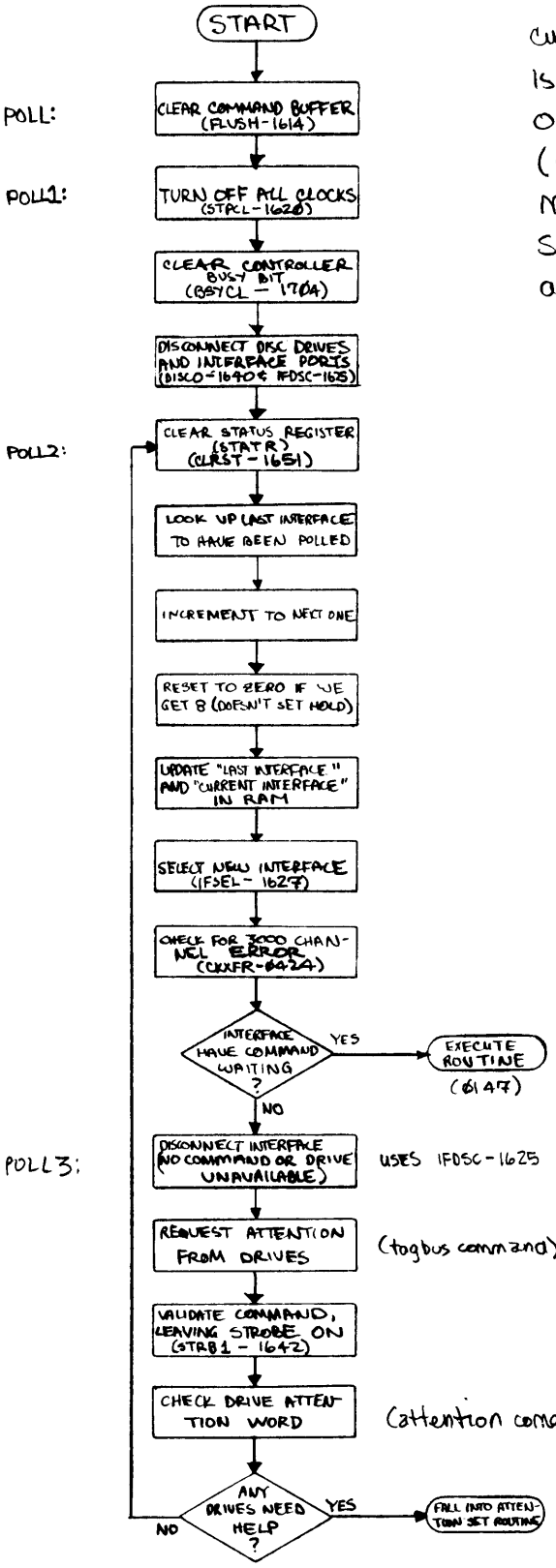
```
                          POWER ON CLEAR, TIME-OUT PROCESSOR
                /
                /
                /
                /
                       ORG = 0
                /
                /
                /  CLEAR RAM ONLY WHEN POWER IS TURNED ON OR WHEN A HARD CLEAR
                /  IS RECEIVED FROM THE CPU   LEAVE IT ALONE IF WE GET HERE VIA
                /  A TIME-OUT INTERRUPT
                /
0000 64000001           BR : NXTAD                      / SET CC BIT IF CLEAR
0001 66001625 NXTAD     CA : IFDSC                      / PREVENT INTERRUPT AT POWER-ON
0002 10100454           DI : TSTTM  ←   TIMER,U     / SEE IF THIS WAS
0003 37706074       TSTTM =         PASS TSTTM,U    /   TIME-OUT INTERRUPT
0004 44540000           CC = TMSB               ,RS
0005 64000025           BR : PWRON                      / NO, GO DO POWER-ON SEQUENCE.
                                                        / YES, FALL INTO TIME-OUT SQNC.
                /
                /
                /  THIS SECTION IS ENTERED IN CASE OF AN INTERFACE TIME-OUT   ANY
                /  DRIVE HOLD BITS WHICH MAY HAVE BEEN SET BY THE INTERFACE ARE
                /  CLEARED SO THAT OTHER INTERFACES MAY USE THE DRIVE.
                /
0006 27722D12        COUNT = 12     PASS       ,L     / TEST ONLY RAM ADDRESSES 10-0.
0007 07620016           DO : RAMAD  ←   CURNT,L     / FIND OUT WHO CURRENT I'FC IS
0010 10120440           DI : REGO   ←   RAM  ,L     /   (IT'S JUST TIMED OUT)
0011 17620405 CLHLD     DO : RAMAD  ←   COUNT,L     / GET I'FC ASSOCIATED WITH
0012 10020456           DI : BUF3   ←   RAM  ,L     /   CURRENT DRIVE.
0013 36437520         BUF3 =        PASS BUF3 ,L,SR / CLEAR IT'S HOLD BIT
0014 36223460        DUMMY = REGO   XOR  BUF3 ,L     / SEE IF DRIVE BELONGS TO
0015 44400000           CC = TNZRO                    /   CURRENT INTERFACE
0016 64000021           BR : NTEQL                    / NO, DON'T MODIFY RAM
0017 36437540         BUF3 =        PASS BUF3 ,L,SL / YES, RESTORE I'FC NUMBER WITH
0020 16421455           DO : RAM    ←   BUF3 ,L     /   HOLD BIT CLEAR AND WRITE BACK.
0021 30122D64 NTEQL COUNT =         DEC  COUNT,L    / SET UP NEXT RAM WORD
0022 44100000           CC = LOVER                    / DONE THEM ALL (ROLLED THROUGH 0)?
0023 64000011           BR : CLHLD                    / NOT YET, DO ANOTHER ONE.
0024 64000035           BR : CLR1                     / YES, RESET FLMSK, POLL INTERFACES.
                /
                /
                /  THIS SECTION CLEARS THE INTERFACE-DISC DRIVE ASSOCIATIVE RAM
                /  WHEN POWER IS TURNED ON OR WHEN THE INTERFACE SENDS A HARD
                /  CLEAR COMMAND
                /
0025 27722D20 PWRON COUNT = 20     PASS       ,L     / SET UP LOOP COUNTER.
0026 30122D64 CLRAM COUNT =        DEC  COUNT,L    / GET NEXT RAM ADDRESS (17 OCTAL-0)
0027 44400000           CC = TNZRO                    / SET CC BIT UNLESS LAST ONE (0)
0030 17620405           DO : RAMAD  ←   COUNT,L     / ADDRESS THE CURRENT RAM WORD
0031 07620400           DO : RAM    ←   0    ,L     / CLEAR IT
0032 64000026           BR : CLRAM                    / LOOP IF NOT DONE (SEE CC AT *-3)
0033 07624012           DO : TGBUS  ←   CLRCM,L     / DONE, CLEAR ALL DRIVES
0034 66001641           CA : STROB
0035 07602777 CLR1      DO : CLKOF  ←   377  ,U     / CLEAR ANY CLOCK OFFSET
0036 07625777           DO : FLMSK  ←   FALSE,L     / RESET THE FILE MASK.
                                                        / FALL INTO POLL LOOP
```

POWER ON CLEAR / TIME-OUT PROCESSOR



Ram is cleared for power on or hard clear conditions only; ram is preserved if entry is made by a time-out interrupt.

POLL LOOP



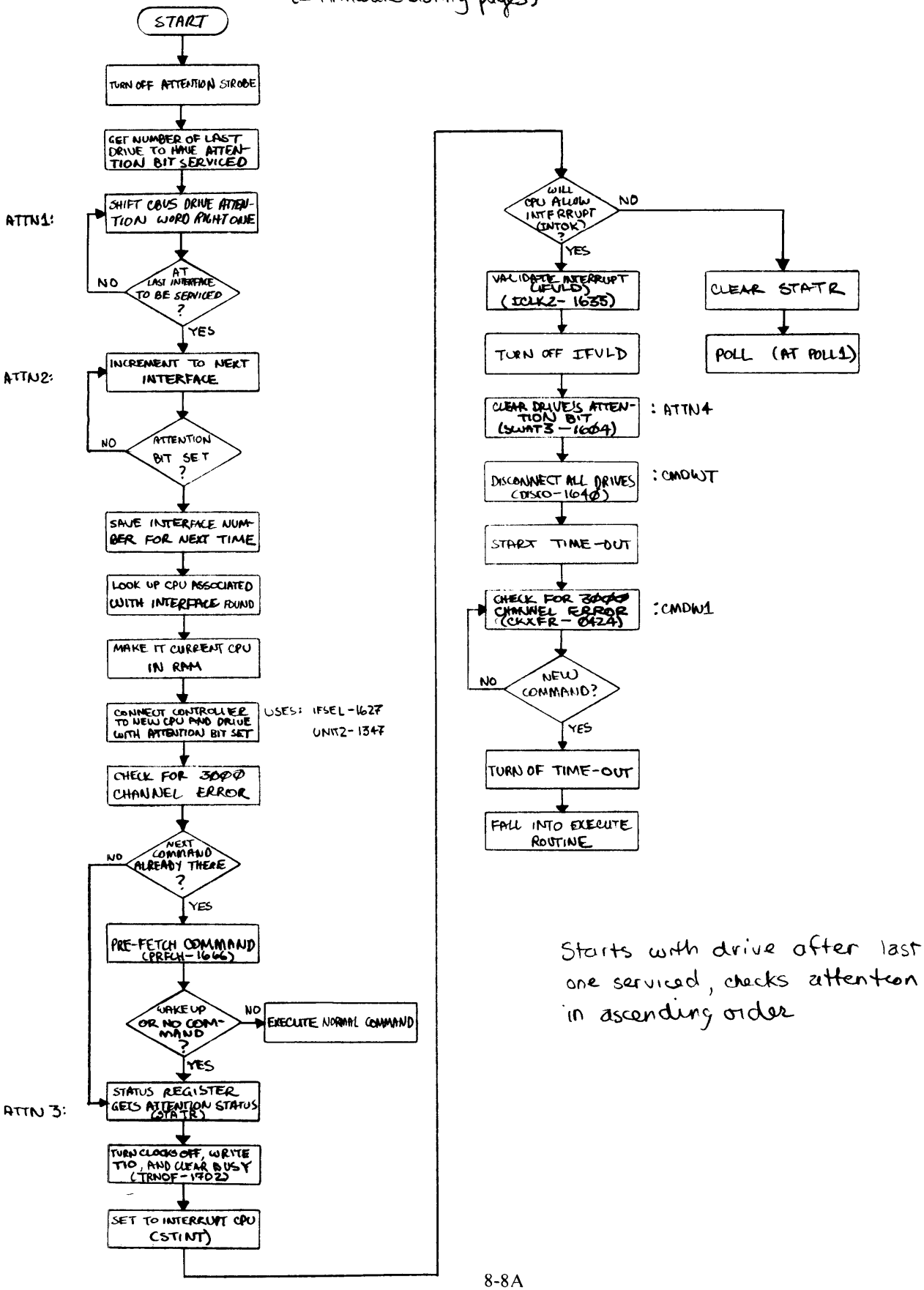
currently connected CPU interface number is stored in RAM 14; poll loop used only when retention of past history (disc or controller status, CYLAD, file mask, etc.) is not required (ie. SEEK, RECALIBRATE, etc.). Interfaces are polled serially.

```
                          POLL LOOP
                /
                /
                /
                /
                /   POLL LOOP -- WAIT HERE BETWEEN EVENTS WHICH DO NOT REQUIRE
                /   RETENTION OF PAST HISTORY (DISC OR CONTROLLER STATUS, CYLAD,
                /   FILE MASK, ETC)   WHILE IN THIS LOOP, THE CPU'S ARE POLLED
                /   FOR NEW COMMANDS AND THE DRIVES ARE POLLED FOR ATTENTION.
                /
0037 66001614 POLL      CA : FLUSH                  / CLEAR COMMAND BUFFER.
0040 66001620 POLL1     CA : STPCL                  / TURN OFF ALL CLOCKS
0041 66001704           CA : BSYCL                  / CLEAR THE CONTROLLER BUSY BIT
0042 66001640           CA : DISCO                  / DISCONNECT THE DISC DRIVES
0043 66001625           CA : IFDSC                  /   AND THE INTERFACE PORTS.
                /
                /  THIS SECTION EXAMINES THE COMMAND READY FLAG OF EACH INTERFACE,
                /  STARTING WITH THE ONE FOLLOWING THE CURRENTLY-SELECTED INTERFACE.
                /  IN THIS WAY, THE INTERFACES ARE POLLED SERIALLY, AND NO COMBINATION
                /  OF OPERATIONS ON LOWER-NUMBERED INTERFACES CAN SHUT OUT OPERATIONS ON
                /  HIGHER-NUMBERED ONES.  THE CURRENTLY CONNECTED CPU (INTERFACE) NUMBER
                /  IS STORED IN RAM(14)   (SEE SUBROUTINE "UNIT" FOR RAM FORMAT)
                /
0044 66001651 POLL2     CA : CLRST                  / CLEAR STATUS REGISTER (STATR)   (B1)
0045 07620017           DO : RAMAD  ←   POLIF,L     / LOOK UP LAST INTERFACE
0046 10020456           DI : BUF3   ←   RAM  ,L     /   TO BE POLLED
0047 22237401         BUF3 = 1      PLUS BUF3 ,L    / BUMP TO NEXT ONE.
0050 27437407         BUF3 = 7      AND  BUF3 ,L    / RESET TO 0 IF WE GET 8
                                                    /   (INSURES HOLD BIT NOT SET)
0051 16421455           DO : RAM    ←   BUF3 ,L     / UPDATE "LAST INTERFACE" IN RAM.
0052 07620016           DO : RAMAD  ←   CURNT,L     / ALSO UPDATE "CURRENT INTERFACE"
0053 16421455           DO : RAM    ←   BUF3 ,L
0054 15221555           DO : IDTBF  ←   BUF3 ,L,C   / NOW SELECT NEW INTERFACE.
0055 66001627           CA : IFSEL
0056 66000424           CA : CKXFR                  / CHECK FOR 3000 CHANNEL ERROR.
0057 42000000           CC = CMRDY                  / INTERFACE HAVE COMMAND WAITING?
0060 64000147           BR : EXEC                   / YES, GO DO IT, LEAVE ATTN ON.
0061 66001625 POLL3     CA : IFDSC                  / NO, OR DRIVE NOT AVAILABLE,
                                                    /   DISCONNECT INTERFACE
0062 07624014           DO : TGBUS  ←   REQAT,L     / REQUEST ATTENTION FROM DRIVES
0063 66001642           CA : STRB1                  / VALIDATE COMMAND, LEAVE STROBE ON.
0064 10102200           DI : ATTN   ←   CBSIN       / CHECK DRIVE ATTENTION WORD
0065 34100260         ATTN =        CMP  ATTN
0066 44440000           CC = TNZRO            ,RS   / ANY DRIVES NEED HELP?
0067 64000044           BR : POLL2                  / NO, CONTINUE POLLING INTERFACES.
```

```
406                          SET ATTENTION AND INTERRUPT
407                  /
408                  /
409                  /
410                  /
411                  /    ONE OR MORE DRIVES HAS ATTENTION SET   STARTING WITH ONE
412                  /  DRIVE AFTER THE ONE LAST SERVICED, CHECK FOR ATTN IN ASCEND-
413                  /  ING ORDER (0 FOLLOWS 7), AND REPORT THE FIRST ONE WITH
414                  /  ATTENTION.  BUILD THE ATTENTION STATUS AND UNIT NUMBER IN
415                  /  A TEMPORARY B-REGISTER.  PUT INTO STATR ONLY IF WE GET TO
416                  /  LABEL ATTN3   THIS AVOIDS LEAVING ATTENTION STATUS LYING
417                  /  AROUND FOR COMMANDS WHICH DON'T CLEAR STATR (E.G. RQSYN)
418                  /
419 0070 07604437            DO : INTCW  ←   CSTRB,U     / TURN OFF ATTENTION STROBE.
420 0071 37610200          BUF2 =        PASS ATTN ,SW    / SET DUPLICATE DRIVE ATTENTION
421 0072 36500060          ATTN =        PASS BUF2 ,U     /   BYTES IN BOTH HALVES OF ATTN.
422 0073 07620010            DO : RAMAD  ←   PRVAT,L     / LOOK UP LAST DRIVE TO
423 0074 10120444            DI : BUF1   ←   RAM  ,L     /   HAVE ATTENTION BIT SERVICED
424 0075 37636064          BUF3 =        PASS BUF1 ,L     / ACCUMULATE DRIVE NUMBER IN BUF3,L.
425 0076 37700320 ATTN1    ATTN =        PASS ATTN ,SR    / SHIFT AND IGNORE ATTENTION BITS
426 0077 30122064          BUF1 =        DEC  BUF1 ,L     /   UNTIL WE COME TO DRIVE BEYOND
427 0100 44100000            CC = LOVER                   /   LAST ONE WE REPORTED.
428 0101 64000076            BR : ATTN1
429 0102 22237401 ATTN2    BUF3 = 1      PLUS BUF3 ,L     / FOUND IT, NOW START COUNTING.
430 0103 27437407          BUF3 = 7      AND  BUF3 ,L     / RESET TO 0 IF WE GET 8
431 0104 37700320          ATTN =        PASS ATTN ,SR    / TEST CURRENT ATTN LSB, SHIFT
432 0105 44640000            CC = TLSB             ,RS    / THIS DRIVE HAVE ATTENTION SET?
433 0106 64000102            BR : ATTN2                   / NO, CONTINUE SEARCH.
434 0107 16421455            DO : RAM    ←   BUF3 ,L      / YES, SAVE ITS NUMBER FOR NEXT TIME.
435 0110 16421415            DO : RAMAD  ←   BUF3 ,L      / LOOK UP CPU FOR THIS DRIVE.
436 0111 10120440            DI : IFCNO  ←   RAM  ,L
437 0112 37700320         IFCNO =        PASS IFCNO,SR    / POSITION CPU FIELD
438 0113 07620016            DO : RAMAD  ←   CURNT,L     / MAKE IT THE CURRENT CPU IN RAM
439 0114 17620041            DO : RAM    ←   IFCNO,L
440 0115 14020141            DO : IDTBF  ←   IFCNO,L,C   / CONNECT CONTROLLER TO NEW CPU
441 0116 66001627            CA : IFSEL
442 0117 15221515            DO : CBUF   ←   BUF3 ,L,C   /   AND TO DRIVE WHICH HAS
443 0120 66001347            CA : UNIT2                   /   ATTENTION BIT SET.
444 0121 66000424            CA : CKXFR                   / CHECK FOR 3000 CHANNEL ERROR.
445 0122 27616037          BUF3 = 37     PASS       ,U    / BUF3,U GETS ATTENTION STATUS.
446 0123 42040000            CC = CMRDY            ,RS    / IS NEXT COMMAND ALREADY THERE?
447 0124 64000131            BR : ATTN3                   / NO, GO INTERRUPT.
448 0125 66001666            CA : PRFCH                   / YES, PRE-FETCH IT
449 0126 26222026         DUMMY = WKUPC XOR  COMAD,L     / TEST IT FOR WAKE-UP COMMAND
450 0127 44400000            CC = TNZRO
451 0130 64000150            BR : EXEC1                   / NO, GO EXECUTE NORMAL COMMAND
452 0131 36413660 ATTN3 STATR =        PASS BUF3          / YES, OR NO COMMAND, NOW SET STATR.
453 0132 66001702            CA : TRNOF                   / CLOCKS OFF, WRT TIO, CLEAR BUSY
454 0133 07622677            DO : IFNBF  ←   STINT,L     / SET TO INTERRUPT CPU
455 0134 43040000            CC = INTOK            ,RS    / WILL CPU ALLOW INTERRUPT?
456 0135 64000040            BR : POLL1                   / NO, CLR STATR, POLL UNTIL IT DOES.
457
458                  /
459                  /
460                  /
461                  /
462                  /  THE FOLLOWING USE OF IFVLD IS FOR THREE REASONS:
463                  /  1    THIS IS A REAL-TIME CONSIDERATION, WHERE WE WANT A MINIMUM
464                  /       LATENCY BETWEEN THE TIME WE TEST THE INTOK FLAG AND WHEN
465                  /       WE INTERRUPT   THIS IS IN CASE THE PROGRAMMER HAS CHANGED
466                  /       INTOK JUST AFTER WE TESTED IT   THE CALL TO ICLK2 AVOIDS
467                  /       THE 600 NSEC DELAY BEFORE THE LEADING EDGE OF IFVLD.
468                  /  2.   THE 600 NSEC DELAY IN ICLCK IS NOT REQUIRED HERE, SINCE THE
469                  /       "STINT" FUNCTION WENT OUT 700 NSEC AGO (SEE PREVIOUS PAGE).
470                  /  3    A DIRECT "IFVLD _ CLRCL" SHOULD FOLLOW RATHER THAN A CALL TO
471                  /       ICLK3   THE FUNCTION IS VALIDATED ON THE TRAILING EDGE OF IFVLD,
472                  /       AND THE DIRECT CALL MAKES THE TRAILING EDGE OCCUR EARLIER.
473                  /
474 0136 66001633            CA : ICLK2                   / VALIDATE INTERRUPT COMMAND.
475 0137 07606001            DO : IFVLD  ←   CLRCL,U     / THEN TURN IT OFF
476 0140 66001604 ATTN4      CA : SWAT3                   / CLEAR THE DRIVE'S ATTENTION BIT
477                  /
478                  /  WAIT HERE FOR NEXT COMMAND FROM INTERFACE.
479                  /
480 0141 66001640 CMDWT      CA : DISCO                   / DISCONNECT ALL DRIVES.
481 0142 07600500            DO : TIMER  ←   START,U     / TURN ON TIME-OUT CIRCUIT
482 0143 66000424 CMDW1      CA : CKXFR                   / CHECK FOR 3000 CHANNEL ERROR.
483 0144 42040000            CC = CMRDY            ,RS    / WAIT FOR NEW COMMAND
484 0145 64000143            BR : CMDW1                   /   OR TIME OUT.
485 0146 07600600            DO : TIMER  ←   STOP ,U     / GOT IT, TURN OFF TIME-OUT
486                                                       /   CIRCUIT AND FALL INTO EXEC.
```

SET ATTENTION AND INTERRUPT

(2 firmware listing pages)

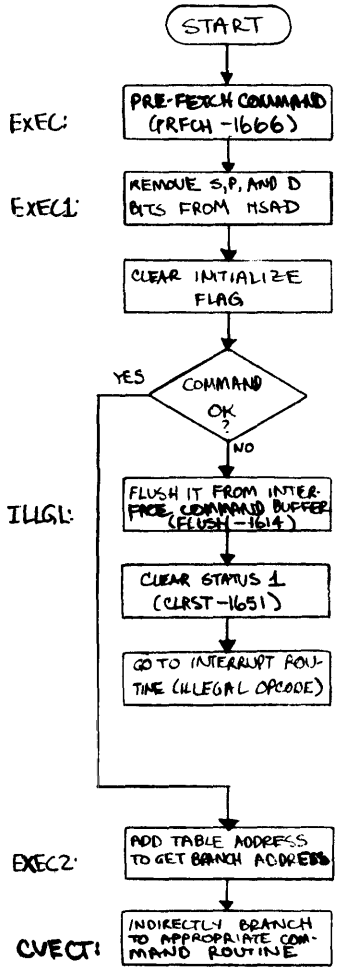


Starts with drive after last one serviced, checks attention in ascending order

```
                        COMMAND FORMATS
/
/
/
/       1 1 1 1 1 1
/       5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0  BIT (2100 NUMBERING)
/       - - - - - - - - - - - - - - - -
/     !       C C C C C                 !  ADREC, CLEAR, END,
/     !                                 !    LTIO, REQAD, RQSYN
/     !       C C C C C         U U U U !  RQSCT, STAT
/     !       C C C C C H D     S E C T !  COLD LOAD
/     !       C C C C C R T R Y M A S K !  SET FILE MASK
/     !       C C C C C 1       U U U U !  SEEK, RECALIBRATE
/     ! S P D C C C C C 0       U U U U !  WRITE ADDRESS (INITIALIZE)
/     !       C C C C C 0       U U U U !  (ALL OTHER COMMANDS)
/       - - - - - - - - - - - - - - - -
/
/      WHERE  C = FIVE-BIT COMMAND OPCODE:
/
/        UBYTE  LBYTE  DESCRIPTION
/        -----  -----  -----------
/
/            0      0  COLD LOAD READ (BOOT)
/          400      1  RECALIBRATE
/         1000      2  SEEK
/         1400      3  REQUEST STATUS
/         2000      4  REQUEST SECTOR ADDRESS
/         2400      5  READ
/         3000      6  READ FULL SECTOR
/         3400      7  VERIFY
/         4000     10  WRITE
/         4400     11  WRITE FULL SECTOR
/         5000     12  CLEAR
/         5400     13  WRITE ADDRESS (INITIALIZE)
/         6000     14  ADDRESS RECORD
/         6400     15  REQUEST SYNDROME
/         7000     16  READ WITH OFFSET
/         7400     17  SET FILE MASK
/        10000     20  (NOT USED)
/        10400     21  (NOT USED)
/        11000     22  READ WITHOUT VERIFY
/        11400     23  LOAD TIO REGISTER
/        12000     24  REQUEST DISC ADDRESS
/        12400     25  END (RETURNS CONTROLLER TO POLL LOOP)
/        13000     26  WAKEUP
/
/             S = FLAG AS SPARE TRACK.
/             P = FLAG AS PROTECTED TRACK (WRITE COMMAND MAY ABORT)
/             D = FLAG AS DEFECTIVE TRACK.
/            HD = HEAD ADDRESS FOR COLD LOAD READ COMMAND
/          SECT = SECTOR ADDRESS FOR COLD LOAD READ COMMAND.
/          RTRY = DATA TRANSFER RETRY COUNTER (3000 ENVIRONMENTS)
/          MASK = FILE MASK BITS (SEE DESCRIPTION IN SFMSK PROCESSOR)
/             U = DISC DRIVE (UNIT) ADDRESSED BY THE COMMAND   ERRORS
/                 MAY OCCUR IF U = 10 (OCTAL)
/         BIT 7 = HOLD (BUSY) BIT   IF SET, RESERVES DRIVE "U" FOR
/                 INTERFACE ISSUING THE COMMAND   COMMANDS FROM OTHER
/                 INTERFACES TRYING TO ACCESS THIS DRIVE WILL BE DEFERRED
/                 UNTIL THE DRIVE IS AVAILABLE.
```

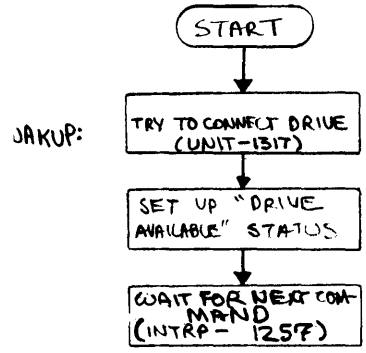
```
                          OBTAINING COMMAND AND EXECUTING BRANCH VECTOR
                 /
                 /
                 /
                 /
0147 66001666 EXEC      CA : PRFCH                    / PRE-FETCH THE NEXT COMMAND.
0150 27616037 EXEC1   BUF3 = 37     PASS       ,U     / CLEAR S, P, AND D BITS
0151 37505470         HSAD = HSAD   AND   BUF3 ,U     /   FROM HSAD
0152 07623377           DO : INITL  ←     FALSE,L     / CLEAR INITIALIZE FLAG.
                 /      DO : RETRY  ←     FALSE,L       DUMMY AS LONG AS RETRY = INITL.
0153 22222351        DUMMY = 351    PLUS COMAD,L     / CHECK FOR ILLEGAL OPCODE.
0154 44140000           CC = LOVER             ,RS
0155 64000161           BR : EXEC2                    / OPCODE O.K.
0156 66001614 ILLGL     CA : FLUSH                    / ILLEGAL, FLUSH IT FROM
                                                      /   INTERFACE COMMAND BUFFER.
0157 66001651           CA : CLRST                    / CLEAR STATUS-1
0160 64001771           BR : OPCER                    / GO INTERRUPT - ILLEGAL OPCODE.
                 /
                 /
                 /  CODING FROM HERE TO END OF PAGE MUST RESIDE IN ADDRESSES <= 377B.
                 /
0161 22236164 EXEC2   BUF3 = CVECT PLUS COMAD,L     / ADD TABLE ADDRESS TO
0162 35221414           NO : BUF3             ,L     /   GET ADDRESS INTO
0163 74000000           BR : I                       /   BRANCH VECTOR.
                 /
                 /  INDIRECT BRANCH THROUGH COMMAND VECTOR TO START OF
                 /  APPROPRIATE ROUTINE.
                 /
0164 64000215 CVECT     BR : BOOT                     / COLD LOAD READ
0165 64000233           BR : RECAL                    / RECALIBRATE (RESTORE HOME)
0166 64000241           BR : SEEK                     / SEEK.
0167 64000301           BR : STATS                    / REQUEST STATUS
0170 64000346           BR : RQSCT                    / REQUEST SECTOR.
0171 64000407           BR : READ                     / READ.
0172 64000613           BR : RFS                      / READ FULL SECTOR.
0173 64000507           BR : VRFCM                    / VERIFY SECTOR(S).
0174 64001002           BR : WRITE                    / WRITE.
0175 64001032           BR : WFS                      / WRITE FULL SECTOR.
0176 64001262           BR : CLR                      / CLEAR.
0177 64000642           BR : INIT                     / WRITE ADDRESS (INITIALIZE)
0200 64000264           BR : RECRD                    / ADDRESS RECORD
0201 64001106           BR : RQSYN                    / REQUEST SYNDROME.
0202 64000460           BR : ROFST                    / READ WITH OFFSET
0203 64001252           BR : SFMSK                    / SET FILE MASK.
0204 64000156           BR : ILLGL                    / ILLEGAL OPCODE (WAS CLRUB).
0205 64000156           BR : ILLGL                    / ILLEGAL OPCODE (WAS UNTIN)
0206 64000416           BR : RNVFY                    / READ WITHOUT VERIFY
0207 64001100           BR : LTIO                     / LOAD TIO REGISTER.
0210 64001266           BR : REQAD                    / REQUEST DISC ADDRESS
0211 64000037           BR : POLL                     / END OF COMMAND SEQUENCE
                                                      /   (RETURN TO POLL LOOP).
                                                      / (FALL INTO WAKEUP COMMAND IF HERE).
```

OPERATING COMMAND AND EXECUTING BRANCH VECTOR



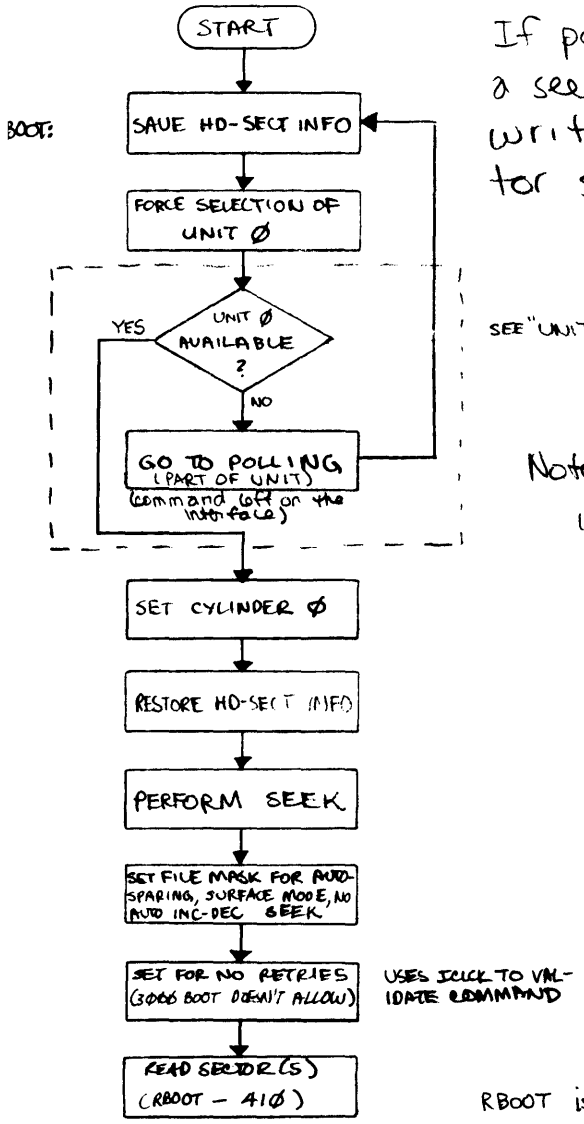
ALLOWABLE COMMANDS:	FLOWCHART:
COLD LOAD READ	P. 8-10B
RECALIBRATE	P. 8-12A
SEEK	P. 8-12A
REQUEST STATUS	P. 8-14A
REQUEST SECTOR ADDRESS	P. 8-16A
READ	P. 8-16B
READ FULL SECTOR	P. 8-22A
VERIFY SECTOR(S)	P. 8-20A
WRITE	P. 8-26A
WRITE FULL SECTOR	P. 8-24B
CLEAR	P. 8-30B
WRITE ADDRESS (INITIALIZE)	P. 8-22B
ADDRESS RECORD	P. 8-12B
REQUEST SYNDROME	P. 8-28A
READ WITH OFFSET	P. 8-18B
SET FILE MASK	P. 8-30B
READ W/O VERIFY	P. 8-16B
LOAD TIO REGISTER	P. 8-26B
REQUEST DISC ADDRESS	P. 8-32A
END OF COMMAND SEQUENCE	P. 8-6B
WAKEUP	P. 8-10B

WAKEUP COMMAND



Used to access a drive currently held by another interface (when drive is available, interface is interrupted with "drive available" status); WAKEUP is left on interface until connection with desired drive is obtained (polling is resumed in UNIT if drive is unavailable)

COLD LOAD READ (BOOT)



If possible, drive zero is connected, a seek is made to cylinder zero, writing begins at head and sector specified in command word

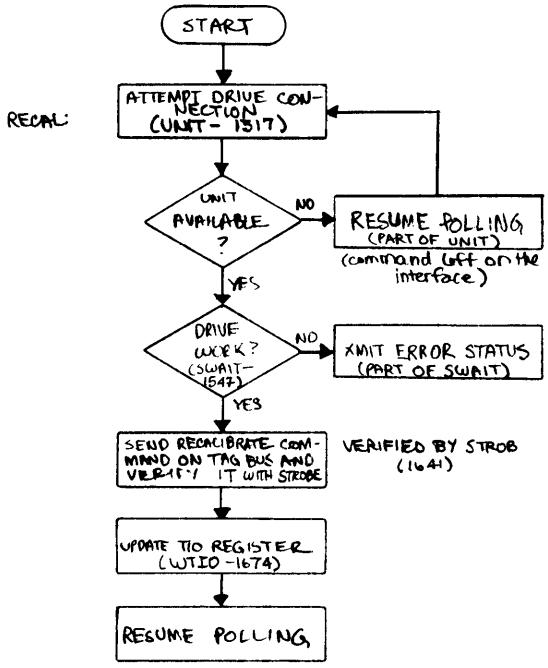
Note: COLD LOAD READ remains on interface during polling

RBOOT is READ subroutine; reads until EOD by interface or error (overrun, etc.)

```
598                          WAKEUP, COLD LOAD READ (BOOT) COMMANDS
599                 /
600                 /
601                 /
602                 /
603                 /  THE WAKEUP COMMAND IS ISSUED BY AN INTERFACE WHEN IT WANTS TO
604                 /  ACCESS A DRIVE CURRENTLY BEING HELD BY ANOTHER INTERFACE.  AS
605                 /  LONG AS THE DRIVE CONTINUES TO BE HELD BY THE OTHER INTERFACE,
606                 /  THE WAKEUP COMMAND FUNCTIONS AS A NOP (CONTROLLER RETURNS TO
607                 /  POLL).  WHEN THE DRIVE IS AVAILABLE, THE FIRST INTERFACE IS
608                 /  INTERRUPTED ("AWAKENED") WITH A "DRIVE AVAILABLE" STATUS AND
609                 /  DRIVE NUMBER.  WHEN THE DRIVE BECOMES AVAILABLE, ITS HOLD BIT
610                 /  WILL BE UPDATED FROM BIT 7 (HOLD BIT FIELD) OF THE WAKEUP
611                 /  COMMAND.  NOTE:  IF THE DRIVE IS BEING HELD BY THE INTERFACE
612                 /  ISSUING THE WAKEUP COMMAND, "DRIVE AVAILABLE" STATUS IS
613                 /  RETURNED IMMEDIATELY
614                 /
615 0212 66001317 WAKUP    CA : UNIT                    / TRY TO CONNECT DRIVE.
616 0213 22212402       STATR = WAKST PLUS STATR,U     / SET UP "DRIVE AVAILABLE" STATUS.
617 0214 64001257          BR : INTRP                   / GO WAKE UP THE INTERFACE.
618                 /
619                 /  BOOT TESTS THE HOLD BIT OF UNIT 0   IF CLEAR, OR IF UNIT 0 IS HELD
620                 /  BY THE CURRENT INTERFACE, BOOT SEEKS TO DRIVE 0, CYLINDER 0, HEAD
621                 /  AND SECTOR SPECIFIED IN COMMAND WORD.  IT THEN READS UNTIL THE
622                 /  INTERFACE SIGNALS END OF DATA.  IF THE DRIVE IS HELD BY ANOTHER
623                 /  INTERFACE, BOOT RETURNS TO POLL WITH THE COLD LOAD COMMAND STILL
624                 /  PENDING ON THE INTERFACE.
625                 /
626 0215 34100274 BOOT   REGO =       CMP  COMWD       / SAVE HD-SECT, CLEAR UPPER BYTE.
627 0216 27726377       COMWD = 377   PASS      ,L     / FORCE UNIT 0
628 0217 66001317          CA : UNIT                   / TRY TO SELECT IT   RETURN
629                                                    /   ONLY IF IT'S AVAILABLE.
630 0220 36414660       CYLAD =       PASS STATR       / SET CYLINDER 0 (CLRST HAS BEEN
631                                                    /   CALLED AND UNIT # = 0).
632 0221 37704340        HSAD =       PASS REGO ,SL    / SHIFT HEAD NUMBER
633 0222 37704350        HSAD =       PASS HSAD ,SL    /   INTO UPPER BYTE.
634 0223 37724130        HSAD =       PASS HSAD ,L,SR  / RESTORE SECTOR NUMBER
635 0224 37724130        HSAD =       PASS HSAD ,L,SR  /   IN LOWER BYTE.
636 0225 66000247          CA : SEEK1                  / DO THE SEEK.
637 0226 07625403          DO : FLMSK  ←   3     ,L    / AUTO TRACK SPARING, SURFACE MODE,
638                                                    /   NO AUTO INCR-DECR SEEK.
639 0227 07622453          DO : IFNBF  ←   SRTRY,L    / SET THE RETRY COUNTER ALSO.
640 0230 07621570          DO : IDTBF  ←   170   ,L    / NO RETRIES ALLOWED, 3000 BOOT
641 0231 66001630          CA : ICLCK                  /   HAS NO PROVISION FOR THEM.
642 0232 64000410          BR : RBOOT                  / NOW READ THE SECTOR(S)
```

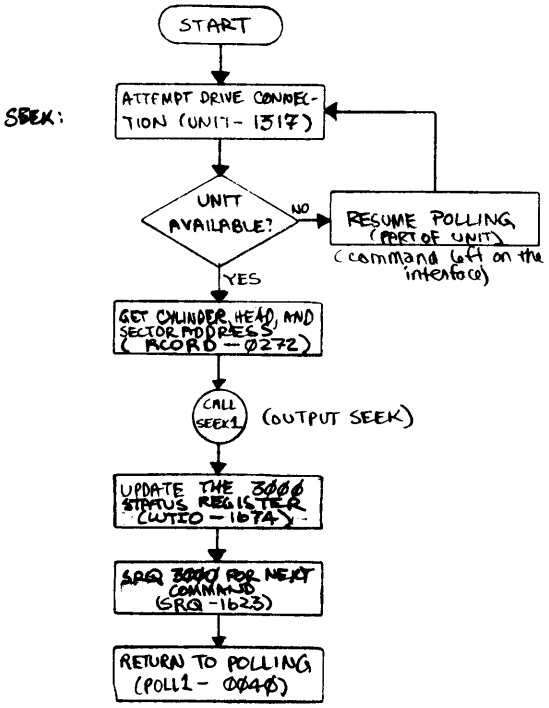
```
643                         RECALIBRATE, SEEK COMMANDS, SEEK1, SEEK2, SEEK3
644                 /
645                 /
646                 /
647                 /
648                 /  THE RECALIBRATE (RESTORE HOME) COMMAND ADDRESSES THE UNIT AND
649                 /  CAUSES IT TO RESET ITSELF TO CYLINDER 0.  IT THEN RELEASES
650                 /  THE UNIT   NOTE:  THE CPU MUST WAIT FOR AN INTERRUPT RESPONSE
651                 /  AFTER OUTPUTTING THIS COMMAND, ELSE THE COMMAND MAY BE
652                 /  OVERWRITTEN ON THE INTERFACE BEFORE THE CONTROLLER PICKS IT UP
653                 /
654 0233 66001317 RECAL    CA : UNIT                   / TRY TO CONNECT DRIVE.
655 0234 66001547          CA : SWAIT                  / SEE IF THE DRIVE WORKS.
656 0235 07624004          DO : TGBUS  ←   RCCOM,L     / YES, PUT OUT RECALIBRATE COMMAND.
657 0236 66001641          CA : STROB
658 0237 66001674          CA : WTIO                   / UPDATE THE TIO REGISTER.
659 0240 64000040          BR : POLL1                  / POLL INTERFACES WHILE WAITING.
660                 /
661                 /
662                 /  THE SEEK COMMAND ACCEPTS TWO ADDRESS WORDS FROM
663                 /  THE CPU.  THE FIRST IS THE CYLINDER ADDRESS (16
664                 /  BITS) AND THE SECOND IS THE HEAD (UPPER BYTE)-
665                 /  SECTOR (LOWER BYTE) ADDRESS.  THEY ARE STORED
666                 /  IN CONTROLLER REGISTERS CYLAD AND HSAD AS WELL AS
667                 /  BEING SENT TO THE DISC DRIVE.
668                 /
669 0241 66001317 SEEK     CA : UNIT                   / TRY TO CONNECT DRIVE.
670 0242 66000272          CA : RCORD                  / GET CYLAD AND HSAD.
671 0243 66000247          CA : SEEK1                  / GO OUTPUT THE SEEK.
672 0244 66001674          CA : WTIO                   / UPDATE 3000 STATUS REGISTER.
673 0245 66001623          CA : SRQ                    / SRQ 3000 FOR NEXT ORDER.
674 0246 64000040          BR : POLL1                  / RETURN TO POLL LOOP
675                 /
676                 /
677                 /  SUBROUTINE SEEK1 DOES THE ACTUAL SEEK COMMAND FOR THE SEEK AND
678                 /  COLD LOAD READ COMMANDS   IT IS SEPARATED OUT SO THAT THE
679                 /  AUTOMATIC TRACK SWITCHING ROUTINES CAN CALL IT AND THEN WAIT
680                 /  FOR SEEK COMPLETION.  THE USER-CALLABLE SEEK COMMAND PROCESSOR
681                 /  (MIDDLE OF PAGE) RETURNS TO THE POLL LOOP AFTER THE SEEK IS
682                 /  ISSUED
683                 /    SEEK1 IS A TWO-LEVEL SUBROUTINE WITH THREE ENTRY POINTS,
684                 /  SEEK1, SEEK2, AND SEEK3   SEEK1 CHECKS DISC STATUS, THEN
685                 /  SEEKS TO CYLAD AND HSAD   SEEK2 AND SEEK3 ARE ONE-LEVEL
686                 /  SUBROUTINES USED BY "SPARE" AND "DECS2"
687                 /
688 0247 66001551 SEEK1    CA : GSTAT                  / SEE IF DRIVE
689 0250 27422002       DUMMY = 2     AND  BUF2 ,L    /   WILL RESPOND
690 0251 44400000          CC = TNZRO                 /   AND IF NOT,
691 0252 64001761          BR : STER                  /   SET STATUS-2 ERROR AND QUIT
692 0253 15201311          DO : CBUF   ←   CYLAD,C    / PUT OUT CYLINDER ADDRESS
693 0254 07624007          DO : TGBUS  ←   SEEKC,L    /   AND SEEK COMMAND
694 0255 66001641          CA : STROB                 /   AND STROBE IT OUT
695 0256 07603777          DO : NWTRK  ←   FALSE,U    / CLEAR NEW TRACK FLAG HERE (FOR
696                                                   /   BOOT CMD, NO CLR FOR DECS2)
697 0257 66000320          CA : GDTYP                 / GET DRIVE TYPE FOR OUTA1
698 0260 37616270 SEEK2  BUF3 =       PASS HSAD      / SET UP FOR OUTA1, SEEK3.
699 0261 07605777 SEEK3    DO : EOC    ←   FALSE,U    / CLEAR END-OF-CYLINDER FLAG.
700 0262 07624006          DO : TGBUS  ←   ADREC,L    / DRIVE ADDRESS RECORD COMMAND.
701 0263 64001727          BR : OUTA1                 / SEND IT TO DRIVE.
```

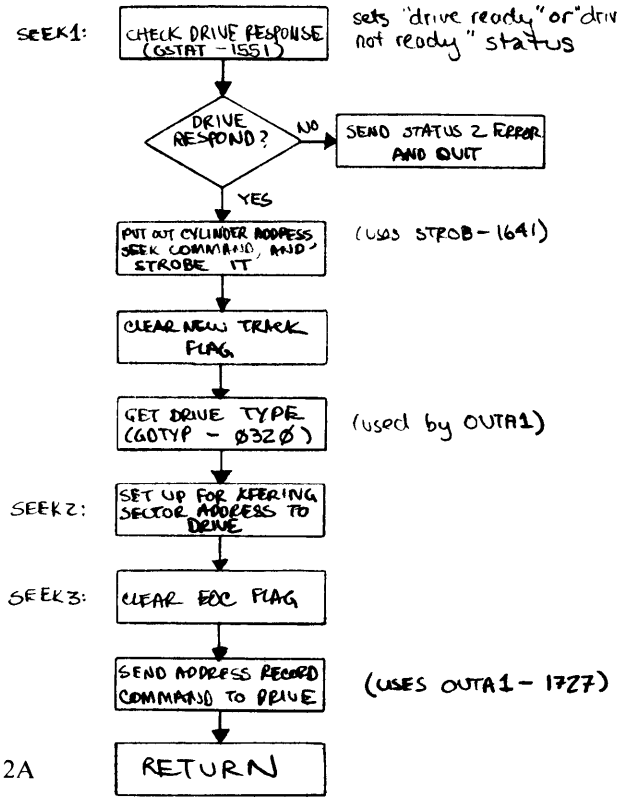
RECALIBRATE COMMAND
(RESTORE HOME)



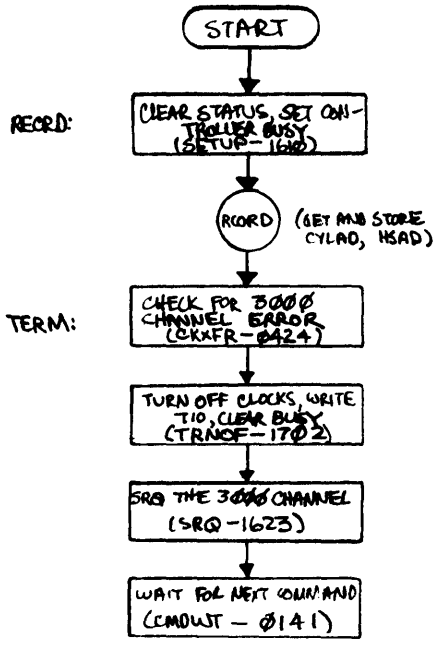
Addresses desired unit, resets it to cylinder Ø, then releases the unit (CPU must wait for an interrupt, or else the command can be overwritten before being accepted by the controller).

SEEK COMMAND

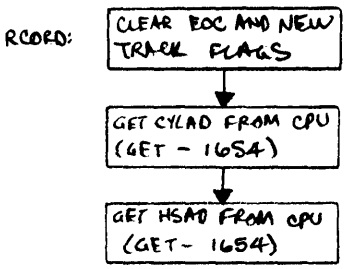




ADDRESS RECORD COMMAND (TERM, RCORD)



Only controller gets cylinder, head, and sector addresses (not the drive)



(does actual work, also called by SEEK command)

Note: TERM is the normal completion point of controller operations that don't disconnect current CPU (i.e. all commands except END and SEEK).

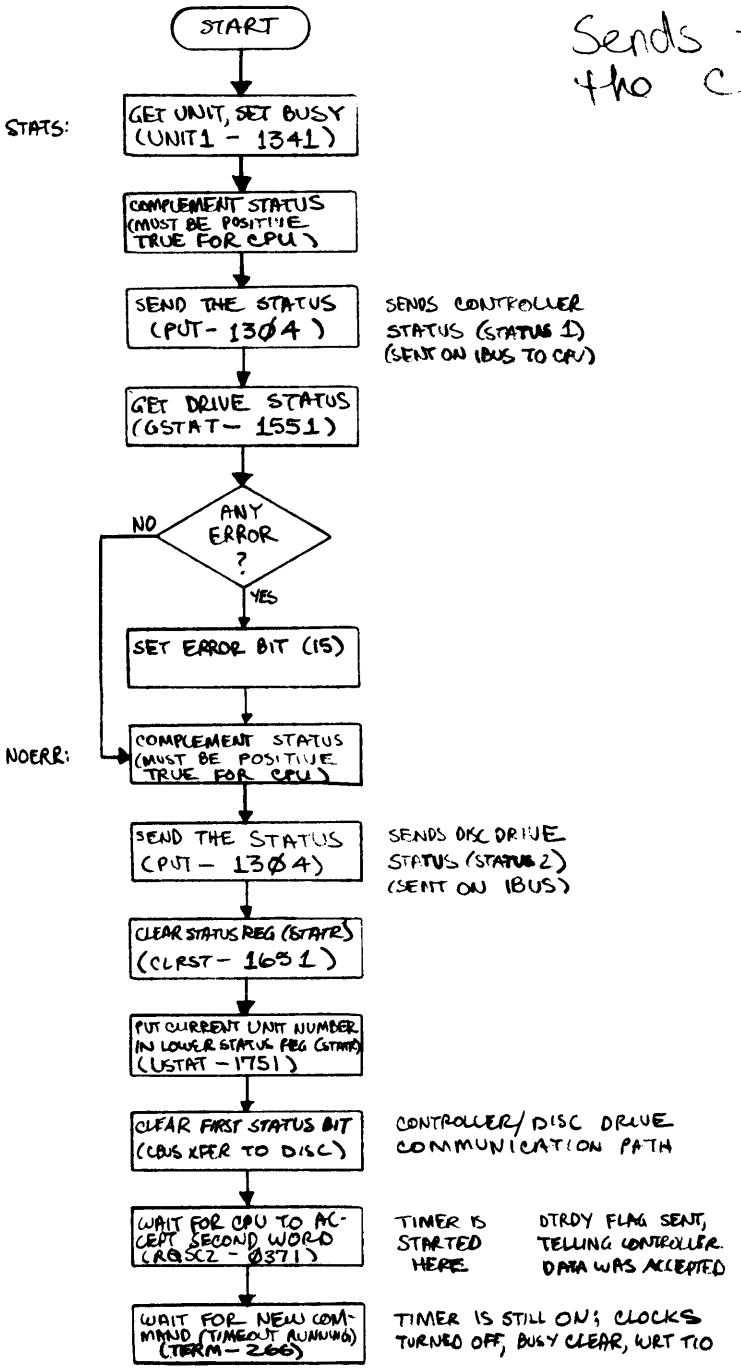
```
                          ADDRESS RECORD COMMAND, TERM, RCORD
                /
                /
                /
                /
                /  ACCEPTS TWO ADDRESS WORDS AS IN "SEEK" COMMAND, BUT PLACES
                /  THEM ONLY IN CYLAD AND HSAD (NOT TRANSMITTED TO DRIVE)
                /
0264 66001610 RECRD     CA : SETUP                  / CLEAR STATUS, SET CONTROLLER BUSY
0265 66000272           CA : RCORD                  / GET AND STORE CYLAD AND HSAD
                                                    / FALL INTO TERM.
                /
                /
                /  TERM IS THE NORMAL COMPLETION POINT OF CONTROLLER OPERATIONS
                /  WHICH CANNOT ALLOW THE CURRENT CPU TO BE DISCONNECTED, NAMELY
                /  ALL OPERATIONS EXCEPT "END" COMMANDS OR WAITING FOR "SEEK" AND
                /  "RECALIBRATE COMMANDS TO BE COMPLETED   THE "END" COMMAND ALLOWS
                /  THE SOFTWARE DRIVER TO DETERMINE WHEN TO RELEASE THE CONTROLLER
                /  AND LET IT RESUME POLLING OF OTHER INTERFACES.  OPERATIONS WHICH
                /  COMPLETE AT TERM REQUIRE A 3000 SRQ BUT NO 2100 DATA FLAG.
                /
0266 66000424 TERM      CA : CKXFR                  / CHECK FOR 3000 CHANNEL ERROR.
0267 66001702           CA : TRNOF                  / CLOCKS OFF, WRT TID, CLEAR BUSY
0270 66001623           CA : SRQ                    / SRQ THE 3000 CHANNEL.
0271 64000141           BR : CMDWT                  / GO WAIT FOR NEXT COMMAND
                /
                /
                /  SUBROUTINE RCORD DOES THE ACTUAL WORK OF THE ADDRESS RECORD
                /  COMMAND   IT IS SEPARATED OUT BECAUSE IT IS ALSO CALLED BY SEEK.
                /
0272 07605777 RCORD     DO : EOC    ←   FALSE,U     / CLEAR THE END-OF-CYLINDER
0273 07603777           DO : NWTRK  ←   FALSE,U     /   AND NEW TRACK FLAGS.
0274 66001654           CA : GET                    / GET CYLAD FROM CPU.
0275 34014264       CYLAD =       CMP   BUF1
0276 66001654           CA : GET                    / GET HSAD FROM CPU
0277 34104264        HSAD =       CMP   BUF1
0300 72000000           RT : 0
```

```
                        STATUS COMMAND FORMATS
                /
                /
                /
                /  RETURNS ENCODED TERMINATION STATUS AND UNIT NUMBER IN THE
                /  FOLLOWING FORMAT:
                /
                /       1 1 1 1 1 1
                /       5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0   BIT (2100 NUMBERING)
                /       - - - - - - - - - - - - - - - -
                /      !S P D E E E E E         U U U U!
                /       - - - - - - - - - - - - - - - -
                /
                /       WHERE S = SPARE TRACK.
                /             P = PROTECTED TRACK.
                /             D = DEFECTIVE TRACK.
                /             E = ENCODED TERMINATION STATUS
                /   00  (0000UU)  NO ERROR
                /   01  (000400)  ILLEGAL OPCODE
                /   02  (0010UU)  DRIVE AVAILABLE STATUS (***NOT AN ERROR***)
                /   07  (0034UU)  CYLINDER COMPARE ERROR
                /   10  (0040UU)  UNCORRECTABLE DATA ERROR
                /   11  (0044UU)  HEAD-SECTOR COMPARE ERROR
                /   12  (005000)  I-O PROGRAM ERROR (3000 ONLY)
                /   14  (0060UU)  END OF CYLINDER
                /   16  (0070UU)  DATA OVERRUN
                /   17  (0074UU)  (AFTER DATA OP OR VRFY):  POSS CORRECTABLE DATA ERR
                /   17  (0074UU)  (AFTER REQUEST SYNDROME):  ERROR WAS CORRECTED
                /   20  (1100UU)  ATTEMPT TO DIRECTLY ACCESS SPARE TRACK
                /   21  (0304UU)  TRACK FLAGGED DEFECTIVE & AUTO SPARING NOT ALLOWED
                /   22  (0110UU)  ACCESS NOT READY DURING DATA OPERATION
                /   23  (0114UU)  DISC DRIVE STATUS ERROR
                /   26  (0130UU)  ATTEMPT TO WRITE ON PROT TRACK & FORMAT SWITCH OFF
                /   27  (0134UU)  UNIT UNAVAILABLE
                /   37  (0174UU)  DRIVE ATTENTION
                /
                /            UU = UNIT NUMBER.
                /
                /
                /   RETURNS CURRENT DRIVE STATUS IN THE FOLLOWING FORMAT:
                /
                /      1 1 1 1 1 1
                /      5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0   BIT (2100 NUMBERING)
                /      - - - - - - - - - - - - - - - -
                /     !E     DRV TYP S S S S S S S S S!
                /      - - - - - - - - - - - - - - - -
                /
                /     WHERE S = DYNAMIC UNIT STATUS:
                /               BIT 0  *DRIVE BUSY
                /                   1  *DRIVE NOT READY
                /                   2  *SEEK CHECK
                /                   3   FIRST STATUS
                /                   4  *FAULT
                /                   5   FORMAT
                /                   6   PROTECTED
                /                   7   ATTENTION
                /
                /          DRV TYP = 4 BITS USED TO DETERMINE LAST AVAIL HD & SECT
                /          E = ERROR (TRUE IF ANY BIT MARKED "*" IS TRUE)
```

```
                        STATUS COMMAND
                /
                /
                /
                /
0301 66001341 STATS     CA : UNIT1                      / GET UNIT, SET BUSY
0302 35302660         BUF1 =        CMP   STATR         / MAKE STATUS +TRUE FOR CPU.
0303 66001304           CA : PUT                        /   THEN GIVE IT AWAY
0304 66001551           CA : GSTAT                      / GET DRIVE STATUS.
0305 27422027        DUMMY = 27     AND   BUF2 ,L
0306 44440000           CC = TNZRO             ,RS      /   .ANY ERROR?
0307 64000311           BR : NOERR
0310 26610200         BUF2 = 200    OR    BUF2 ,U       / YES, SET ERROR BIT (BIT 15)
0311 35302260 NOERR   BUF1 =        CMP   BUF2          / NO, MAKE +TRUE FOR CPU
0312 66001304           CA : PUT
0313 66001651           CA : CLRST
0314 66001751           CA : USTAT                      / PUT CURRENT UNIT# IN STATR,L.
0315 07621375           DO : CBUF   -   CFST ,L         / CLEAR FIRST STATUS.
0316 66001606           CA : CST
0317 64000371           BR : RQSC2                      / WAIT FOR CPU TO ACCEPT 2ND WORD.
```

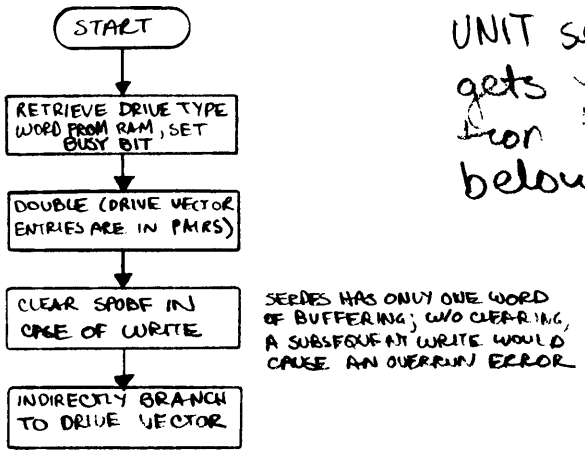
STATUS COMMAND

Sends two status words to the CPU.



SUBROUTINE GDTYP
(Ø32Ø)

GDTYP:



UNIT sets drive type in RAM; GDTYP gets this and provides information to other routines as shown below.

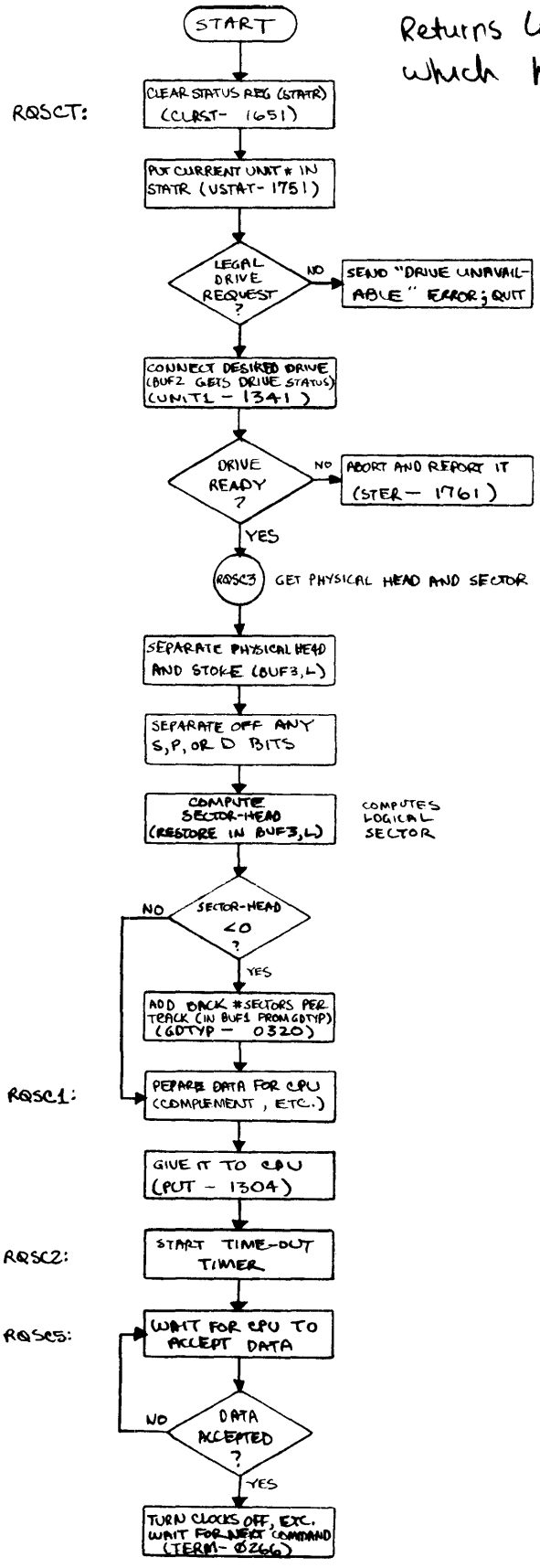
DTW=5:	TYPE	UNSPECIFIED
	LAST HEAD	UNDEFINED
	LAST SECTOR	UNDEFINED
DTW=4:	TYPE	UNSPECIFIED
	LAST HEAD	14
	LAST SECTOR	63
DTW=3:	TYPE	7925
	LAST HEAD	8
	LAST SECTOR	63
DTW=2:	TYPE	7905
	LAST HEAD	2
	LAST SECTOR	47
DTW=1:	TYPE	7920
	LAST HEAD	4
	LAST SECTOR	47
DTW=0:	TYPE	7906
	LAST HEAD	3
	LAST SECTOR	47

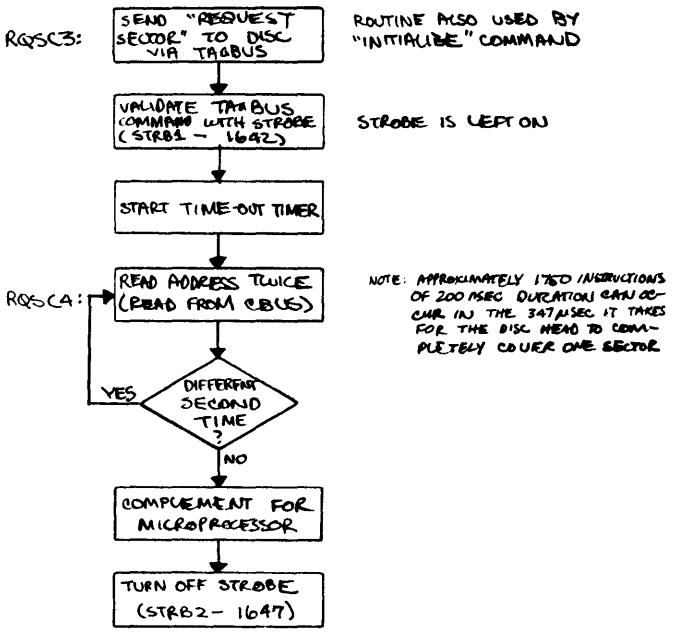
```
818                          SUBROUTINE GDTYP
819                 /
820                 /
821                 /
822                 /
823                 /    SUBROUTINE GDTYP RETRIEVES THE DRIVE TYPE WORD FROM RAM(12)
824                 /  (PLACED THERE BY SUBROUTINE "UNIT")   ON EXIT BUF2,U CONTAINS
825                 /  -(LAST AVAILABLE SURFACE) (TWO'S COMPLEMENT) AND BUF2,L
826                 /  CONTAINS -(LAST AVAILABLE SECTOR) (TWO'S COMPLEMENT).
827                 /    THE MAPPING IS IMPLEMENTED AS A VECTOR SO THAT OTHER DRIVES
828                 /  MAY BE EASILY ADDED   AS OF THIS DATE, THE 7925 (DRIVE TYPE
829                 /  WORD = 3, LAST AVAIL HEAD = 8, LAST AVAIL SECTOR = 63), THE
830                 /  7905A (DRIVE TYPE WORD = 2, LAH = 2, LAS = 47), THE 7920 (DRIVE
831                 /  TYPE WORD = 1, LAH = 4, LAS = 47), THE 7905B (DRIVE TYPE WORD = 0,
832                 /  LAH = 3, LAS = 47), AND TWO ADDITIONAL LARGER CAPACITY DRIVES
833                 /  (DRIVE TYPE WORD = 5, LAH AND LAS NOT DEFINED, AND DRIVE TYPE
834                 /  WORD = 4, LAH = 14, LAS = 63) ARE DEFINED   NOTE THAT CHANGES TO
835                 /  ONE DRIVE TYPE (OR THE ADDITION OF NEW DRIVE TYPES) MAY AFFECT
836                 /  TABLE ENTRIES FOR OTHER DRIVE TYPES.  BE WARNED!!!!!!
837                 /    NOTE:  THIS CODING MUST RESIDE IN ADDRESSES <= 377B
838                 /
839 0320 07620014 GDTYP    DO : RAMAD  ←   DRTYP,L     / RETRIEVE THE
840 0321 10020442          DI : BUF2   ←   RAM  ,L     /   DRIVE TYPE WORD
841 0322 36430140        BUF2 =        PASS BUF2 ,L,SL / MUST DOUBLE BECAUSE DRIVE
842 0323 21560343        REGO = DVECT SUB   BUF2 ,L    /   VECTOR ENTRIES ARE IN PAIRS
843 0324 27610000        BUF2 = 0      PASS       ,U    / MUST CLEAR BUF2 FOR
844 0325 27630000        BUF2 = 0      PASS       ,L    /   TABLE TO WORK PROPERLY
845 0326 15206241          DO : SPOBF  ←   BUF2 ,C     / CLEAR SPOBF IN CASE OF WRITE.
846 0327 34020000          NO : REGO             ,L
847 0330 74000000          BR : I                      / BRANCH TO DRIVE VECTOR.
848                 /
849 0331 22210000        BUF2 = 0      PLUS BUF2 ,U    / DTW = 5, LAST HEAD UNDEFINED,
850 0332 22230000        BUF2 = 0      PLUS BUF2 ,L    /   LAST SECTOR UNDEFINED.
851 0333 22210372        BUF2 = 372    PLUS BUF2 ,U    / DTW = 4, LAST HEAD = 14,
852 0334 22230000        BUF2 = 0      PLUS BUF2 ,L    /   LAST SECTOR = 63.
853 0335 22210372        BUF2 = 372    PLUS BUF2 ,U    / 7925 -- LAST HEAD = 8,
854 0336 22230360        BUF2 = 360    PLUS BUF2 ,L    /   LAST SECTOR = 63.
855 0337 22210002        BUF2 = 2      PLUS BUF2 ,U    / 7905A -- LAST HEAD = 2,
856 0340 22230000        BUF2 = 0      PLUS BUF2 ,L    /   LAST SECTOR = 47
857 0341 22210377        BUF2 = 377    PLUS BUF2 ,U    / 7920 -- LAST HEAD = 4,
858 0342 22230000        BUF2 = 0      PLUS BUF2 ,L    /   LAST SECTOR = 47
859 0343 22210375 DVECT  BUF2 = 375    PLUS BUF2 ,U    / 7905B -- LAST HEAD = 3,
860 0344 22230321        BUF2 = 321    PLUS BUF2 ,L    /   LAST SECTOR = 47.
861 0345 72000000          RT : 0
```

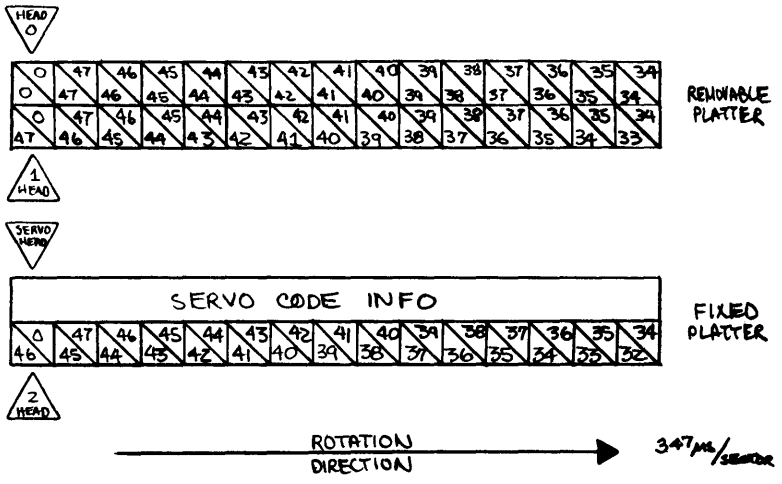
```
862                          REQUEST SECTOR COMMAND
863                 /
864                 /
865                 /
866                 /
867                 /  THIS COMMAND RETURNS THE ADDRESS OF THE SECTOR
868                 /  OVER WHICH THE HEADS ARE POSITIONED WHEN THE
869                 /  COMMAND IS ISSUED.  THE DISC DRIVE RETURNS THE PHYSICAL SECTOR
870                 /  ADDRESS, WHICH WE MUST CONVERT TO THE LOGICAL ADDRESS BEFORE
871                 /  SENDING IT OFF TO THE CPU.
872                 /
873 0346 66001651 RQSCT     CA : CLRST                  / CLEAR THE STATUS REGISTER.
874 0347 66001751          CA : USTAT                  / PUT CURRENT UNIT# IN STATR,L,
875                                                     /   CHECK FOR LEGAL DRIVE REQUEST.
876 0350 66001341          CA : UNIT1                  / CONNECT THE DESIRED DRIVE.
877 0351 27422002       DUMMY = 2      AND  BUF2 ,L     / CONTINUE ONLY IF DRIVE IS READY.
878                                                     /   (BUF2 HAS DRV STAT AFTER UNIT1).
879 0352 44400000          CC = TNZRO
880 0353 64001761          BR : STER                   / NOT READY, ABORT AND REPORT IT.
881 0354 66000375          CA : RQSC3                  / O.K., GET PHYSICAL HEAD AND SECTOR.
882 0355 37616210        BUF3 =       PASS HSAD ,SW    / PUT LOGICAL HEAD IN BUF3,L.
883 0356 27437437        BUF3 = 37    AND  BUF3 ,L     / KILL ANY S, P, OR D BITS
884 0357 31477464        BUF3 = BUF1  SUB  BUF3 ,L     / TAKE SECTOR - HEAD
885 0360 44100000          CC = LOVER                  / IS THAT < 0?
886 0361 64000366          BR : RQSC1                  / NO, SAFE TO SEND IT
887 0362 66000320          CA : GDTYP                  / YES, SO MUST ADD BACK
888 0363 35230060        BUF2 =       CMP  BUF2 ,L     /   NUMBER OF SECTORS PER TRACK.
889 0364 22322002        BUF1 = 2     PLUS BUF2 ,L     / BUF1 = # SECTORS PER TRACK.
890 0365 32237464        BUF3 = BUF1  PLUS BUF3 ,L
891 0366 27702377 RQSC1  BUF1 = 377   PASS      ,U     / ZERO TOP HALF OF BUF1.
892 0367 35323460        BUF1 =       CMP  BUF3 ,L     / COMPLEMENT LOW BUF3 INTO BUF1
893 0370 66001304          CA : PUT                    / GIVE IT TO CPU
894 0371 07600500 RQSC2    DO : TIMER  ←   START,U     / RUN TIMER WHILE
895 0372 42100000 RQSC5    CC = DTRDY                  /   WAITING FOR CPU
896 0373 64000372          BR : RQSC5                  /   TO ACCEPT DATA.
897 0374 64000266          BR : TERM                   / TERM CALLS TRNOF TO STOP TIMER.
898                 /
899                 /
900                 /  SUBROUTINE RQSC3 IS SEPARATED OUT FROM THE REST OF THE REQUEST
901                 /  SECTOR COMMAND SO THAT THE INITIALIZE COMMAND MAY ALSO USE IT
902                 /  TO GET THE PHYSICAL HEAD ADDRESS FROM THE DRIVE.
903                 /
904 0375 07624011 RQSC3     DO : TGBUS  ←   RSCOM,L     / SEND "REQUEST SECTOR" TO DISC.
905 0376 66001642          CA : STRB1                  / VALIDATE IT, LEAVE STROBE ON.
906 0377 07600500          DO : TIMER  ←   START,U     / TURN ON TIME-OUT CIRCUIT
907 0400 10102204 RQSC4    DI : BUF1   ←   CBSIN       / READ ADDRESS.
908 0401 10002202          DI : BUF2   ←   CBSIN       / READ AGAIN IN CASE IT CHANGED
909 0402 36202264       DUMMY = BUF1   XOR  BUF2
910 0403 44400000          CC = TNZRO
911 0404 64000400          BR : RQSC4                  / IF SO, TRY AGAIN.
912 0405 34102264        BUF1 =       CMP  BUF1       / COMPLEMENT FOR MICROPROCESSOR,
913 0406 64001647          BR : STRB2                  /   TURN OFF STROBE, AND RETURN.
```

REQUEST SECTOR COMMAND

Returns logical address of sector over which heads are currently passing.



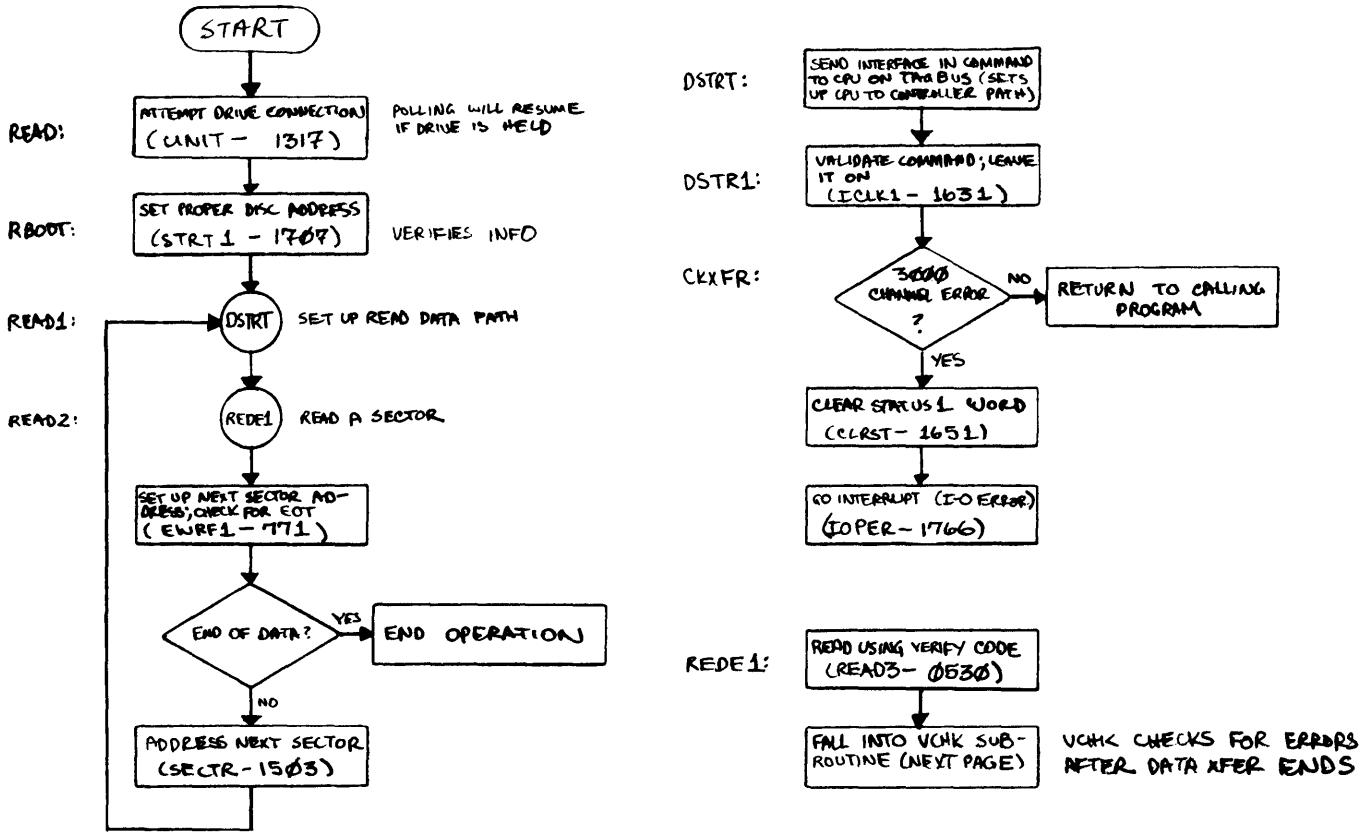




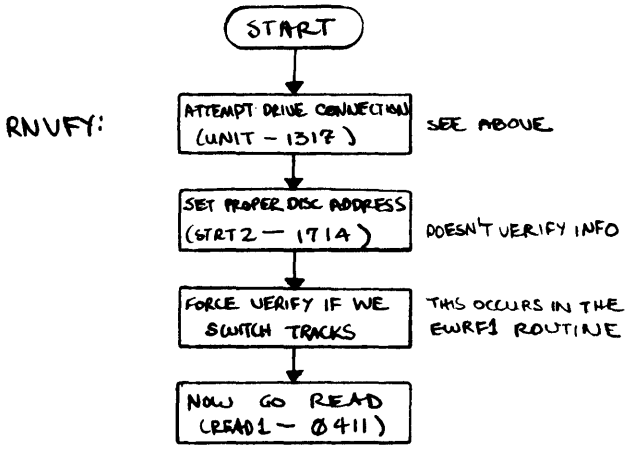
EXAMPLE OF 7905 DISC

PHYSICAL SECTOR / SECTOR LOGICAL

READ



RNVFY



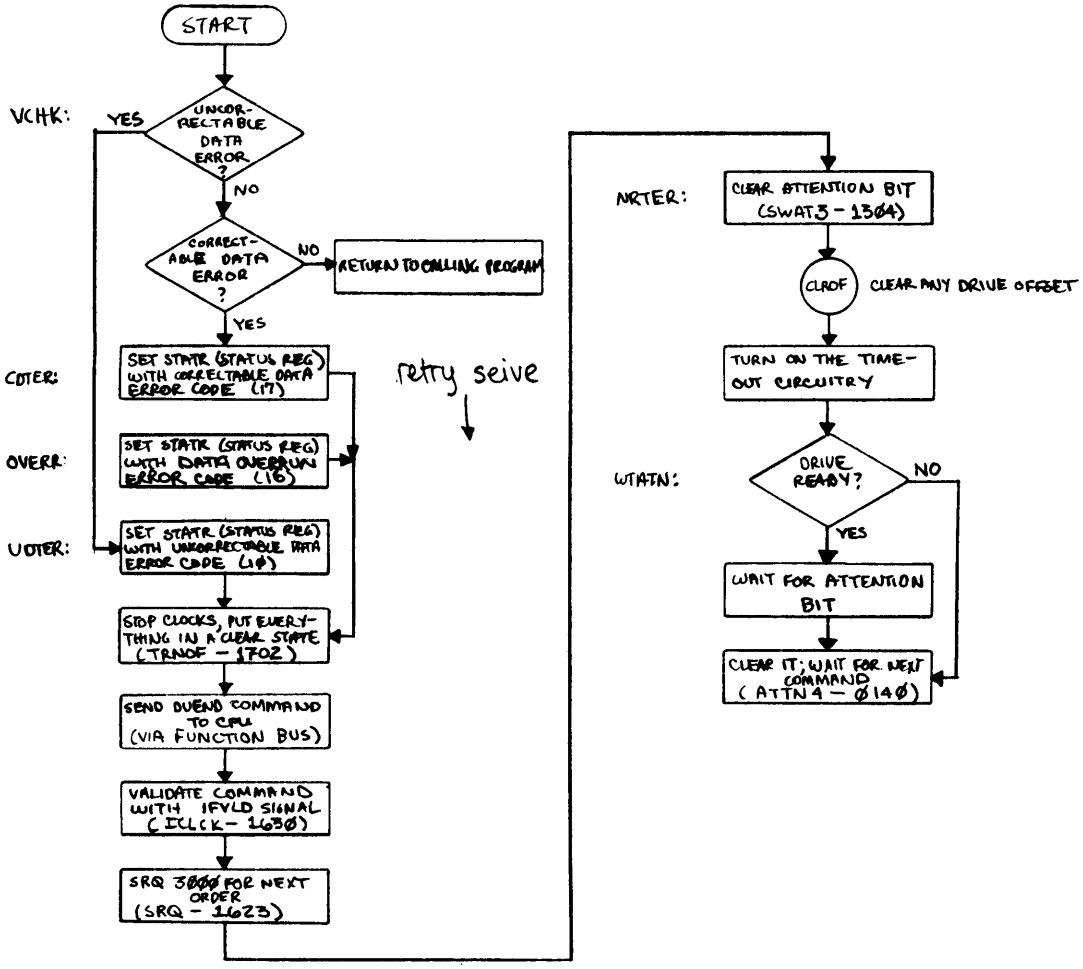
Reads without verification of the preceding sector.

```
914                          READ, RNVFY COMMANDS, SUBROUTINES DSTRT, DSTR1, CKXFR, REDE1
915                  /
916                  /
917                  /
918                  /
919                  /  THE READ COMMAND READS ONE SECTOR AND PASSES THE DATA TO THE CPU.
920                  /  RBOOT IS THE ENTRY POINT USED BY THE COLD LOAD READ COMMAND, AND
921                  /  READ1 IS THE ENTRY POINT USED BY THE READ-WITHOUT-VERIFY COMMAND.
922                  /
923 0407 66001317 READ     CA : UNIT                    / TRY TO CONNECT DRIVE.
924 0410 66001707 RBOOT    CA : STRT1                   / SET PROPER DISC ADDRESS.
925 0411 66000422 READ1    CA : DSTRT                   / GO SET UP READ DATA PATH.
926 0412 66000430 READ2    CA : REDE1                   / THEN GO READ A SECTOR.
927 0413 66000771          CA : EWRF1                   / SET UP NEXT SECTOR ADDRESS,
928                                                     /   CHECK FOR END OF TRANSFER.
929 0414 66001503          CA : SECTR                   / NOT THE END, ACCESS NEXT SECTOR.
930 0415 64000411          BR : READ1                   / THEN GO BACK AND READ IT.
931                  /
932                  /
933                  /  THIS COMMAND READS THE ADDRESSED SECTOR WITHOUT VERIFICATION
934                  /  OF THE PRECEDING SECTOR.  IT IS INTENDED AS THE CONTINUATION
935                  /  PORTION OF A WRAPAROUND READ AND MUST BE USED WITH CAUTION
936                  /  SINCE NO SAFEGUARDS AGAINST ADDRESS OR TRACK STATUS ERRORS ARE
937                  /  PROVIDED.  THE ADDRESS AND TRACK STATUS WILL BE VERIFIED,
938                  /  HOWEVER, IF THE TRANSFER CONTINUES BEYOND A TRACK BOUNDARY
939                  /
940 0416 66001317 RNVFY    CA : UNIT                    / TRY TO CONNECT DRIVE.
941 0417 66001714          CA : STRT2                   / SET PROPER DISC ADDRESS.
942 0420 07623377          DO : INITL  ←   FALSE,L      / FORCE VERIFY IF WE SWITCH TRACKS
943 0421 64000411          BR : READ1                   / NOW GO READ.
944                  /
945                  /
946                  /  SUBROUTINE DSTRT SETS UP THE READ DATA PATH TO THE INTERFACE.
947                  /  IT IS SEPARATED OUT SO THAT IFNBF PROP TIME ONLY OCCURS AT
948                  /  THE START OF TRANSFER, NOT BETWEEN SECTORS.  THE ENTRY POINT
949                  /  AT DSTR1 IS USED BY THE INIT, WRITE, AND WFS ROUTINES   FOR
950                  /  THESE ROUTINES, IFNBF IS SET TO IFOUT
951                  /
952 0422 07622443 DSTRT    DO : IFNBF  ←   IFIN ,L      / SET UP INTERFACE DATA PATH.
953 0423 66001631 DSTR1    CA : ICLK1                   / VALIDATE COMMAND, LEAVE IT ON.
954                                                     / FALL INTO CKXFR.
955                  /
956                  /
957                  /  SUBROUTINE CKXFR CHECKS THE 3000 I-O CHANNEL ERROR FLAG.
958                  /
959 0424 42340000 CKXFR    CC = XFRNG            ,RS    / ANY ERROR IN THE 3000 CHANNEL?
960 0425 72000000          RT : 0                       / NO, RETURN.
961 0426 66001651          CA : CLRST                   / YES, CLEAR THE STATUS-1 WORD
962 0427 64001766          BR : IOPER                   / GO INTERRUPT - I-O PROG ERR.
963                  /
964                  /
965                  /  SUBROUTINE REDE1 TRANSFERS ONE SECTOR FROM DISC TO CPU.  IT
966                  /  IS CALLED AFTER THE DATA PATH IS SET UP BY DSTRT.
967                  /
968 0430 66000530 REDE1    CA : READ3                   / READ USING VRFY CODE.
969                                                     / THEN FALL INTO VCHK.
```

```
                        SUBROUTINES VCHK, CLROF; RETRYABLE ERROR STATUS SIEVE
                /
                /
                /
                /
                /  DATA TRANSFER IS FINISHED   NOW CHECK FOR ERRORS
                /
0431 44040000 VCHK      CC = UNCOR              ,RS    / THE ULTIMATE SIN--
0432 64000437           BR : UDTER                     /   UNCORRECTABLE
0433 43300000           CC = ANYER                     / ANY OTHER ERROR (CORRECTABLE)?
0434 72000000           RT : 0                         / NO, RETURN
                                                       / YES, FALL INTO RETRY SIEVE.
                /
                /
                /    ON DATA ERROR OR OVERRUN, THE SIGNAL DVEND (DEVICE END)
                /  INCREMENTS A RETRY COUNTER ON THE 3000 INTERFACE AND CAUSES
                /  THE INTERFACE TO SIGNAL "DEVICE END" TO THE CHANNEL
                /  EXCEPTION:  IF THE COUNTER ROLLS OVER (OUT OF RETRIES) THE
                /  INTERFACE INTERRUPTS THE CPU   ON A 2100 INTERFACE, DVEND
                /  SETS THE FLAG, ALWAYS CAUSING AN INTERRUPT
                /    THE ENTRY POINT AT NRTER IS FROM THE NON-RETRYABLE ERROR
                /  SIEVE.  WE CLEAR ANY DRIVE OFFSET AT THIS POINT, SINCE WE
                /  MAY HAVE HAD AN ERROR ABORT FROM A READ WITH OFFSET COMMAND
                /  CLEARING THE DRIVE OFFSET GENERATES A DRIVE ATTENTION, SO
                /  WE WAIT FOR THAT AND THEN CLEAR IT TO AVOID CONFUSING THE
                /  USER WITH A POSSIBLE EXTRA ATTENTION
                /
0435 22212401 CDTER STATR = 1      PLUS STATR,U     / CORRECTABLE DATA ERROR    (17)
0436 22212406 OVERR STATR = 6      PLUS STATR,U     / DATA OVERRUN              (16)
0437 22212410 UDTER STATR = 10     PLUS STATR,U     / UNCORRECTABLE DATA ERROR  (10)
0440 66001702           CA : TRHOF                  / PUT EVERYTHING IN A KNOWN STATE.
0441 07622672           DO : IFNBF  ←   DVEND,L     / THEN BUMP COUNTER ON 3000 INTERFACE
                                                    /   (OR SET FLAG ON 2100 INTERFACE)
0442 66001630           CA : ICLCK                  / VALIDATE THE COMMAND
0443 66001623           CA : SRQ                    / NOW SRQ 3000 FOR NEXT ORDER
0444 66001604 NRTER     CA : SWAT3                  / CLEAR ATTENTION BIT
0445 66000454           CA : CLROF                  / CLEAR ANY DRIVE OFFSET
0446 07600500           DO : TIMER  ←   START,U     / TURN ON TIME-OUT CIRCUIT
0447 66001551 WTATN     CA : GSTAT                  / WAIT FOR ATTENTION BIT
0450 27422202       DUMMY = 202   AND   BUF2 ,L     /   FROM DRIVE (ONLY IF
0451 44440000           CC = TM2RO          ,RS     /   DRIVE IS READY)
0452 64000447           BR : WTATN
0453 64000140           BR : ATTN4                  / GO CLEAR IT AND WAIT
                                                    /   FOR THE NEXT COMMAND
                /
                /
                /  SUBROUTINE CLROF CLEARS THE DRIVE OFFSET   IT IS CALLED FOR
                /  NORMAL COMPLETION OF THE ROFST COMMAND, AND IS ALSO CALLED
                /  BY THE ERROR INTERRUPT PROCESSOR IN CASE A READ-WITH-OFFSET
                /  COMMAND WAS ABORTED BEFORE NORMAL COMPLETION
                /
0454 07624002 CLROF     DO : TGBUS  ←   OFFST,L     / PUT OUT OFFSET COMMAND
0455 07621377           DO : CBUF   ←   377  ,L     / OFFSET PARAMETER = 0
0456 07602777           DO : CLKOF  ←   377  ,U     / ALSO TURN OFF SEPARATOR OFFSET
0457 64001641           BR : STROB
```

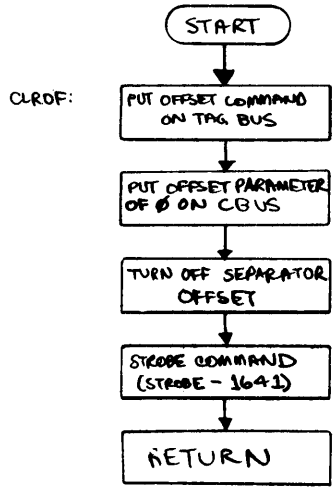
SUBROUTINE VCHK

(RETRYABLE ERROR STATUS SIEVE)

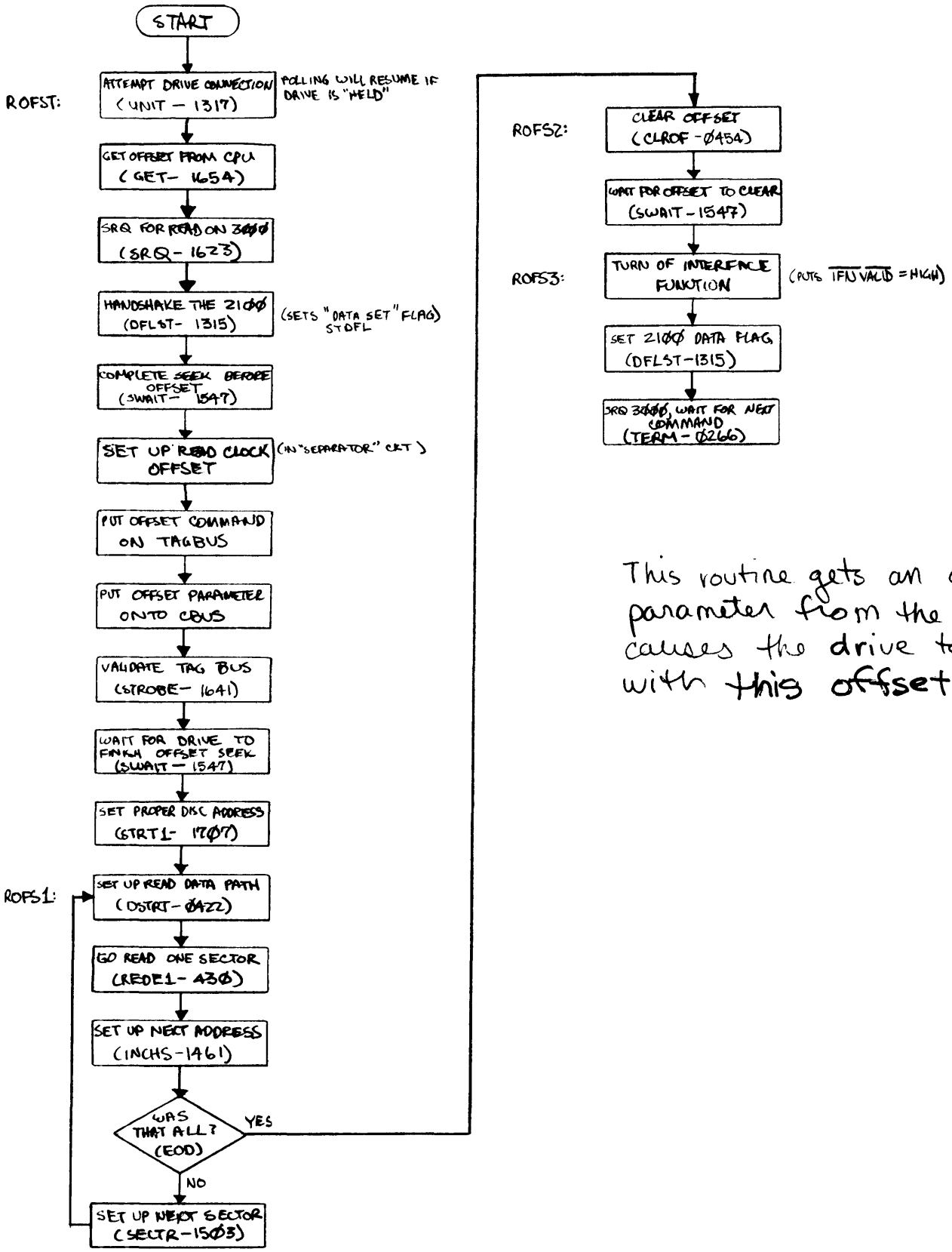


SUBROUTINE CLROF

(CLEARS DRIVE OFFSET)



READ WITH OFFSET

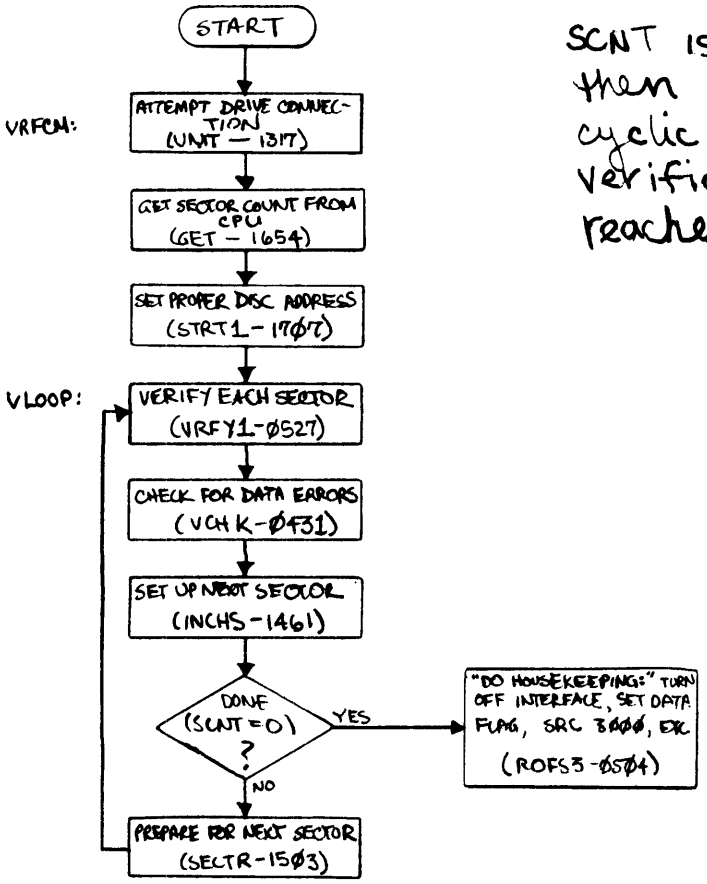


This routine gets an offset parameter from the CPU, causes the drive to read with this offset.

```
1025                          READ WITH OFFSET COMMAND
1026                  /
1027                  /  THIS COMMAND REQUESTS AN OFFSET PARAMETER FROM THE CPU AND
1028                  /  COMMANDS THE DRIVE TO OFFSET THE HEADS FROM TRACK CENTER
1029                  /  THE OFFSET IS REMOVED AT COMMAND COMPLETION, IF A CONTROLLER-
1030                  /  GENERATED SEEK OCCURS (AUTOMATIC TRACK SWITCHING AT END OF
1031                  /  TRACK OR SPARE TRACK ACCESS), OR IF AN ERROR OCCURS   THIS COMMAND IS
1032                  /  USED ONLY IN ERROR RE-READ SITUATIONS.  NOTE THAT SPARE TRACKS CANNOT
1033                  /  BE READ WITH OFFSET   THE REASONING IS AS FOLLOWS:
1034                  /    1   A SEEK BY THE DRIVE REMOVES ANY OFFSET, THEREFORE TO READ A SPARE
1035                  /  TRACK WITH OFFSET THE OFFSET MUST BE APPLIED AFTER THE SPARE TRACK IS
1036                  /  REACHED
1037                  /    2   THE OFFSET PARAMETER MUST BE READ IN BEFORE THE STRT1 ROUTINE IS
1038                  /  CALLED   THIS IS BECAUSE THE SOFTWARE EXPECTS TO SEE A HANDSHAKE FLAG
1039                  /  ON THE INTERFACE WHEN THE OFFSET PARAMETER IS ACCEPTED, SO THAT IT CAN
1040                  /  PROPERLY START UP DMA   SINCE THERE ARE ERROR INTERRUPT EXITS FROM STRT1
1041                  /  (WHICH ALSO SET THE INTERFACE FLAG), THE SOFTWARE WILL ASSUME THIS ERROR
1042                  /  FLAG IS REQUESTING THE PARAMETER RATHER THAN TERMINATING THE COMMAND,
1043                  /  UNLESS THE PARAMETER HAS ALREADY BEEN READ IN.
1044                  /    3   THE STRT1 ROUTINE (AND THE SUBROUTINES CALLED BY STRT1) USE ALL 8
1045                  /  WORKING REGISTERS IN THE MICROPROCESSOR   THERE IS NO PLACE TO STORE THE
1046                  /  OFFSET PARAMETER DURING STRT1
1047                  /    4   THEREFORE THE OFFSET PARAMETER MUST BE REQUESTED FROM THE INTERFACE
1048                  /  AND SENT TO THE DRIVE BEFORE STRT1 IS CALLED, TO REMOVE THE INTERFACE
1049                  /  FLAG AMBIGUITY   BUT THIS MEANS THAT ANY CONTROLLER-GENERATED SEEK TO A
1050                  /  SPARE TRACK WILL REMOVE THE OFFSET   HENCE SPARE TRACKS CANNOT BE READ
1051                  /  WITH OFFSET
1052                  /
1053 0460 66001317 ROFST    CA : UNIT                  / TRY TO CONNECT DRIVE
1054 0461 66001654          CA : GET                   / GET OFFSET FROM CPU
1055 0462 66001623          CA : SRQ                   / SRQ FOR READ ON 3000
1056 0463 66001315          CA : DFLST                 / HANDSHAKE THE 2100 ALSO.
1057 0464 66001547          CA : SWAIT                 / COMPLETE SEEK BEFORE OFFSETTING.
1058 0465 17602445          DO : CLKOF  ←   BUF1 ,U    / SET UP READ CLOCK OFFSET
1059 0466 07624002          DO : TGBUS  ←   OFFST,L    / PREPARE OFFSET COMMAND
1060 0467 17600705          DO : CBUF   ←   BUF1       /   AND THE PARAMETER.
1061 0470 66001641          CA : STROB                 / SEND THEM TO THE DRIVE
1062 0471 66001547          CA : SWAIT                 / WAIT FOR DRIVE TO FINISH OFFSET
1063 0472 66001707          CA : STRT1                 / SET PROPER DISC ADDRESS.
1064 0473 66000422 ROFS1    CA : DSTRT                 / GO SET UP READ DATA PATH
1065 0474 66000430          CA : READ1                 / NOW GO READ ONE SECTOR
1066 0475 66001461          CA : INCHS                 / THEN SET UP NEXT ADDRESS
1067 0476 42600000          CC = EOD                   / WAS THAT ALL?
1068 0477 64000502          BR : ROFS2                 / YES, GO CLEAR OFFSET
1069 0500 66001503          CA : SECTR                 / NO, SET UP NEXT SECTOR
1070 0501 64000473          BR : ROFS1                 /   AND GO READ IT
1071                  /
1072 0502 66000454 ROFS2    CA : CLROF                 / ALL DONE, SO CLEAR OFFSET
1073 0503 66001547          CA : SWAIT                 / WAIT FOR OFFSET TO COMPLETE
1074                                                   /   THEN FALL INTO ROFS3.
1075                  /
1076                  /
1077                  /  ROFS3 NOTIFIES THE CPU THAT THE OPERATION IS COMPLETE   THE
1078                  /  HP3000 INTERFACE SERVICE REQUESTS, AND THE 2100 INTERFACE SETS ITS
1079                  /  FLAG
1080                  /
1081 0504 07606001 ROFS3    DO : IFVLD  ←   CLRCL,U    / TURN OFF INTERFACE FUNCTION
1082 0505 66001315          CA : DFLST                 / 2100 FLAG SET HERE.
1083 0506 64000266          BR : TERM                  / 3000 IS SRQ'ED AT TERM
```

```
1084                          VERIFY COMMAND, SUBROUTINES VRFY, VRFY1, VRFY2, READ3
1085                 /
1086                 /
1087                 /
1088                 /
1089                 /  VRFCM PERFORMS AN ADDRESS VERIFICATION
1090                 /  AND CYCLIC CHECK ON EACH SECTOR UNTIL SCNT = 0
1091                 /  SCNT IS REQUESTED FROM THE CPU AT THE BEGINNING
1092                 /  OF THE OPERATION.
1093                 /
1094                 /
1095 0507 66001317 VRFCM    CA : UNIT                    / TRY TO CONNECT DRIVE.
1096 0510 66001654          CA : GET                     / GET SECTOR COUNT FROM CPU
1097 0511 34106264        SCNT =       CMP  BUF1
1098 0512 66001707          CA : STRT1                   / SET PROPER DISC ADDRESS.
1099 0513 66000527 VLOOP    CA : VRFY1                   / NOW VERIFY EACH SECTOR IN TURN,
1100 0514 66000431          CA : VCHK                    /   CHECKING DATA ERRORS
1101 0515 66001461          CA : INCHS                   / SET UP NEXT SECTOR.
1102 0516 30106274        SCNT =       DEC  SCNT        / THEN SEE IF DONE.
1103 0517 44440000          CC = TNZRO           ,RS
1104 0520 64000504          BR : ROFS3                   /    YES, DO HOUSEKEEPING.
1105 0521 66001503          CA : SECTR                   / . .NO, GET READY TO CONTINUE
1106 0522 64000513          BR : VLOOP                   / AND DO THE NEXT ONE
1107                 /
1108                 /
1109                 /
1110                 /
1111                 /  THE FOLLOWING SUBROUTINE IS USED TO RECOVER DATA FROM THE DISC
1112                 /  DURING ALL READ AND VERIFY ROUTINES EXCEPT READ FULL SECTOR
1113                 /  FOUR ENTRY POINTS ARE USED, DEPENDING ON JUST HOW MUCH THE
1114                 /  ROUTINE IS TO DO OTHER THAN READ THE DISC   VRFY1 IS THE ENTRY
1115                 /  POINT THAT CAUSES THE ROUTINE TO PASS DATA THROUGH THE HARDWARE
1116                 /  CRC AND ECC REGISTERS WITHOUT ANY SPARING OPERATIONS, BUT UPDATING
1117                 /  TCYLD AND THSAD   VRFY2 IS THE ENTRY POINT USED FOR SPARING,
1118                 /  SINCE IT SAVES THE TARGET SECTOR ADDRESS AND RESETS THE VERIFY
1119                 /  RETRY COUNTER TO SCRATCH.  VRFY IS THE PRIMARY ENTRY POINT AND
1120                 /  RESETS THE ADDRESS ERROR RETRY BIT AS WELL.  A FOURTH ENTRY POINT
1121                 /  AT READ3 IS CALLED BY ALL THE READ ROUTINES (EXCEPT RFS) TO
1122                 /  TRANSFER DATA TO THE INTERFACE.  THE READ ROUTINES MUST SET UP
1123                 /  THE DATA TRANSFER PATH BEFORE CALLING READ3   NOTE THAT ENTRY
1124                 /  AT VRFY1 OR EARLIER PROHIBITS ANY DATA TRANSFER BECAUSE IFVLD
1125                 /  IS CLEARED
1126                 /    FOLLOWING ANY FLAVOR OF VRFY OR READ3, CALLS TO VCHK CHECK
1127                 /  DATA ERRORS DETECTED DURING EXECUTION, AND A CALL TO SPARE WILL
1128                 /  USE THE INFORMATION SAVED BY VRFY TO ACCESS A SPARE TRACK IF
1129                 /  NECESSARY
1130                 /    TIMING:  DO NOT LESSEN THE NUMBER OF INSTRUCTIONS BETWEEN
1131                 /  READ3 AND READ3+3 OR BETWEEN READ3+3 AND READ3+8   THESE
1132                 /  INSTRUCTIONS ARE SPACED DELIBERATELY TO ALLOW TGBUS AND
1133                 /  COMMAND BUS PROP TIMES, BUT WITHOUT THE ARTIFICIAL DELAY
1134                 /  INTRODUCED BY A CALL TO STRB1   THIS CUTS DOWN ON WASTED
1135                 /  TIME BETWEEN SECTORS OF A MULTIPLE-SECTOR TRANSFER.
```

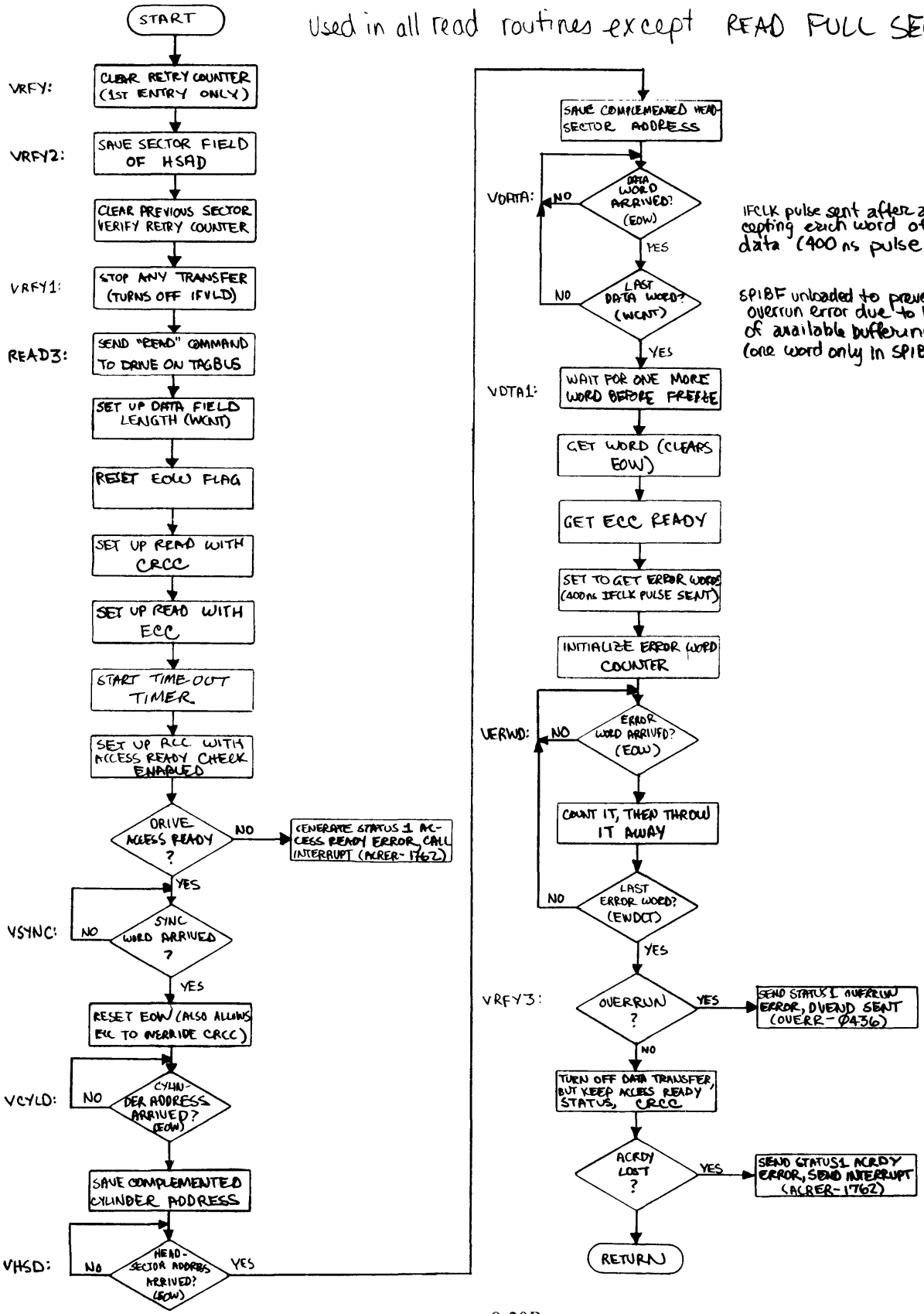
VERIFY COMMAND



SCNT is requested from CPU, then sectors are verified (ie. cyclic check and address verification) until SCNT reaches zero

SUBROUTINES VRFY1, VRFY2, VRFY3

Used in all read routines except READ FULL SECTOR

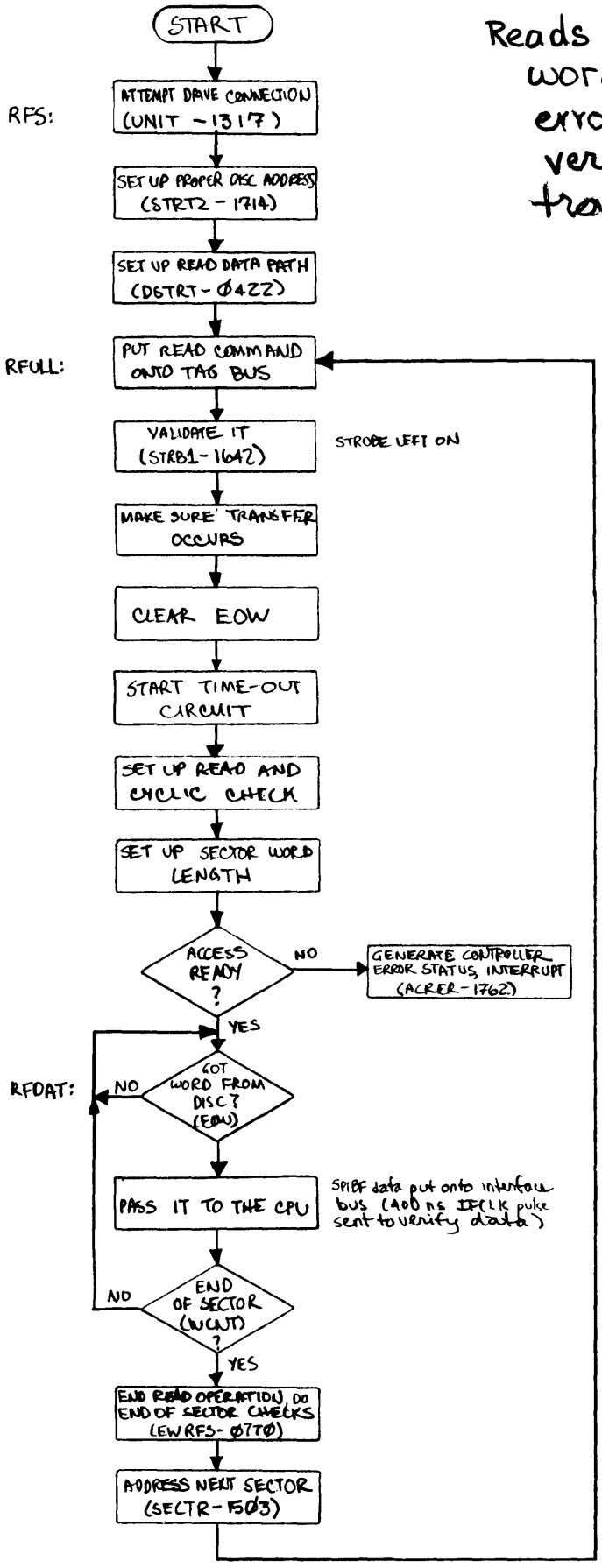


```
1136                          SUBROUTINES VRFY, VRFY1, VRFY2
1137                  /
1138 0523 07623377 VRFY     DO : RETRY  ←   FALSE,L     / CLEAR RETRY ONLY AT 1ST ENTRY
1139 0524 37702210 VRFY2  BUF1 =       PASS HSAD ,SW    / SAVE SECTOR FIELD OF HSAD
1140 0525 07620015          DO : RAMAD  ←   NSEC ,L     / CLEAR PREVIOUS SECTOR VERIFY
1141 0526 07620777          DO : RAM    ←   377  ,L     /   RETRY COUNTER.
1142 0527 07606001 VRFY1    DO : IFVLD  ←   CLRCL,U     / STOP ANY TRANSFER.
1143 0530 07624017 READ3    DO : TGBUS  ←   RDCOM,L     / SEND READ COMMAND TO DRIVE.
1144 0531 27722201        WCNT = RWCT  PASS       ,L    / SET UP DATA FIELD LENGTH.
1145 0532 10007304          DI : DUMMY  ←   SPIBF       / MAKE SURE EOW IS CLEAR.
1146 0533 07604476          DO : INTCW  ←   RCC1 ,U     / READ AND CYCLIC CHECK.
1147 0534 07610226          DO : ECICW  ←   RECC ,U     / READ WITH ECC.
1148 0535 07600500          DO : TIMER  ←   START,U     / TURN ON TIME-OUT CIRCUIT
1149 0536 34000000          NO :                        / ALLOW RCC1 TO SET UP AT DRIVE.
1150 0537 34000000          NO :
1151 0540 07604472          DO : INTCW  ←   RCC2 ,U     / RCC WITH ACRDY CHECK ENABLED.
1152 0541 42440000          CC = ACRDY          ,RS     / DRIVE ACCESS READY?
1153 0542 64001762          BR : ACRER                  / NO, ESCAPE HERE
1154 0543 42240000 VSYNC    CC = EOW            ,RS     / YES, WAIT FOR SYNC WORD
1155 0544 64000543          BR : VSYNC
1156 0545 10107300          DI : REGO   ←   SPIBF       / THIS RESETS EOW BESIDES ALLOW-
1157 0546 17632041          DO : DSYNC  ←   REGO ,L     /   ING ECC TO OVERRIDE CRCC.
1158 0547 42240000 VCYLD    CC = EOW            ,RS     / GET AND SAVE CYLINDER ADDRESS
1159 0550 64000547          BR : VCYLD
1160 0551 10107300          DI : TCYLD  ←   SPIBF
1161 0552 34100260        TCYLD =       CMP   TCYLD       / COMPLEMENT TO GROUND TRUE
1162 0553 42240000 VHSAD    CC = EOW            ,RS     / GET AND SAVE HEAD-SECTOR ADDRESS
1163 0554 64000553          BR : VHSAD
1164 0555 10007302          DI : THSAD  ←   SPIBF
1165 0556 35210260        THSAD =       CMP   THSAD       / COMPLEMENT TO GROUND TRUE
1166 0557 42240000 VDATA    CC = EOW            ,RS     / READ DATA
1167 0560 64000557          BR : VDATA
1168 0561 10007316          DI : BUF3   ←   SPIBF
1169 0562 16401755          DO : IDTBF  ←   BUF3
1170 0563 16401755          DO : IDTBF  ←   BUF3        / (400 NSEC IFCLK PULSE)
1171 0564 33762064        WCNT =        INC   WCNT ,L     / CHECK FOR END OF DATA.
1172 0565 44140000          CC = LOVER          ,RS
1173 0566 64000557          BR : VDATA                  / NOT YET
1174 0567 42240000 VDTA1    CC = EOW            ,RS     / WAIT FOR ONE MORE BEFORE FREEZE.
1175 0570 64000567          BR : VDTA1
1176 0571 10007316          DI : BUF3   ←   SPIBF       / GET WORD, CLEAR EOW
1177 0572 07610200          DO : ECICW  ←   DSC  ,U     / TELL ECC TO GET READY
1178 0573 07604452          DO : INTCW  ←   RERWD,U     / SET TO GET ERROR WORDS
1179 0574 16401755          DO : IDTBF  ←   BUF3
1180 0575 16401755          DO : IDTBF  ←   BUF3        / (400 NSEC IFCLK PULSE)
1181 0576 27722371        EWDCT = ERWCT PASS      ,L    / INITIALIZE ERROR WORD COUNTER
1182 0577 42240000 VERWD    CC = EOW            ,RS     / WAIT FOR ERROR WORD
1183 0600 64000577          BR : VERWD
1184 0601 10007304          DI : DUMMY  ←   SPIBF       / THEN THROW IT AWAY
1185 0602 33762064        EWDCT =       INC   EWDCT,L     / BUT DON'T FORGET TO COUNT IT
1186 0603 44140000          CC = LOVER          ,RS     / LAST ERROR WORD?
1187 0604 64000577          BR : VERWD                  / NO, GO BACK FOR NEXT ONE
1188 0605 42700000 VRFY3    CC = OVRUN                  / YES, A SLOWPOKE OUT THERE?
1189 0606 64000436          BR : OVERR                  / OVERRUN, TOO BAD ABOUT THAT
1190 0607 07604413          DO : INTCW  ←   RDWRT,U     / NO, TURN OFF DATA TRANSFER, BUT
1191                                                    /   KEEP ACRDY STATUS, CRCC
1192 0610 42440000          CC = ACRDY          ,RS     / DRIVE GO NOT READY DURING OP?
1193 0611 64001762          BR : ACRER                  / AIN'T THAT A SHAME!
1194 0612 72000000          RT : 0                      / NO, READ OR VRFY DONE, RETURN
```

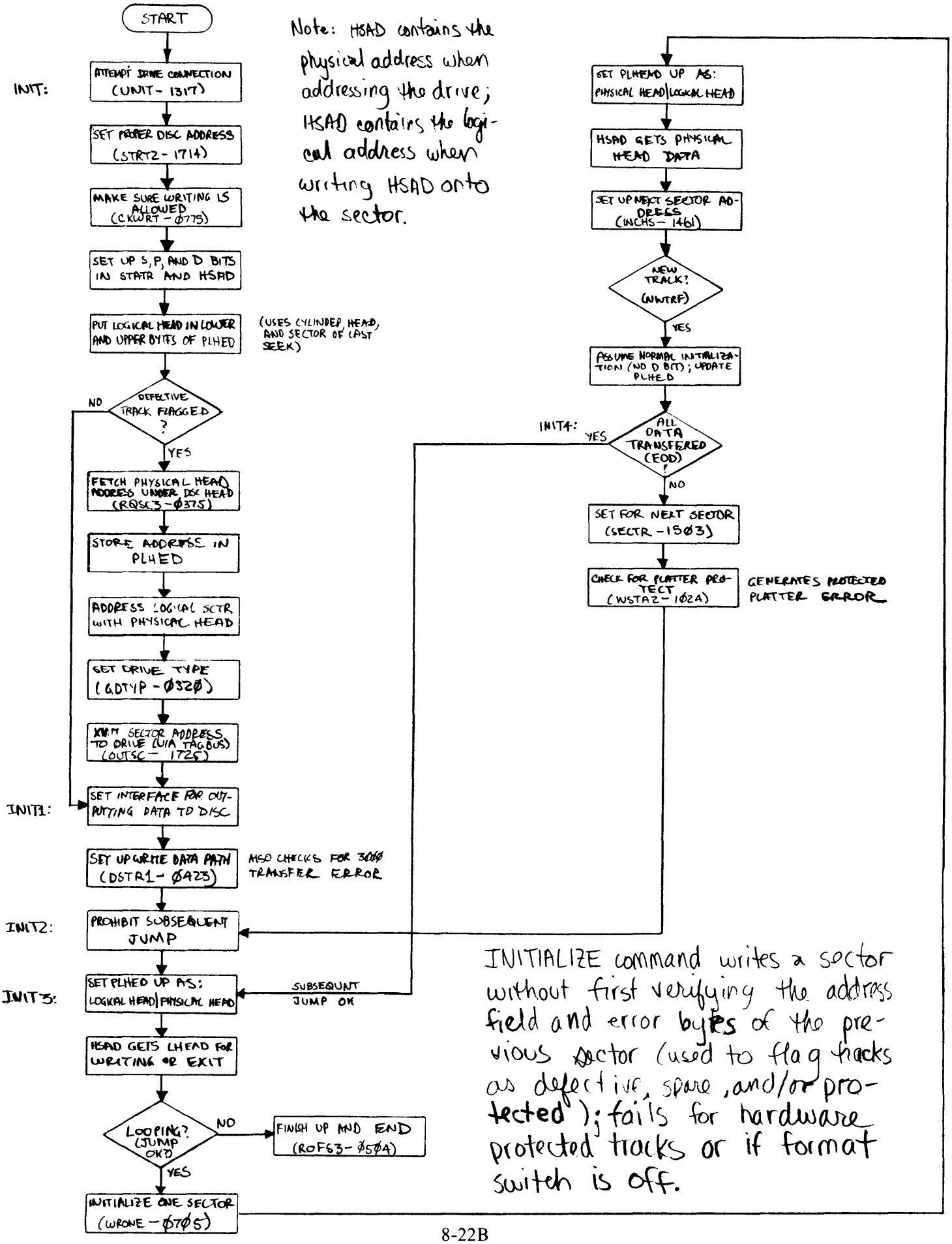
```
1195                          READ FULL SECTOR COMMAND
1196                  /
1197                  /
1198                  /
1199                  /
1200                  /  RFS (READ FULL SECTOR) READS FROM THE DISC AND PASSES
1201                  /  TO THE CPU THE SYNC WORD, THE ADDRESS WORDS, THE DATA,
1202                  /  AND THE ERROR WORDS WITH NO ERROR CHECKING.  THE SECTOR
1203                  /  ADDRESS AND TRACK STATUS ARE NOT VERIFIED
1204                  /
1205 0613 66001317 RFS      CA : UNIT                    / TRY TO CONNECT DRIVE
1206 0614 66001714          CA : STRT2                   / SET PROPER DISC ADDRESS.
1207 0615 66000422          CA : DSTRT                   / GO SET UP READ DATA PATH.
1208 0616 07624017 RFULL    DO : TGBUS  ←   RDCOM,L      / GIVE READ COMMAND TO DRIVE.
1209 0617 66001642          CA : STRB1                   / TURN ON STROBE, LEAVE IT ON.
1210 0620 07606000          DO : IFVLD  ←   SETCL,U      / MAKE SURE TRANSFER OCCURS.
1211 0621 10007304          DI : DUMMY  ←   SPIBF        / MAKE SURE EOW IS CLEAR.
1212 0622 07600500          DO : TIMER  ←   START,U      / TURN ON TIME-OUT CIRCUIT
1213 0623 07604472          DO : INTCW  ←   RCC2 ,U      / READ AND CYCLIC CHECK.
1214 0624 27722166        WCNT = FULSC PASS      ,L      / SET UP SECTOR WORD LENGTH.
1215 0625 42440000          CC = ACRDY           ,RS
1216 0626 64001762          BR : ACRER                   / DRIVE BUSY, ABORT
1217 0627 42240000 RFDAT    CC = EOW             ,RS     / WAIT FOR WORD FROM DISC AND
1218 0630 64000627          BR : RFDAT                   /   PASS IT TO THE CPU.
1219 0631 10007316          DI : BUF3   ←   SPIBF
1220 0632 16401755          DO : IDTBF  ←   BUF3
1221 0633 16401755          DO : IDTBF  ←   BUF3         / (400 NSEC IFCLK PULSE)
1222 0634 33762064        WCNT =        INC  WCNT ,L
1223 0635 44140000          CC = LOVER           ,RS     / END OF SECTOR?
1224 0636 64000627          BR : RFDAT                   / NOT YET
1225 0637 66000770          CA : EWRFS                   / YES, READ OFF, DO END SECTOR CHECKS
1226 0640 66001503          CA : SECTR                   / ADDRESS NEXT SECTOR
1227 0641 64000616          BR : RFULL                   /   AND GO READ IT
```

READ FULL SECTOR

Reads data and error words, sync word, address words, all without error checking and without verifying sector address or track status.



INITIALIZE COMMAND



Note: HSAD contains the physical address when addressing the drive; HSAD contains the logical address when writing HSAD onto the sector.

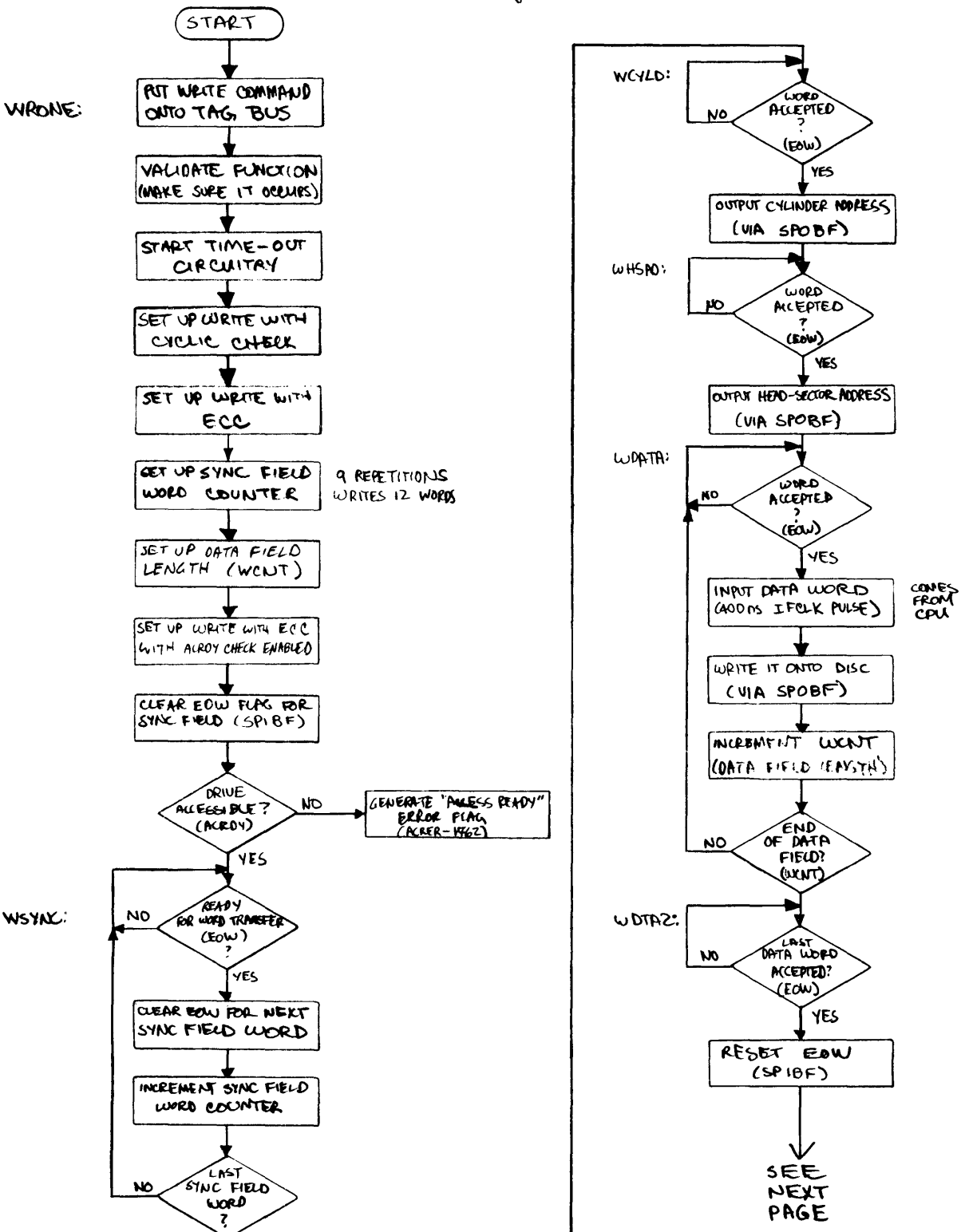
INITIALIZE command writes a sector without first verifying the address field and error bytes of the previous sector (used to flag tracks as defective, spare, and/or protected); fails for hardware protected tracks or if format switch is off.

```
1228                          INITIALIZE COMMAND
1229                  /
1230                  /
1231                  /
1232                  /
1233                  /  INITIALIZE WRITES A SECTOR WITHOUT FIRST VERIFYING THE
1234                  /  ADDRESS FIELD AND ERROR BYTES OF THE PREVIOUS SECTOR.  IT IS
1235                  /  ALSO USED TO FLAG TRACKS SPARE, PROTECTED, AND-OR DEFECTIVE
1236                  /  (COMMAND WORD BITS 15-13 RESPECTIVELY)   THE OPERATION WILL
1237                  /  FAIL (STATUS-2 ERROR) IF THE DISC SURFACE IS HARDWARE
1238                  /  PROTECTED OR IF THE FORMAT SWITCH IS OFF
1239                  /    WHEN A TRACK IS BEING INITIALIZED DEFECTIVE, THE
1240                  /  (LOGICAL) HEAD ADDRESS IN HSAD IS NOT NECESSARILY THE SAME AS
1241                  /  THE PHYSICAL HEAD BEING ADDRESSED   SINCE THE HEAD ADDRESS IN
1242                  /  HSAD IS THE BASIS FOR SKEWING SECTORS WHEN ADDRESSING THE DRIVE,
1243                  /  WE MUST PUT THE PHYSICAL HEAD IN HSAD WHEN ADDRESSING THE DRIVE
1244                  /  AND THE LOGICAL HEAD IN WHEN WRITING HSAD ON TO THE SECTOR
1245                  /  THIS ASSURES PROPER SKEWING, I.E., ON ANY TRACK, SECTORS ARE
1246                  /  SKEWED BY THE LOGICAL HEAD (THE ONE PASSED DURING THE LAST
1247                  /  SEEK OR ADDRESS RECORD COMMAND)
1248                  /
1249 0642 66001317 INIT      CA : UNIT                    / TRY TO CONNECT DRIVE
1250 0643 66001714           CA : STRT2                   / SET PROPER DISC ADDRESS.
1251 0644 66000775           CA : CKWRT                   / MAKE SURE WRITING IS ALLOWED
1252 0645 34010274         BUF2 =       CMP  COMWD       / SET UP S, P, AND D BITS
1253 0646 27412340        STATR = 340   AND  BUF2 ,U     /   IN STATR AND HSAD
1254 0647 36704470         HSAD = HSAD  OR   STATR,U
1255 0650 37706210        PLHED =       PASS HSAD ,SW    / PUT LOGICAL HEAD IN LOWER BYTE
1256 0651 37706070        PLHED =       PASS HSAD ,U     /   AND UPPER BYTE (ASSUME SAME
1257                                                     /   LHEAD AND PHEAD TO START)
1258 0652 27402040        DUMMY = 40    AND  BUF2 ,U     / ISOLATE THE D BIT
1259 0653 44440000           CC = TNZRO           ,RS    / IS IT ON?
1260 0654 64000662           BR : INIT1                  / NO, LHEAD = PHEAD, CONTINUE.
1261 0655 66000375           CA : RQSC3                  / YES, GO FETCH PHYSICAL HEAD
1262 0656 37706064        PLHED =       PASS BUF1 ,U     / ! PHYSICAL HEAD ! LOGICAL HEAD !
1263 0657 37704074         HSAD =       PASS PLHED,U     / ADDR LOGICAL SCTR WITH PHYS HEAD
1264 0660 66000320           CA : GDTYP                  / GET DRIVE TYPE FOR OUTSC
1265 0661 66001725           CA : OUTSC
1266 0662 07622624 INIT1     DO : IFNBF  ←    IFOUT,L    / SET INTERFACE FOR DATA OUTPUT
1267 0663 66000423           CA : DSTR1                  / GO SET UP WRITE DATA PATH.
1268 0664 44700000 INIT2     CC = FALSE                  / LOOP EXIT FAILS FROM HERE
1269 0665 37706214 INIT3  PLHED =       PASS PLHED,SW    / ! LOGICAL HEAD ! PHYSICAL HEAD !
1270 0666 37704074         HSAD =       PASS PLHED,U     / HSAD _ LHEAD FOR WRITING OR EXIT
1271 0667 64000504           BR : ROFS3                  / FAILS IF WE'RE STILL LOOPING.
1272 0670 66000705           CA : WRONE                  / INITIALIZE THE SECTOR.
1273 0671 37706214        PLHED =       PASS PLHED,SW    / ! PHYSICAL HEAD ! LOGICAL HEAD !
1274 0672 37704074         HSAD =       PASS PLHED,U
1275 0673 66001461           CA : INCHS                  / SET UP NEXT SECTOR ADDRESS.
1276 0674 42540000           CC = NWTRF           ,RS    / DID WE SWITCH TRACKS?
1277 0675 64000700           BR : INIT4                  / NO, CONTINUE
1278 0676 37706210        PLHED =       PASS HSAD ,SW    / YES, ASSUME NORMAL INIT (NO
1279 0677 37706070        PLHED =       PASS HSAD ,U     /   D BIT), UPDATE PLHED
1280 0700 42600000 INIT4     CC = EOD                    / ALL THE DATA TRANSFERRED?
1281 0701 64000665           BR : INIT3                  / YES, GO END THE OPERATION.
1282 0702 66001503           CA : SECTR                  / NO, GO SET FOR NEXT SECTOR.
1283 0703 66001024           CA : WSTA2                  / PLATTER PROTECT SWITCH SET?
1284 0704 64000664           BR : INIT2                  / NO, GO INITIALIZE ANOTHER SECTOR
```

```
1285                          WRITE ONE SECTOR SUBROUTINE
1286                 /
1287                 /
1288                 /
1289                 /
1290                 /  SUBROUTINE WRONE WRITES ONE SECTOR ON THE DISC   IT ASSUMES THAT
1291                 /  THE SECTOR HAS BEEN PREVIOUSLY ADDRESSED AND THAT THE DATA PATH
1292                 /  TO THE INTERFACE IS ALREADY SET   IT ALSO ASSUMES THAT ALL INTER-
1293                 /  LOCKS OF A PARTICULAR WRITE OPERATION HAVE BEEN SATISFIED.  WRONE
1294                 /  IS NOT USED FOR THE "WRITE FULL SECTOR" COMMAND
1295                 /    TIMING:  DO NOT LESSEN THE NUMBER OF INSTRUCTIONS BETWEEN
1296                 /  WRONE AND WRONE+3 OR BETWEEN WRONE+3 AND WSYNC-4.  THESE
1297                 /  INSTRUCTIONS ARE SPACED DELIBERATELY TO ALLOW TGBUS AND
1298                 /  COMMAND BUS PROP TIMES, BUT WITHOUT THE ARTIFICIAL DELAY
1299                 /  INTRODUCED BY A CALL TO STRB1   THIS CUTS DOWN ON WASTED
1300                 /  TIME BETWEEN SECTORS OF A MULTIPLE-SECTOR TRANSFER.
1301                 /
1302 0705 07624016 WRONE    DO : TGBUS  ←   WRTCM,L    / PUT OUT WRITE COMMAND.
1303 0706 07606000          DO : IFVLD  ←   SETCL,U    / MAKE SURE TRANSFER OCCURS
1304 0707 07600500          DO : TIMER  ←   START,U    / TURN ON TIME-OUT CIRCUIT
1305 0710 07604475          DO : INTCW  ←   WCC1 ,U    / WRITE AND CYCLIC CHECK.
1306 0711 07610026          DO : ECICW  ←   WECC ,U    / WRITE WITH ECC
1307 0712 27636366        BUF3 = 366    PASS       ,L    / SYNC FIELD WORD COUNTER
1308                                                      /   (9 REPS, WRITES 12 WORDS)
1309 0713 27616177        BUF3 = 177    PASS       ,U    / UPPER HALF OF SYNC WORD
1310 0714 27722200        WCNT = WCT    PASS       ,L    / DATA FIELD LENGTH (1'S COMP)
1311 0715 07604471          DO : INTCW  ←   WCC2 ,U    / WCC1 WITH ACRDY CHECK ENABLED
1312 0716 10007304          DI : DUMMY  ←   SPIBF      / CLEARS EOW FLAG FOR SYNC FIELD
1313                                                      /   (HOWE INITIALIZES SERDES TO 0)
1314 0717 42440000          CC = ACRDY            ,RS  / IS DRIVE O.K.?
1315 0720 64001762          BR : ACRER                 / NO, ESCAPE HERE.
1316 0721 42240000 WSYNC    CC = EOW              ,RS  / YES, READY TO TRANSFER WORD?
1317 0722 64000721          BR : WSYNC                 / NO, LOOP UNTIL WE ARE.
1318 0723 10007304          DI : DUMMY  ←   SPIBF      / YES, CLEAR EOW FOR NEXT
1319                                                      /   SYNC FIELD WORD
1320 0724 22237401        BUF3 = 1      PLUS BUF3 ,L
1321 0725 44140000          CC = LOVER            ,RS
1322 0726 64000721          BR : WSYNC                 / IF NOT DONE, DO ANOTHER.
1323 0727 42240000 WSYN1    CC = EOW              ,RS  / WAIT FOR LAST ONE
1324 0730 64000727          BR : WSYN1                 /   BEFORE PUTTING OUT SYNC WORD
1325 0731 10031556          DI : BUF3   ←   ESYNC,L    / PUT OUT ECC MARK IN SYNC WORD
1326 0732 16407655          DO : SPOBF  ←   BUF3       / PUT OUT SYNC WORD
1327 0733 42240000 WCYLD    CC = EOW              ,RS  / WAIT FOR IT TO BE ACCEPTED
1328 0734 64000733          BR : WCYLD
1329 0735 15207251          DO : SPOBF  ←   CYLAD,C    / THEN OUTPUT CYLINDER ADDRESS.
1330 0736 42240000 WHSAD    CC = EOW              ,RS  / WAIT FOR BUFFER TO ACCEPT IT
1331 0737 64000736          BR : WHSAD
1332 0740 14007251          DO : SPOBF  ←   HSAD ,C    / OUTPUT HEAD-SECTOR ADDRESS.
1333 0741 42240000 WDATA    CC = EOW              ,RS
1334 0742 64000741          BR : WDATA
1335 0743 10001756          DI : BUF3   ←   IDTBF      / WRITE DATA FIELD IN THIS LOOP
1336 0744 10001756          DI : BUF3   ←   IDTBF      /   (400 NSEC IFCLK PULSE)
1337 0745 16407655          DO : SPOBF  ←   BUF3
1338 0746 33762064        WCNT =        INC  WCNT ,L    / COUNT THE DATA WORD
1339 0747 44140000          CC = LOVER            ,RS  / END OF DATA FIELD?
1340 0750 64000741          BR : WDATA                 / NO, GO BACK FOR NEXT WORD
1341 0751 42240000 WDTA2    CC = EOW              ,RS  / WAIT FOR LAST DATA WORD
1342 0752 64000751          BR : WDTA2                 /   TO BE ACCEPTED
1343 0753 10007304          DI : DUMMY  ←   SPIBF      / RESET EOW
```

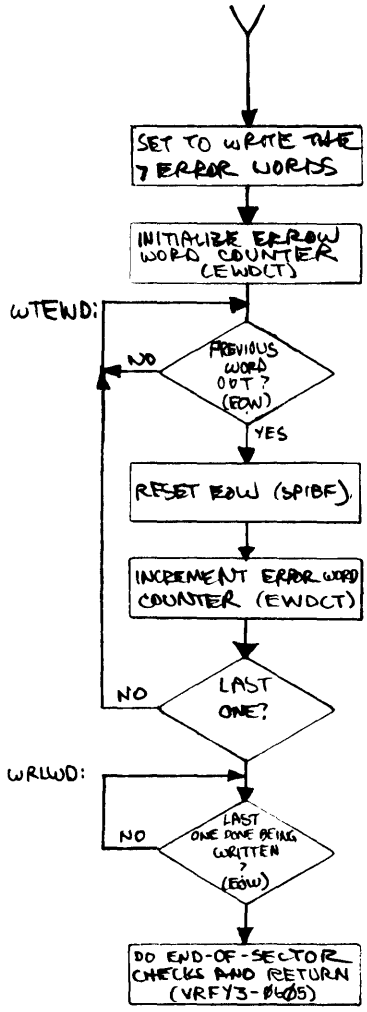
WRITE ONE SECTOR SUBROUTINE

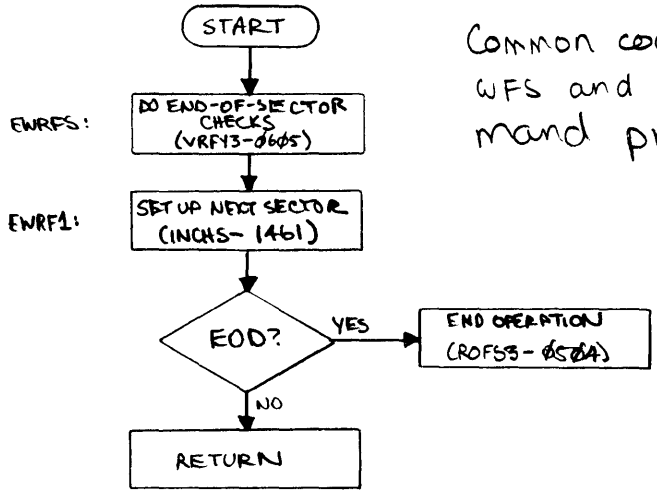
(see next page also)



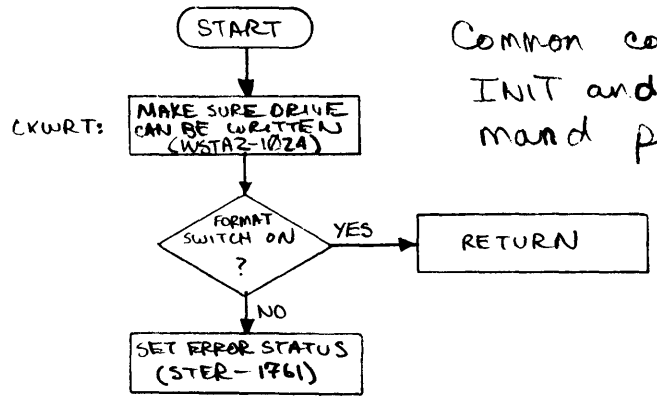
WRONE not used by WRITE FULL SECTOR; assumes sector is addressed and data path set up.

WRITE ONE SECTOR SUBROUTINE (CONT.)
EWRFS, CKWRT





Common code after WFS and RFS command processors.

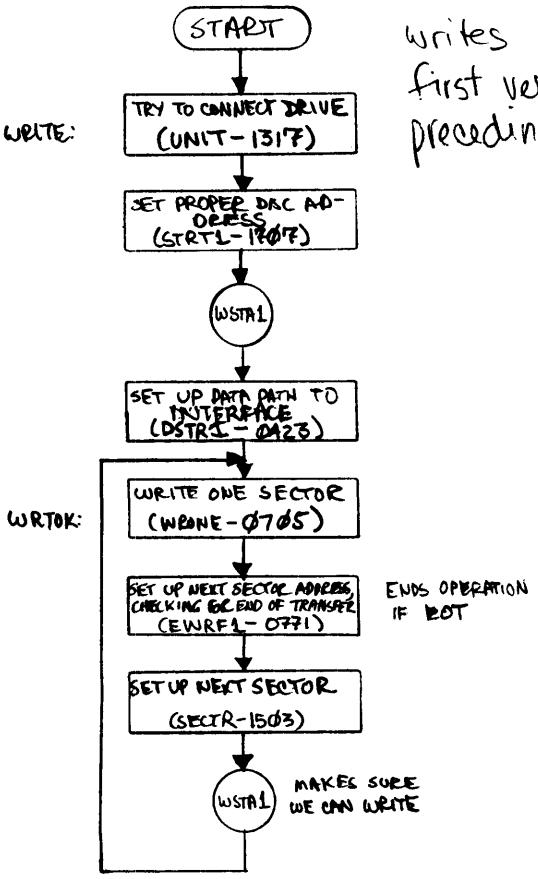


Common code after INIT and WFS command processors.

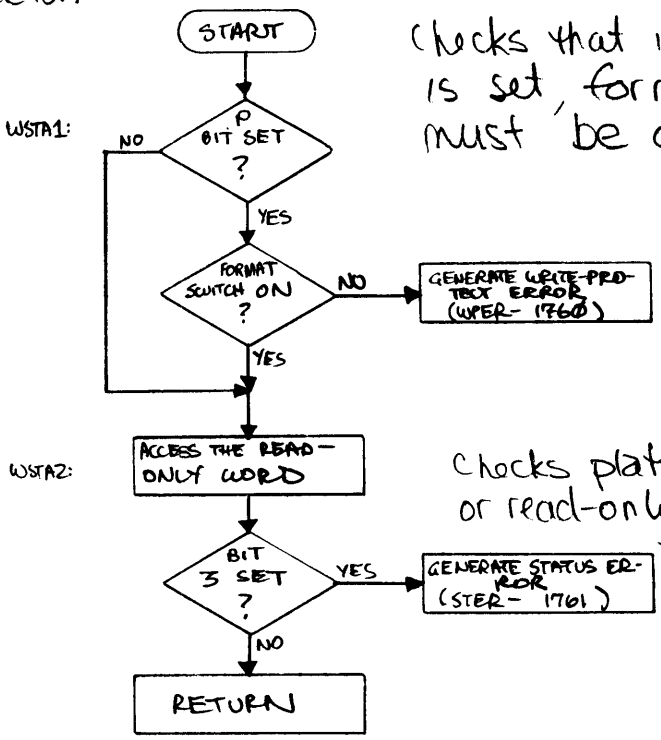
```
1344                          WRITE ONE SECTOR SUBROUTINE, EWRFS, CKWRT
1345                 /
1346                 /
1347                 /
1348                 /
1349 0754 07610000          DO : ECICW  ←   ESC  ,U     / START COUNTING 2 EOWS TO FREEZE.
1350 0755 07604461          DO : INTCW  ←   WERWD,U     / SET TO WRITE ERROR WORDS
1351 0756 27722371       EWDCT = ERWCT PASS       ,L     / INITIALIZE ERROR WORD COUNTER.
1352 0757 42240000 WTEWD    CC = EOW              ,RS    / WAIT FOR PREVIOUS WORD TO GO OUT
1353 0760 64000757          BR : WTEWD
1354 0761 10007304          DI : DUMMY  ←   SPIBF      / RESET EOW
1355 0762 33762064       EWDCT =       INC  EWDCT,L     / COUNT THE ERROR WORD
1356 0763 44140000          CC = LOVER            ,RS    / LAST ONE?
1357 0764 64000757          BR : WTEWD                   / NO, GO BACK FOR NEXT ONE
1358 0765 42240000 WRLWD    CC = EOW              ,RS    / YES, WAIT FOR IT TO BE WRITTEN
1359 0766 64000765          BR : WRLWD
1360 0767 64000605          BR : VRFY3                   / DO END-OF-SECTOR CHECKS, RETURN.
1361                 /
1362                 /
1363                 /  SUBROUTINE EWRFS IS SOME COMMON CODE AT THE END OF THE WFS
1364                 /  AND RFS COMMAND PROCESSORS   THE ENTRY AT EWRF1 IS USED BY THE
1365                 /  WRITE COMMAND AND READ COMMAND PROCESSORS.
1366                 /
1367 0770 66000605 EWRFS    CA : VRFY3                   / GO DO END-OF-SECTOR CHECKS.
1368 0771 66001461 EWRF1    CA : INCHS                   / ALL O.K., SET UP NEXT SECTOR.
1369 0772 42600000          CC = EOD                     / END OF DATA?
1370 0773 64000504          BR : ROFS3                   / YES, GO END THE OPERATION.
1371 0774 72000000          RT : 0                       / NO, RETURN AND CONTINUE.
1372                 /
1373                 /
1374                 /  SUBROUTINE CKWRT IS SOME COMMON CODE FROM THE INIT AND WFS
1375                 /  COMMAND PROCESSORS
1376                 /
1377 0775 66001024 CKWRT    CA : WSTA2                   / MAKE SURE THE DRIVE CAN WRITE.
1378 0776 27423404       DUMMY = 4     AND  BUF3 ,L     / "FORMAT" SWITCH MUST BE ON TOO
1379 0777 44440000          CC = TNZRO            ,RS
1380 1000 64001761          BR : STER                    / IT'S OFF, CAN'T DO IT
1381 1001 72000000          RT : 0
```

```
1382                        WRITE COMMAND, SUBROUTINES WSTA1, WSTA2
1383                /
1384                /
1385                /
1386                /
1387                /  WRITES A SECTOR OF INFORMATION ONTO THE DISC
1388                /  FIRST VERIFIES THE ADDRESS FIELD OF THE PRECEDING
1389                /  SECTOR.  OPERATION FAILS IF SURFACE IS PROTECTED
1390                /
1391 1002 66001317 WRITE    CA : UNIT                  / TRY TO CONNECT DRIVE.
1392 1003 66001707          CA : STRT1                 / SET PROPER DISC ADDRESS.
1393 1004 66001014          CA : WSTA1                 / SEE IF WE CAN WRITE.
1394 1005 07622624          DO : IFNBF  ←   IFOUT,L    / ALL O.K., SET UP I'FC DATA PATH.
1395 1006 66000423          CA : DSTR1
1396 1007 66000705 WRTOK    CA : WRONE                 / GO WRITE ONE SECTOR.
1397 1010 66000771          CA : EWRF1                 / SET UP NEXT SECTOR ADDRESS,
1398                                                   /   CHECK FOR END OF TRANSFER.
1399 1011 66001503          CA : SECTR                 / NOT END, SET UP NEXT SECTOR.
1400 1012 66001014          CA : WSTA1                 / RECHECK P, D BITS, READ-ONLY
1401 1013 64001007          BR : WRTOK                 / ALL O.K., GO WRITE NEXT SECTOR.
1402                /
1403                /
1404                /    SUBROUTINE WSTA1 CHECKS THE P-BIT   IF IT IS SET, THE FORMAT
1405                /  SWITCH MUST ALSO BE SET TO ALLOW WRITING.  FOLLOWING WSTA1, WE
1406                /  FALL INTO WSTA2 TO CHECK THE PLATTER PROTECT (7905) OR READ-
1407                /  ONLY (7920) SWITCH.  NOTE:  DUPLICATING THE TWO RAM ACCESS
1408                /  INSTRUCTIONS (ONCE IN WSTA1, AGAIN IN WSTA2) COSTS NO EXTRA
1409                /  CODE AND SAVES 400 NSEC IN EXECUTION TIME OVER ALTERNATE METHODS
1410                /
1411 1014 27402500 WSTA1 DUMMY = 100   AND  STATR,U
1412 1015 44440000          CC = TNZRO           ,RS   / IS THE P-BIT SET?
1413 1016 64001024          BR : WSTA2                 / NO, GO CHECK READ ONLY SWITCH.
1414 1017 07620013          DO : RAMAD  ←   RDONL,L    / YES, CHECK IF
1415 1020 10020456          DI : BUF3   ←   RAM  ,L    /   FORMAT SWITCH IS ON.
1416 1021 27423404       DUMMY = 4      AND  BUF3 ,L
1417 1022 44440000          CC = TNZRO           ,RS
1418 1023 64001760          BR : WPER                  / NO, CAN'T WRITE ON P-TRACK.
1419                                                   / FALL INTO WSTA2 IF HERE.
1420                /
1421                /
1422                /  SUBROUTINE WSTA2 CHECKS THE PLATTER PROTECT WORD IN RAM TO SEE
1423                /  IF THE PLATTER PROTECT (READ-ONLY) SWITCH IS SET FOR THE
1424                /  CURRENT SURFACE.
1425                /
1426 1024 07620013 WSTA2    DO : RAMAD  ←   RDONL,L    / ACCESS THE
1427 1025 10020456          DI : BUF3   ←   RAM  ,L    /   READ-ONLY WORD
1428 1026 27423410       DUMMY = 10     AND  BUF3 ,L
1429 1027 44400000          CC = TNZRO                 / BIT 3 ≠ 0 MEANS
1430 1030 64001761          BR : STER                  /   READ-ONLY SWITCH SET
1431 1031 72000000          RT : 0                     / ALL O.K., RETURN.
```

WRITE COMMAND, SUBROUTINES WSTA1, WSTA2



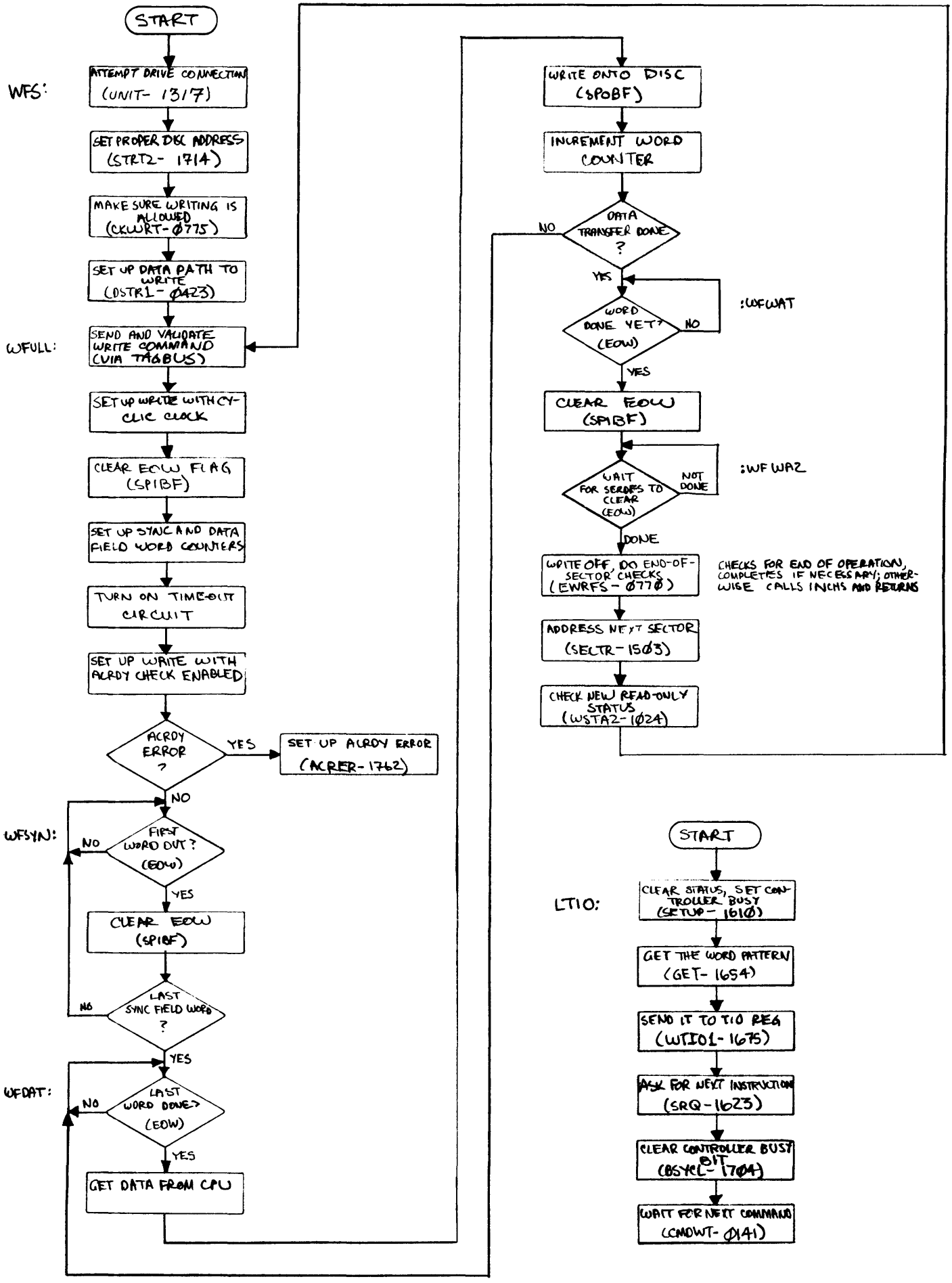
writes a sector onto the disc, first verifying address field of preceding sector.



Checks that if P-bit is set, format switch must be on.

Checks platter protect or read-only switch.

WRITE FULL SECTOR, LOAD TIO



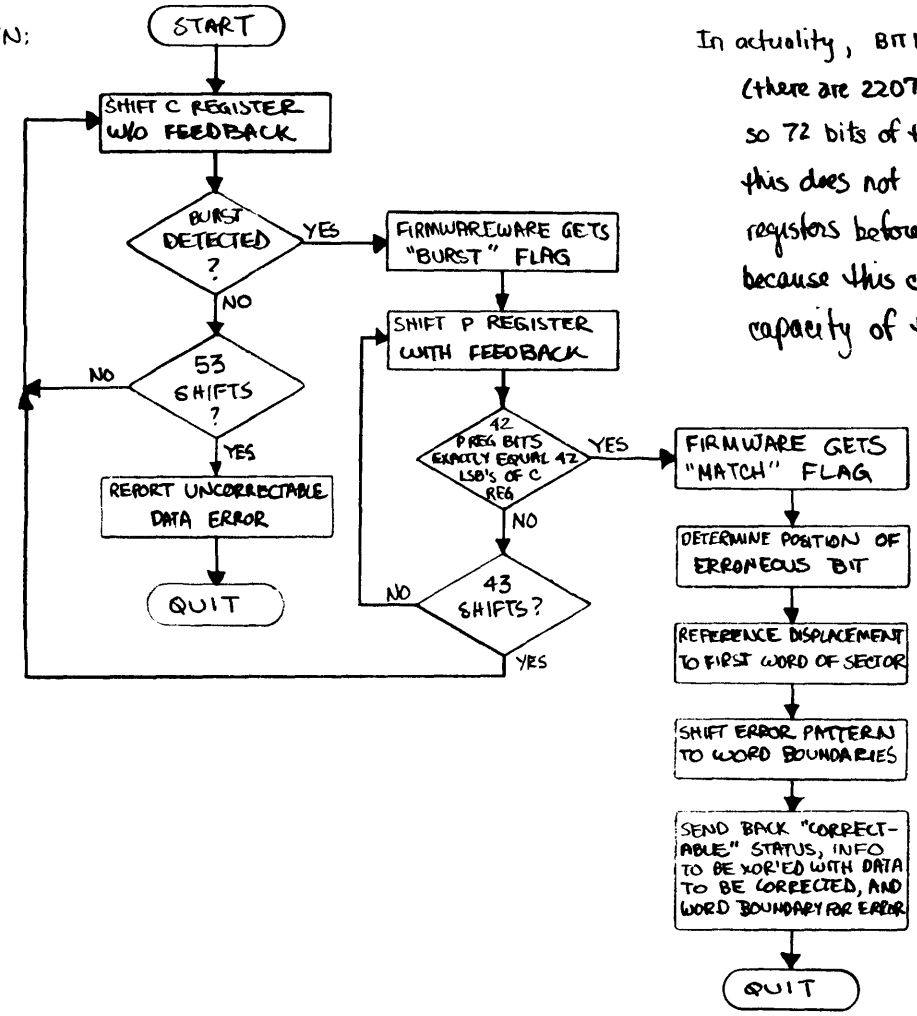
```
1432                              WRITE FULL SECTOR, LOAD TIO COMMANDS
1433                    /
1434                    /
1435                    /
1436                    /  THE WFS (WRITE FULL SECTOR) COMMAND WRITES THE ENTIRE SECTOR
1437                    /  (INCLUDING PRE- AND POSTAMBLE, BUT NOT SYNC FIELD) FROM DATA
1438                    /  SUPPLIED BY THE CPU   FORMAT SWITCH MUST BE SET TO OVERRIDE.
1439                    /    TIMING:  SAME CONSIDERATIONS HERE AS FOR WRONE.
1440                    /
1441 1032 66001317 WFS       CA : UNIT                    / TRY TO CONNECT DRIVE.
1442 1033 66001714           CA : STRT2                   / SET PROPER DISC ADDRESS.
1443 1034 66000775           CA : CKWRT                   / MAKE SURE WRITING IS ALLOWED
1444 1035 07622624           DO : IFNBF  ←   IFOUT,L      / ALL O.K., SET UP DATA PATH.
1445 1036 66000423           CA : DSTR1
1446 1037 07624016 WFULL     DO : TGBUS  ←   WRTCM,L      / SEND WRITE COMMAND TO DRIVE.
1447 1040 07606000           DO : IFVLD  ←   SETCL,U      / MAKE SURE TRANSFER OCCURS.
1448 1041 07604475           DO : INTCW  ←   WCC1 ,U      / WRITE (WITH "CYCLIC CHECK")
1449 1042 10007304           DI : DUMMY  ←   SPIBF        / CLEARS EOW FLAG FOR SYNC FIELD
1450                                                      /   (HDWE INITIALIZES SERDES TO 0)
1451 1043 27636366         BUF3 = 366    PASS       ,L     / SYNC FIELD WORD COUNTER.
1452 1044 27722166         WCNT = FULSC  PASS       ,L     / DATA FIELD WORD COUNTER.
1453 1045 07600500           DO : TIMER  ←   START,U      / TURN ON TIME-OUT CIRCUIT
1454 1046 07604471           DO : INTCW  ←   WCC2 ,U      / WCC1 WITH ACRDY CHECK ENABLED
1455 1047 42440000           CC = ACRDY           ,RS     / WAIT FOR FIRST WORD OUT
1456 1050 64001762           BR : ACRER
1457 1051 42240000 WFSYN     CC = EOW             ,RS
1458 1052 64001051           BR : WFSYN
1459 1053 10007304           DI : DUMMY  ←   SPIBF        / CLEAR EOW
1460 1054 22237401         BUF3 = 1      PLUS BUF3 ,L     / COUNT THE SYNC FIELD WORD
1461 1055 44140000           CC = LOVER           ,RS
1462 1056 64001051           BR : WFSYN                    /   AND GO BACK FOR MORE,
1463 1057 42240000 WFDAT     CC = EOW             ,RS     /   OR ELSE START THE DATA FIELD
1464 1060 64001057           BR : WFDAT
1465 1061 10001756           DI : BUF3   ←   IDTBF
1466 1062 10001756           DI : BUF3   ←   IDTBF        / (400 NSEC IFCLK PULSE)
1467 1063 16407655           DO : SPDBF  ←   BUF3         / SEND OUT THE DATA WORD
1468 1064 33762064         WCNT =        INC  WCNT ,L
1469 1065 44140000           CC = LOVER           ,RS     / DATA TRANSFER DONE?
1470 1066 64001057           BR : WFDAT                    / NOT YET
1471 1067 42240000 WFWAT     CC = EOW             ,RS     / YES, WAIT FOR LAST WORD TO GO OUT
1472 1070 64001067           BR : WFWAT
1473 1071 10007304           DI : DUMMY  ←   SPIBF        / CLEAR EOW
1474 1072 42240000 WFWA2     CC = EOW             ,RS     /   THEN WAIT FOR SERDES TO CLEAR.
1475 1073 64001072           BR : WFWA2
1476 1074 66000770           CA : EWRFS                    / WRITE OFF, DO END SECTOR CHECKS.
1477 1075 66001503           CA : SECTR                    / MORE TO DO, ADDRESS NEXT SECTOR.
1478 1076 66001024           CA : WSTA2                    / CHECK NEW READ-ONLY STATUS.
1479 1077 64001037           BR : WFULL                    / O.K., GO WRITE THE SECTOR.
1480                    /
1481                    /
1482                    /  LTIO IS A DIAGNOSTIC ROUTINE THAT LOADS THE TIO REGISTER WITH
1483                    /  THE CONTENTS OF A WORD PASSED BY THE 3000 CPU.
1484                    /
1485 1100 66001610 LTIO      CA : SETUP                   / CLEAR STATUS, SET CONTROLLER BUSY
1486 1101 66001654           CA : GET                     / GET THE PATTERN WORD
1487 1102 66001675           CA : WTIO1                   / SEND IT TO THE TIO REGISTER
1488 1103 66001623           CA : SRQ                     / ASK FOR THE NEXT INSTRUCTION.
1489 1104 66001704           CA : BSYCL                   / CLEAR THE CONTROLLER BUSY BIT
1490 1105 64000141           BR : CMDWT                   / GO WAIT FOR NEXT COMMAND
```

```
1491                        REQUEST SYNDROME COMMAND
1492                /
1493                /    THIS SECTION OF CODING IMPLEMENTS THE REQUEST SYNDROME (RQSYN)
1494                /  COMMAND   THE RQSYN COMMAND RETURNS 7 WORDS OF INFORMATION:
1495                /
1496                /    1)  AN UPDATED CONTROLLER STATUS WORD (7400B IF THE ERROR WAS
1497                /  CORRECTED, 4000B IF IT WAS UNCORRECTABLE.  IN THE LATTER CASE,
1498                /  WORDS 4-7 CONTAIN GARBAGE AND SHOULD BE IGNORED)
1499                /    2-3)  THE DISC ADDRESS (CYLAD AND HSAD-MINUS-SPD-BITS) WHERE
1500                /  THE DATA ERROR OCCURRED (USEFUL IN MULTIPLE-SECTOR TRANSFERS)
1501                /    4)  THE DISPLACEMENT WITHIN THE SECTOR WHERE THE ERROR PATTERN
1502                /  (WORDS 5-7) SHOULD BE APPLIED
1503                /    5-7)  THE ERROR PATTERN, USED TO CORRECT DATA IN THE USER'S
1504                /  BUFFER.
1505                /
1506                /    THE DISPLACEMENT MAY VARY FROM -5 (TWO'S COMPLEMENT) TO +135.
1507                /  IT REPRESENTS THE OFFSET THAT SHOULD BE ALGEBRAICALLY ADDED TO
1508                /  THE BASE (FIRST WORD) ADDRESS OF THE DATA BUFFER CORRESPONDING
1509                /  TO THE SECTOR IN ERROR (USE WORDS 2 AND 3)   THIS GETS THE
1510                /  ADDRESS OF THE FIRST WORD TO WHICH THE ERROR PATTERN SHOULD BE
1511                /  APPLIED   NOTE THAT IF THE DISPLACEMENT < 0 OR > 125, SOME OR
1512                /  ALL OF THE SECTOR ERRORS ARE OUTSIDE THE DATA AREA.  TO AVOID
1513                /  MIS-CORRECTION IN THIS CASE, FOLLOW THE ALGORITHM SHOWN IN THE
1514                /  13037 PRODUCT SPECIFICATIONS (HOPEFULLY ALSO THE OPERATING MANUAL)
1515                /
1516                /    THE ERROR PATTERN WORDS ARE MASKS TO BE EXCLUSIVE-OR'ED WITH
1517                /  DATA ALREADY IN THE USER'S BUFFER   BITS IN ERROR WILL BE 1 IN
1518                /  THE MASK, CAUSING THE CORRESPONDING BITS IN THE DATA BUFFER TO
1519                /  BE COMPLEMENTED   THE ERROR PATTERN IS ALWAYS ADJUSTED TO A WORD
1520                /  BOUNDARY, SO NO BIT SHIFTING WITHIN WORDS IS REQUIRED
1521                /
1522                /    THE RQSYN COMMAND SHOULD ONLY BE INVOKED IF BITS 12-8 OF THE
1523                /  CONTROLLER STATUS (STATUS-1) WORD FROM THE PREVIOUS COMMAND
1524                /  ARE 0 111 1 (STATUS = 74UU (OCTAL))   THIS INDICATES:
1525                /
1526                /    1)  THE ECC FEATURE IS INSTALLED IN THE CONTROLLER,
1527                /    2)  THE SECTOR IN ERROR WAS WRITTEN USING A CONTROLLER IN
1528                /  WHICH ECC WAS INSTALLED (GUARANTEEING A VALID ECC FIELD), AND
1529                /    3)  THE ERROR IS POSSIBLY CORRECTABLE.
1530                /
1531                /  IF ANY OF THE ABOVE CONDITIONS ARE FALSE, AND A DATA ERROR
1532                /  OCCURS, CONTROLLER STATUS WILL BE 0 100 0 (40UU (OCTAL))   A RQSYN
1533                /  COMMAND ISSUED HERE WILL RETURN STATUS = 4000B AND GARBAGE IN
1534                /  WORDS 4-7   (TO OBTAIN THE DISC ADDRESS OF THE SECTOR IN ERROR
1535                /  WHEN STATUS = 40XXB, USE THE REQUEST ADDRESS (REQAD) COMMAND
1536                /    IF CONDITION 1 OR 2 IS FALSE (NO ECC), A 16-BIT CRC (ALWAYS
1537                /  PRESENT) IS USED   IT CANNOT CORRECT ERRORS, BUT WILL DETECT:
1538                /
1539                /    1)  ALL SINGLE-16-BIT-OR-LESS BURST ERRORS.
1540                /    2)  99 997% OF ALL SINGLE-17-BIT BURST ERRORS.
1541                /    3)  99 9985% OF ALL BURST ERRORS > 17 BITS LONG.
1542                /
1543                /    IF ECC IS INSTALLED AND IS VALID FOR THE SECTOR IN ERROR, THE
1544                /  HARDWARE AND THIS CODING WILL:
1545                /
1546                /    1)  CORRECT ALL SINGLE-BURST ERRORS <= 32 BITS LONG.
1547                /    2)  DETECT ALL SINGLE-BURST ERRORS > 32 BITS BUT <= 48 BITS
1548                /  LONG WITHOUT MIS-CORRECTING THEM.
1549                /    3)  DETECT 99 999% OF ALL SINGLE-BURST ERRORS > 48 BITS LONG.
```

REQUEST SYNDROME
(3 PAGES OF μCODE)

Note: below is a condensed flowchart of this command, indicating the major chain of events for this complicated routine.

RQSYN:



In actuality, BIT DISP=(1591x#CSHIFTS +689x#PSHIFTS)MOD 2279 (there are 2207 bits in a sector if sync field is excluded, so 72 bits of the zero sync field is shifted in— note this does not upset the initial cleared state of the ECC registers before the actual data is shifted through); because this calculation could overload the 16 bit capacity of the μprocessor, the following method of determining bit displacement is employed:

BIT DISP = [(CACC:=CACC+1591)MOD 2279 + (PACC:=PACC+689)MOD 2279]

where:

CACC, PACC are μprocessor registers used to hold intermediate C and P shift calculations

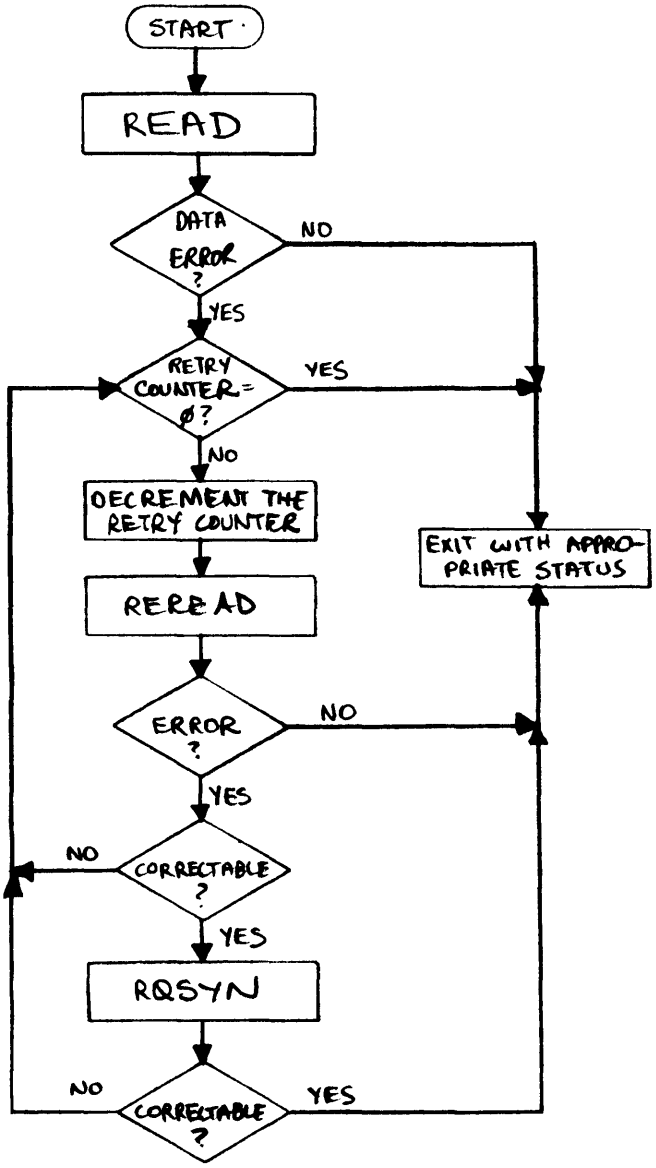
RETURNED WORDS:

UPDATED CONTROLLER STATUS WORD	ERROR ADDRESSES		DISPLACEMENT WITHIN SECTOR OF ERROR				
7400B	CYLAD	HSAD-SPD	DISPLACEMENT	ERROR PATTERN WORD 1	ERROR PATTERN WORD 2	ERROR PATTERN WORD 3	(CORRECTABLE)
4000B	CYLAD	HSAD-SPD					(UNCORRECTABLE)
1	2	3	4	5	6	7	NO. OF RETURNED WORD

```
1550                          REQUEST SYNDROME COMMAND
1551                  /
1552                  /
1553                  /
1554                  /
1555 1106 66001611 RQSYN     CA : BSYST                      / SET CONTROLLER BUSY
1556 1107 27700000          CACC = 0      PASS       ,U     / START WITH C-ACCUMULATOR SET TO 0.
1557 1110 27720000          CACC = 0      PASS       ,L
1558 1111 27412740         STATR = 340    AND   STATR,U     / PRESERVE S, P, AND D BITS
1559 1112 26612417         STATR = 17     OR    STATR,U     / ASSUME IT'S CORRECTABLE AT FIRST
1560 1113 27610010          CAPM = CAPMU  PASS       ,U     / SET UP CODE LENGTH MODULUS (2279)
1561 1114 27630347          CAPM = CAPML  PASS       ,L     /   FOR BOTH BYTES.
1562 1115 07610211            DO : ECICW  ←    CLKHH,U     / CLOCK HIGH ONCE TO AVOID
1563                                                        /   RACE CONDITION IN ECICW
1564 1116 07610230            DO : ECICW  ←    CLKHI,U     / CLOCK MUST BE HIGH BEFORE INHIBIT
1565 1117 27722312          CLIM = 312    PASS       ,L     / C-LOOP COUNTER = -53 (DEC) -1
1566                                                        /   (BECAUSE WE TEST LIMIT BEFORE
1567                                                        /   WE TEST FOR BURST)
1568 1120 43240000 MOREC      CC = BURST                ,RS  / HAS BURST OCCURRED ALREADY?  WITHOUT
1569 1121 64001152            BR : PLOOP                    /   ANY C-SHIFTS?  GO MATCH
1570 1122 07610312 CLOOP      DO : ECICW  ←    FRPSH,U     / FREEZE P-REGISTER, SET CLOCK HIGH
1571                                                        /   (OFF), REMOVE REGISTER INHIBIT
1572 1123 27616006         CCONS = CCONU PASS       ,U     / SET UP CHINESE REMAINDER THEOREM
1573 1124 27636067         CCONS = CCONL PASS       ,L     /   C-CONSTANT (1591) IN BOTH BYTES.
1574 1125 07610300            DO : ECICW  ←    CCLKL,U     / FREEZE P, CLOCK LOW-HIGH TO
1575 1126 07610310            DO : ECICW  ←    CCLKH,U     /   SHIFT C ONCE WITH FEEDBACK.
1576 1127 32301660          CACC = CACC   PLUS CCONS       / ADD THE CONSTANT TO C-ACCUMULATOR.
1577 1130 66001200            CA : ACMOD                    / REDUCE CACC MOD CAPM.
1578 1131 33762064          CLIM =        INC   CLIM ,L     / COUNT THE NON-BURST
1579 1132 44140000            CC = LOVER                ,RS  / CHECK LIMIT - DONE?
1580 1133 64001120            BR : MOREC                    / NO, GO SEE IF LAST SHIFT GAVE
1581                                                        /   US A BURST
1582                  /
1583                                                        / DONE, CAN'T GET A CORRECTABLE
1584                                                        /   PATTERN, GONNA HAVE TO QUIT
1585 1134 27412750         STATR = 350    AND   STATR,U     / UNCORRECTABLE DATA ERROR
1586 1135 35302660          BUF1 =        CMP   STATR       / SEND UDTER STATUS AND DRIVE NO
1587 1136 66001304            CA : PUT                      / SENDS C(BUF1) TO INTERFACE.
1588 1137 66001271            CA : RQAD1                    / SEND OUT CYLAD, HSAD
1589 1140 34102260 CDER1    BUF1 =        CMP   ACC         / SEND OUT WORD DISPLACEMENT
1590 1141 66001304            CA : PUT
1591 1142 36503660          BUF1 =        PASS ZREG         / SEND OUT FIRST WORD OF PATTERN
1592 1143 66001304            CA : PUT
1593 1144 36502260          BUF1 =        PASS YREG         / SEND OUT SECOND WORD OF PATTERN.
1594 1145 66001304            CA : PUT
1595 1146 37702274          BUF1 =        PASS XREG         / SEND OUT LAST WORD OF PATTERN
1596 1147 66001304            CA : PUT
1597 1150 66001461            CA : INCHS                    / ADDRESS THE NEXT SECTOR.
1598 1151 64000371            BR : RQSC2                    / NOW TERMINATE.
1599
1600                  /
1601                  /
1602                  /
1603                  /
1604 1152 27706000 PLOOP    PACC = 0      PASS       ,U     / START P-LOOP WITH P-ACCUMULATOR
1605 1153 27726000          PACC = 0      PASS       ,L     /   SET TO 0
1606 1154 07610250            DO : ECICW  ←    PCLKH,U     / FREEZE C-REGISTER, SET CLOCK HIGH
1607                                                        /   (OFF) INITIALLY
1608 1155 27616002         PCONS = PCONU PASS       ,U     / SET UP CHINESE REMAINDER THEOREM
1609 1156 27636261         PCONS = PCONL PASS       ,L     /   P-CONSTANT (689) IN BOTH BYTES
1610 1157 37702204          PLIM =        PASS CLIM ,SW     / PLIM AND CLIM ARE IN SAME WORD
1611 1160 27722325          PLIM = 325    PASS       ,L     / P-LOOP COUNTER = -43 (DEC) BECAUSE
1612                                                        /   WE MUST LEAVE P-REGISTER LIKE WE
1613                                                        /   FOUND IT IF NO MATCH.
1614 1161 64001172            BR : COMP2                    / GO CHECK FOR IMMEDIATE MATCH.
1615 1162 07610240 MOREP      DO : ECICW  ←    PCLKL,U     / FREEZE C, CLOCK LOW-HIGH TO
1616 1163 07610250            DO : ECICW  ←    PCLKH,U     /   SHIFT P ONCE WITH FEEDBACK.
1617 1164 32307674          PACC = PACC   PLUS PCONS       / ADD THE CONSTANT TO P-ACCUMULATOR.
1618 1165 31546274          PACC = PACC   SUB  CAPM        / REDUCE MOD CAPM
1619 1166 44540000            CC = TMSB                 ,RS  / SUBTRACT TOO MUCH?
1620 1167 64001171            BR : COMP1                    / NO, IT'S OK.
1621 1170 32306274          PACC = PACC   PLUS CAPM        / YES, ADD IT BACK.
1622 1171 33762064 COMP1    PLIM =        INC   PLIM ,L     / COUNT THE NON-MATCH.
1623 1172 43240000 COMP2      CC = MATCH                ,RS  / GET MATCH DUE TO LAST SHIFT?
1624 1173 64001205            BR : GTPAT                    / YES, GO GET PATTERN.
1625 1174 44140000            CC = LOVER                ,RS  / NO MATCH, CHECK LIMIT - DONE?
1626 1175 64001162            BR : MOREP                    / NO, GO BACK, TRY TO MATCH AGAIN.
1627 1176 37702204          CLIM =        PASS PLIM ,SW     / YES, RESTORE CLIM.
1628 1177 64001122            BR : CLOOP                    / RESET PACC TO 0, TRY NEW
1629                                                        /   PATTERN.  RESET TO 0 IS DONE
1630                                                        /   ON ENTRY INTO P-LOOP
```

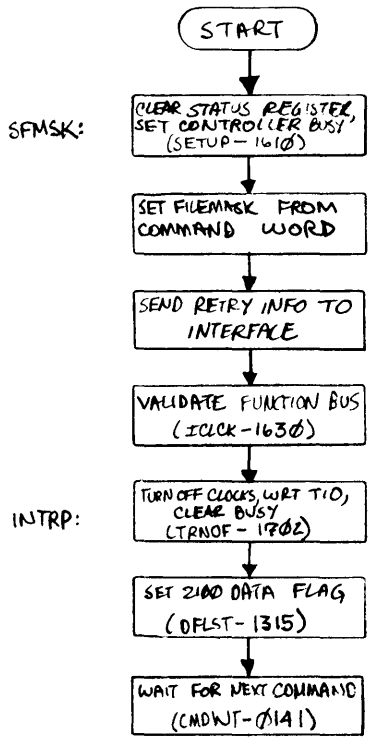
```
1631                    /           REQUEST SYNDROME COMMAND
1632                    /
1633                    /    SUBROUTINE ACMOD GROUPS SOME COMMON CODE FROM THE CLOOP AND GTPAT
1634                    /  ROUTINES, THEREBY SAVING ONE WORD    ****NOTE****:  THIS PLOY ONLY
1635                    /  WORKS BECAUSE THE SYMBOLIC REGISTERS ACC AND CACC ARE THE SAME
1636                    /  PHYSICAL REGISTER.  IT CANNOT BE USED FOR THE SIMILAR CODING IN PLOOP
1637                    /  IF ACC AND CACC ARE EVER A DIFFERENT PHYSICAL REGISTER, IT WILL BE
1638                    /  NECESSARY TO RESTORE THIS CODING TO IN-LINE CODE IN CLOOP AND GTPAT
1639                    /
1640 1200 31540260 ACMOD    ACC = ACC    SUB   CAPM          / REDUCE ACC (CACC) MOD CAPM.
1641 1201 44540000           CC = TMSB                ,RS   / SUBTRACT TOO MUCH?
1642 1202 72000000           RT : 0                         / NO, RETURN.
1643 1203 32300260          ACC = ACC    PLUS CAPM          / YES, ADD IT BACK.
1644 1204 72000000           RT : 0                         / THEN RETURN.
1645
1646                    /
1647                    /
1648                    /
1649                    /
1650 1205 35302660 GTPAT   BUF1 =         CMP   STATR        / DATA ERROR CORRECTABLE, SEND
1651 1206 66001304           CA : PUT                        /   STATUS AND DISC ADDRESS HERE TO
1652 1207 66001271           CA : RQAD1                      /   PRESERVE STATR LATER
1653 1210 37616274        PCONS =         PASS PACC          / TEMPORARILY GET A B-REGISTER.
1654 1211 32301660          ACC = CACC    PLUS PCONS         / ADD THE TWO DISPLACEMENTS
1655 1212 66001200           CA : ACMOD                      / REDUCE ACC MOD CAPM.
1656 1213 27630231         BIAS = 231     PASS       ,L     / SET UP SHORTENED CODE BIAS
1657 1214 27610000         BIAS = 0       PASS       ,U     /   PLUS 48 PRE-AMBLE BITS
1658 1215 31450260         BIAS = ACC     SUB   BIAS        / SUBTRACT BIAS FROM ORIGINAL BIT
1659                                                        /   DISPLACEMENT
1660 1216 44540000           CC = TMSB                ,RS   / REMEMBER IF IT WAS NEGATIVE.
1661 1217 27436017         BUF3 = 17      AND   BIAS ,L     / MASK OUT LOWER ORDER 4 BITS
1662                                                        /   WHICH IS 15-# SHIFTS REQUIRED TO
1663                                                        /   PLACE ERROR PATTERN ON WORD BOUNDARY
1664 1220 21563420        COUNT = 20     SUB   BUF3 ,L     / START WITH 16-# SHIFTS REQUIRED,
1665                                                        /   BECAUSE WE DECREMENT FIRST
1666                                                        /   (AT WLOOP)
1667 1221 36500320          ACC =         PASS BIAS ,SR     / THEN DIVIDE MODIFIED BIT DISPLACEMENT
1668 1222 37700320          ACC =         PASS ACC  ,SR     /   BY 16 (SHIFT RIGHT 4 TIMES) TO
1669 1223 37700320          ACC =         PASS ACC  ,SR     /   GET THE WORD DISPLACEMENT
1670 1224 37700320          ACC =         PASS ACC  ,SR
1671 1225 64001230           BR : COMP3                     / WAS DISPLACEMENT NEGATIVE?
1672 1226 27610360         BIAS = 360     PASS       ,U     / YES, EXTEND THE SIGN BIT
1673 1227 36700060          ACC = BIAS    OR    ACC  ,U     /   BY PUTTING IN 1'S
1674 1230 10013302 COMP3     DI : YREG     ←     WORD1      / LOAD THE 16 MSB'S OF PATTERN.
1675 1231 10113754           DI : XREG     ←     WORD2      / LOAD THE 16 LSB'S OF PATTERN.
1676                                                        /   (HARDWARE SWAPS THESE WORDS END-
1677                                                        /   FOR-END DURING LOADING)
1678 1232 27616377         ZREG = 377     PASS       ,U     / CLEAR ZREG INITIALLY   WORK IN +TRUE
1679 1233 27636377         ZREG = 377     PASS       ,L     /   TO SAVE A WORD OF CODE.
1680 1234 30122064 WLOOP  COUNT =         DEC   COUNT,L     / COUNT DOWN # SHIFTS REQUIRED
1681 1235 44440000           CC = TNZRO               ,RS   / DONE SHIFTING?
1682 1236 64001140           BR : CDER1                     / YES, GO SEND DISPLACEMENT & DATA.
1683 1237 36417740         ZREG =         PASS ZREG ,SL     / NO, SHIFT ZREG ONCE WITH 1-FILL.
1684 1240 36410340         YREG =         PASS YREG ,SL     / SHIFT YREG ONCE WITH 1-FILL.
1685 1241 44540000           CC = TMSB                ,RS   / LOOK AT PREVIOUS YREG MSB
1686 1242 64001244           BR : SHFTX                     / 1 (+TRUE), DON'T WORRY ABOUT ZREG.
1687 1243 26237401         ZREG = 1       XOR   ZREG ,L     / 0, SO SHIFT A 0 INTO ZREG LSB
1688 1244 37706354 SHFTX   XREG =         PASS XREG ,SL     / SHIFT XREG LEFT ONCE WITH 1-FILL.
1689 1245 44540000           CC = TMSB                ,RS   / LOOK AT PREVIOUS XREG MSB
1690 1246 64001250           BR : ADJX                      / 1 (+TRUE), DON'T WORRY ABOUT YREG.
1691 1247 26230001         YREG = 1       XOR   YREG ,L     / 0, SO SHIFT A 0 INTO YREG LSB
1692 1250 33766074 ADJX    XREG =         INC   XREG ,L     / XREG MUST END UP WITH 0-FILL.
1693 1251 64001234           BR : WLOOP                     / GO SEE IF WE'RE DONE SHIFTING.
```

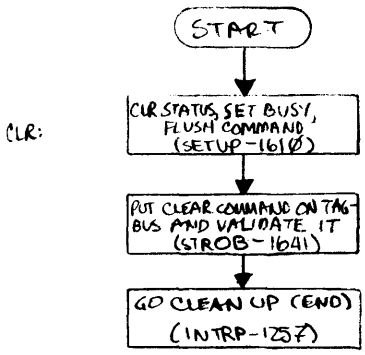
SUGGESTED USE OF RQSYN



This use of RQSYN is suggested because occasionally a random transmission error will occur that can be more quickly corrected with a reREAD rather than by subsequent use of RQSYN.

SET FILE MASK, CLEAR



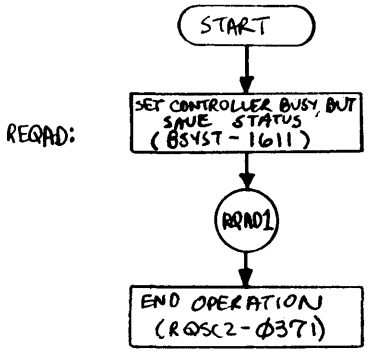


Clears all disc drives (must be used with extreme caution in multi-CPU applications).

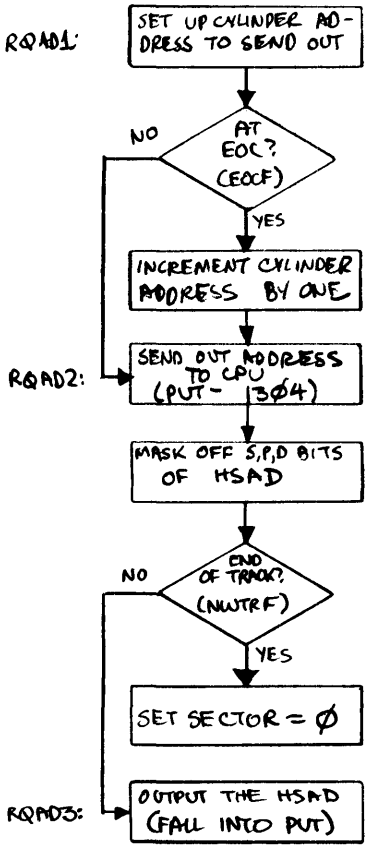
```
1694                          SET FILE MASK, CLEAR COMMANDS
1695                 /
1696                 /
1697                 /
1698                 /
1699                 /  THE SET FILE MASK (SFMSK) COMMAND ROUTES BITS 7-0 OF THE COMMAND
1700                 /  WORD TO APPROPRIATE DESTINATIONS.  BITS 3-0 OF THIS WORD ARE
1701                 /  SAVED IN THE FILE MASK REGISTER AND ARE INTERPRETED AS FOLLOWS:
1702                 /
1703                 /    BIT 0:  ALLOW AUTOMATIC INCREMENTAL-DECREMENTAL SEEK.
1704                 /    BIT 1:  SET ==> CYLINDER MODE, CLEAR ==> SURFACE MODE.
1705                 /    BIT 2:  ALLOW AUTOMATIC TRACK SPARING.
1706                 /    BIT 3:  IF BIT 0 SET, SET ==> DECREMENT, CLEAR ==> INCREMENT.
1707                 /            IF BIT 0 CLEAR, BIT 3 IS IGNORED
1708                 /
1709                 /  BITS 7-4 ARE SENT TO THE 3000 INTERFACE AS A RETRY COUNTER FOR
1710                 /  DATA TRANSFER OPERATIONS IN WHICH ONE OR MORE ERRORS OCCUR.
1711                 /
1712 1252 66001610 SFMSK     CA : SETUP                    / SET UP STATUSES (STATI???)
1713 1253 17625555           DO : FLMSK  ←   CMWD,L       / PUT FILE MASK OUT TO REGISTER.
1714 1254 07622453           DO : IFNBF  ←   SRTRY,L      / SET UP RETRY COUNT
1715 1255 17601755           DO : IDTBF  ←   CMWD
1716 1256 66001630           CA : ICLCK
1717 1257 66001702 INTRP     CA : TRNOF                    / CLOCKS OFF, WRT TIO, CLEAR BUSY
1718 1260 66001315           CA : DFLST                    / SET THE 2100 DATA FLAG.
1719 1261 64000141           BR : CMDWT                    / GO WAIT FOR NEXT COMMAND
1720                 /
1721                 /
1722                 /    THE CLEAR COMMAND PROCESSOR CLEARS ALL DISC DRIVES.  IT MUST
1723                 /  BE USED WITH EXTREME CAUTION (IF AT ALL) IN MULTI-CPU SYSTEMS
1724                 /
1725 1262 66001610 CLR       CA : SETUP                    / CLR STATUS, SET BUSY, FLUSH CMND
1726 1263 07624012           DO : TGBUS  ←   CLRCM,L      / PUT OUT CLEAR COMMAND AND
1727 1264 66001641           CA : STROB                    /   VALIDATE IT
1728 1265 64001257           BR : INTRP                    / GO CLEAN UP
1729                 /
1730                 /
1731                 /  BECAUSE OF CONTROL STORE SPACE LIMITATIONS, THE CLEAR UNIT BUSY
1732                 /  COMMAND (CLRUB) HAS BEEN DELETED   ITS FUNCTION, CLEARING THE
1733                 /  HOLD BIT OF DRIVES ATTACHED TO INTERFACES WHOSE CPU HAS DIED,
1734                 /  IS NOW AUTOMATICALLY PROGRAMMED AS PART OF THE TIME-OUT
1735                 /  PROCESSOR   SHOULD IT BE (POSSIBLE-REQUIRED-DESIRED) (CHOOSE
1736                 /  ONE OR MORE) TO USE IT AGAIN IN THE FUTURE, LISTINGS DATED
1737                 /  6-19-75 AND EARLIER CONTAIN THE MICROCODE USED IN THE COMMAND
1738                 /  PROCESSOR   THERE WERE NO KNOWN BUGS IN THE COMMAND AT THAT TIME.
1739                 /
1740                 /
1741                 /  TO IMPLEMENT LONGER DISC AND INTERFACE CLOCK STROBES, THE
1742                 /  REQUEST UNIT ALLOCATION AND TIME OUT INTERRUPTS COMMAND
1743                 /  HAS BEEN DELETED   SHOULD IT BECOME POSSIBLE TO USE IT
1744                 /  AGAIN IN THE FUTURE, LISTINGS DATED 4-11-75 AND EARLIER
1745                 /  CONTAIN THE MICROCODE USED IN THE COMMAND PROCESSOR AND
1746                 /  ASSOCIATED SUBROUTINES.  THERE WERE NO KNOWN BUGS IN THE
1747                 /  COMMAND AT THAT TIME.
```

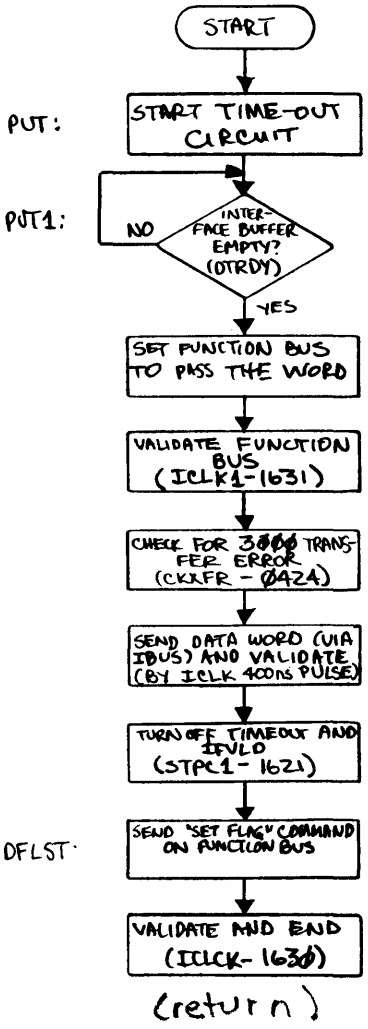
```
1748                          REQUEST DISC ADDRESS COMMAND, SUBROUTINE PUT
1749                 /
1750                 /
1751                 /    THE REQAD (REQUEST DISC ADDRESS) COMMAND IS USED WHENEVER THE
1752                 /  USER WANTS TO KNOW THE DISC ADDRESS CURRENTLY BEING POINTED TO
1753                 /  BY THE CONTROLLER.  IN GENERAL, THIS WILL BE THE CONTENTS OF THE
1754                 /  CONTROLLER REGISTERS CYLAD AND HSAD   THE CONTROLLER'S DISC
1755                 /  ADDRESS IS ALWAYS SUCH THAT A SUBSEQUENT DATA TRANSFER (OR VERIFY)
1756                 /  OPERATION MAY OCCUR WITHOUT RE-ADDRESSING THE CONTROLLER WITH A
1757                 /  SEEK OR ADDRESS RECORD COMMAND   THIS MEANS THAT IN CASE OF AN
1758                 /  ERROR DURING THE DATA TRANSFER, CYLAD AND HSAD POINT TO THE SECTOR
1759                 /  IN WHICH THE ERROR OCCURRED   THIS INFORMATION IS USEFUL TO THE
1760                 /  SYSTEM DURING MULTIPLE-SECTOR TRANSFERS, AND ALSO ALLOWS RE-READS.
1761                 /  IF NO ERROR OCCURRED, CYLAD AND HSAD USUALLY POINT TO THE NEXT
1762                 /  SECTOR TO BE TRANSFERRED
1763                 /    AT THE END OF A TRACK OR CYLINDER, THE CONTENTS OF CYLAD AND HSAD
1764                 /  ARE ONLY PARTIALLY UPDATED BY THE INCHS ROUTINE.  THE REST OF THE
1765                 /  UPDATING OCCURS WHEN THE NEXT TRANSFER BEGINS.  THIS IS TO AVOID
1766                 /  A POSSIBLE END OF CYLINDER ERROR (SEE THE DESCRIPTION FOR
1767                 /  SUBROUTINE SECTR)   A REQAD ISSUED HERE WOULD RETURN THE WRONG
1768                 /  LOGICAL ADDRESS TO THE USER, SO THE END OF CYLINDER AND NEW TRACK
1769                 /  FLAGS (EOCF AND NWTRF) ARE USED TO MODIFY THESE ADDRESSES
1770                 /  APPROPRIATELY BEFORE SENDING THEM OFF
1771                 /    SUBROUTINE RQAD1 IS SEPARATED OUT SO THAT THE RQSYN PROCESSOR CAN
1772                 /  USE IT TOO.  EOCF AND NWTRF ARE ALWAYS FALSE DURING RQSYN.
1773                 /
1774 1266 66001611 REQAD    CA : BSYST                  / SET CONTROLLER BUSY, SAVE STATUS
1775 1267 66001271          CA : RQAD1                  / SO "RQSYN" CAN USE ALSO.
1776 1270 64000371          BR : RQSC2                  / GO END THE OPERATION
1777                 /
1778 1271 35303260 RQAD1  BUF1 =       CMP  CYLAD       / SEND OUT CYLINDER ADDRESS
1779 1272 43440000          CC = EOCF           ,RS     / INCREMENT IT BY 1 IF AT EOC
1780 1273 64001275          BR : RQAD2                  / DON'T BOTHER IT OTHERWISE.
1781 1274 30102264        BUF1 =       DEC  BUF1        / EOC, ADD 1 TO +TRUE CYLAD
1782 1275 66001304 RQAD2    CA : PUT                    / THERE IT GOES.
1783 1276 37616270       HSADB =       PASS HSAD        / PUT HSAD IN -B- REGISTER
1784 1277 27417437       HSADB = 37    AND  HSADB,U     /   SO WE CAN MASK OFF SPD BITS
1785 1300 42540000          CC = NWTRF           ,RS     / RESET SECTOR TO 0 IF AT END OF
1786 1301 64001303          BR : RQAD3                  /   TRACK, ELSE LEAVE IT ALONE.
1787 1302 27636000       HSADB = 0     PASS       ,L     / END OF TRACK, SET SECTOR = 0.
1788 1303 35303660 RQAD3  BUF1 =       CMP  HSADB       / GIVE HSAD TO BUF1
1789                                                    /   AND FALL INTO PUT
1790                 /
1791                 /
1792                 /  SUBROUTINE PUT WRITES ONE WORD TO THE INTERFACE.  THE WORD
1793                 /  IS IN BUF1 ON ENTRY   DFLST SETS THE 2100 INTERFACE FLAG.
1794                 /  PUT IS A SECOND-LEVEL SUBROUTINE.
1795                 /
1796 1304 07600500 PUT      DO : TIMER  ←   START,U     / TURN ON TIME-OUT CIRCUIT
1797 1305 42100000 PUT1     CC = DTRDY                  / INTERFACE BUFFER EMPTY?
1798 1306 64001305          BR : PUT1                   / NO, WAIT UNTIL IT IS
1799 1307 07622443          DO : IFNBF  ←   IFIN ,L     / YES, SET UP TO PASS THE WORD
1800 1310 66001631          CA : ICLK1                  / CAN'T CALL DSTRT -- TOO DEEP
1801 1311 66000424          CA : CKXFR                  / CHECK FOR 3000 CHANNEL ERROR.
1802 1312 17600745          DO : IDTBF  ←   BUF1        / O.K., SEND THE DATA WORD
1803 1313 17600745          DO : IDTBF  ←   BUF1        /   (400 NSEC IFCLK PULSE)
1804 1314 66001621          CA : STPC1                  / TURN OFF TIME-OUT AND IFYLD
1805 1315 07622676 DFLST    DO : IFNBF  ←   STDFL,L     / SEND OUT "SET FLAG" COMMAND.
1806 1316 64001630          BR : ICLCK
```

REQUEST DISC ADDRESS, PUT



Sends CPU current disc address (CYLAD and HSAD).





Puts one word to the interface, validates with 400 nsec $\overline{\text{IFCLK}}$ pulse.

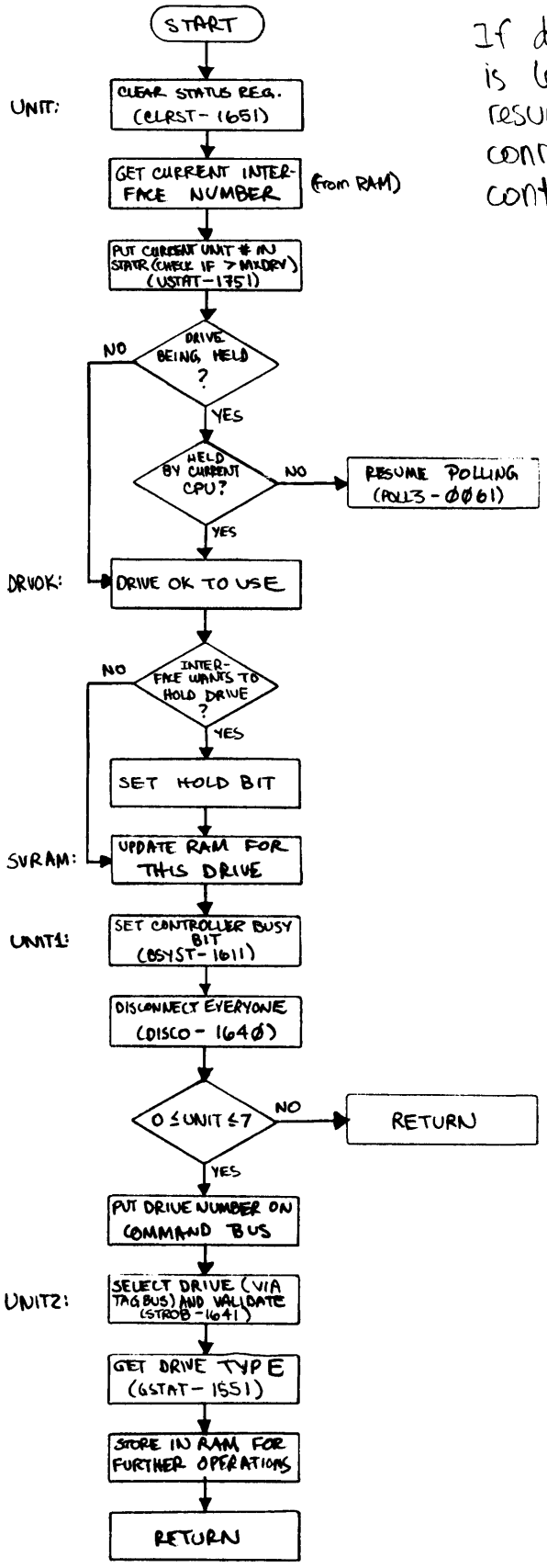
turns on IFVLD

Sets 2ØØ data flag

```
1807                        DRIVE NUMBER VERIFICATION AND SELECT ROUTINE
1808                /
1809                /
1810                /
1811                /
1812                /    THE FOLLOWING DIAGRAM IS THE LAYOUT OF THE 64-BIT (16X4) RAM WHICH
1813                /  MAPS THE DISC UNIT NUMBER (SAME AS THE RAM WORD NUMBER EXCEPT FOR
1814                /  NUMBERS 11-15) INTO THE NUMBER OF THE INTERFACE WHICH LAST
1815                /  ACCESSED THAT DRIVE.  WORD 15 CONTAINS THE NUMBER OF THE
1816                /  INTERFACE LAST POLLED TO SEE IF A COMMAND WAS PENDING.  WORD
1817                /  14 CONTAINS THE NUMBER OF THE INTERFACE CURRENTLY CONNECTED TO
1818                /  THE CONTROLLER   WORD 13 IS A SECTOR COUNTER USED BY THE
1819                /  "SPARE" SUBROUTINE.  WORD 12 HOLDS THE DRIVE TYPE, RETURNED IN
1820                /  BITS 12-9 OF THE DRIVE STATUS WORD   THIS WORD DETERMINES HOW
1821                /  MANY HEADS PER DRIVE AND SECTORS PER TRACK THE DRIVE HAS.  IF
1822                /  BIT 3 OF WORD 11 IS SET, THE PLATTER PROTECT SWITCH FOR THE
1823                /  CURRENT SURFACE (7905) OR THE READ-ONLY SWITCH FOR THE ENTIRE
1824                /  DISC PACK (7920, 7925) IS ON, LOCKING OUT WRITING OF ANY KIND
1825                /  IF BIT 2 IS ON, THE DRIVE'S FORMAT SWITCH IS SET TO OVERRIDE.
1826                /  WORD 8 HOLDS THE NUMBER OF THE LAST DRIVE FOR WHICH THE
1827                /  CONTROLLER PROCESSED AN ATTENTION REQUEST   COMMAND WORDS
1828                /  SHOULD NOT REFER TO UNIT 8 OR ERRORS MAY OCCUR.
1829                /    ALL INFORMATION IS STORED GROUND TRUE.
1830                /
1831                /
1832                /        BIT  3 2 1 0    WORD
1833                /             ---------
1834                /            ! X I I I !  15
1835                /            ! X I I I !  14
1836                /            ! C C C C !  13
1837                /            ! DRV TYP !  12
1838                /            ! RD ONLY !  11
1839                /            ! I I I H !  10
1840                /            ! I I I H !   9
1841                /            ! PRV ATN !   8
1842                /            ! I I I H !   7
1843                /
1844                /
1845                /            ! I I I H !   1
1846                /            ! I I I H !   0
1847                /             ---------
1848                /
1849                /
1850                /   WHERE I  IS A 3-BIT NUMBER (0-7) REPRESENTING THE INTERFACE
1851                /            TO WHICH THE ASSOCIATED DRIVE (WORD NUMBER) WAS LAST
1852                /            CONNECTED   FOR WORDS 15 AND 14 ONLY, THE I-FIELD IS
1853                /            AS DESCRIBED ABOVE THE DIAGRAM.  WORDS 15 AND 14 ARE
1854                /            THE SAME EXCEPT WHEN THE CONTROLLER IS RESPONDING TO
1855                /            A DRIVE ATTENTION BIT   THERE CAN BE NO DISC DRIVE
1856                /            11-15.
1857                /
1858                /          H IF SET MEANS THAT THE INTERFACE HAS RESERVED (HELD) THE
1859                /            DRIVE FOR A SERIES OF OPERATIONS   WHILE H IS SET,
1860                /            NO OTHER INTERFACE MAY ACCESS THAT DRIVE.
1861                /
1862                /          C IS A SECTOR COUNTER USED BY SUBROUTINE "SPARE"
1863                /
1864                /          X IS NOT USED
```

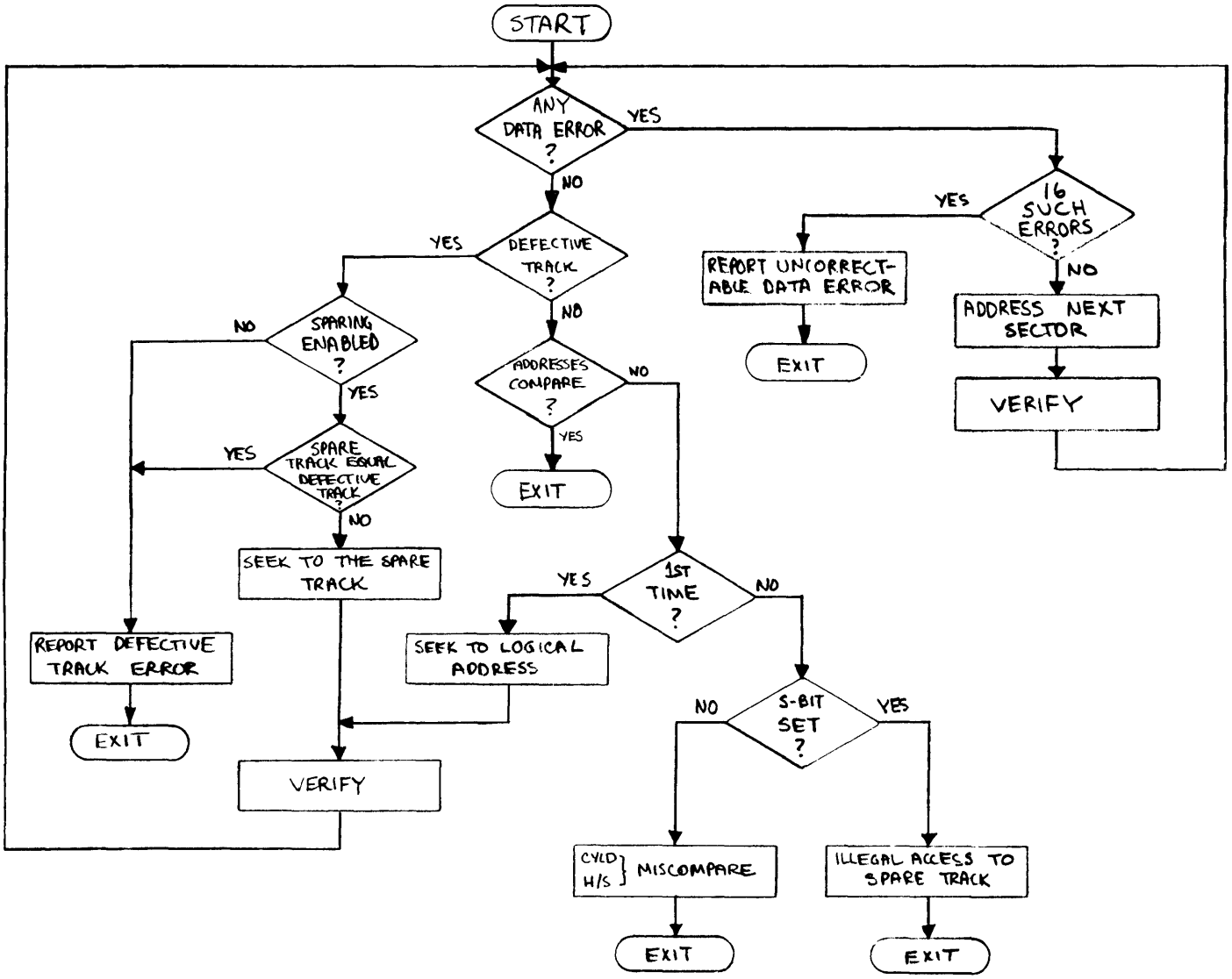
```
1865                          DRIVE NUMBER VERIFICATION AND SELECT ROUTINE
1866                  /
1867                  /
1868                  /
1869                  /
1870                  /    SUBROUTINE UNIT EXAMINES THE UNIT NUMBER FIELD OF THE CPU
1871                  /  COMMAND WORD   THE FIELD IS TESTED FOR VALIDITY
1872                  /  (0 <= UNIT <= 10), THEN THE WORD IN RAM CORRESPONDING TO
1873                  /  THAT DRIVE IS EXAMINED   IF THE DRIVE HAS NOT BEEN RESERVED
1874                  /  FOR USE (HOLD BIT NOT SET) BY ANOTHER CPU, IT IS
1875                  /  ASSIGNED TO THE CURRENT CPU.  THE HOLD BIT WILL BE SET ONLY
1876                  /  IF THE HOLD BIT IN THE COMMAND WORD IS SET   IF THE DRIVE HAS
1877                  /  BEEN RESERVED BY ANOTHER CPU, THE COMMAND IS LEFT PENDING AND
1878                  /  THE CONTROLLER RESUMES POLLING.  IF THE DRIVE IS AVAILABLE OR IS
1879                  /  HELD BY THE CURRENT CPU, IT IS CONNECTED TO THE CONTROLLER
1880                  /  (0 <= UNIT <= 7 ONLY) AND THE CONTROLLER BUSY BIT IS SET ON THE
1881                  /  CURRENT INTERFACE.  THE DRIVE TYPE IS SET IN RAM(12) FROM BITS
1882                  /  12-9 OF THE DRIVE STATUS WORD
1883                  /    UNIT MUST BE CALLED FROM LEVEL 0, SINCE IT CALLS BSYST WHICH IS
1884                  /  TWO LEVELS DEEP
1885                  /
1886 1317 66001651 UNIT      CA : CLRST                    / CLEAR STATUS REGISTER (STATR)
1887 1320 07620016           DO : RAMAD  ←   CURNT,L       / GET THE CURRENT INTERFACE NUMBER
1888 1321 10120444           DI : BUF1   ←   RAM  ,L       /   IN THE LOW THREE BITS OF BUF1
1889 1322 66001751           CA : USTAT                    / PUT CURRENT UNIT# IN STATR,L,
1890                                                       /   CHECK FOR LEGAL DRIVE REQUEST
1891 1323 16420405           DO : RAMAD  ←   STATR,L       / DRIVE NUMBER O.K., FIND OUT
1892 1324 10020456           DI : BUF3   ←   RAM  ,L       /   IF DRIVE IS BEING HELD
1893 1325 36437520         BUF3 =        PASS BUF3 ,L,SR   / TEST HOLD BIT
1894 1326 44640000           CC = TLSB             ,RS
1895 1327 64001333           BR : DRVOK                    / HOLD BIT CLEAR, SAFE TO USE.
1896 1330 36223464        DUMMY = BUF1   XOR  BUF3 ,L      / HOLD BIT SET, CPU'S BETTER MATCH.
1897 1331 44400000           CC = TNZRO                    / DO THEY?
1898 1332 64000061           BR : POLL3                    / NO, GO RESUME POLLING.
1899 1333 37616344 DRVOK  BUF3  =        PASS BUF1 ,SL     / O.K. TO USE DRIVE, MERGE CURRENT
1900 1334 36402060        DUMMY =        PASS COMAD,U      /   INTERFACE NUMBER WITH HOLD BIT
1901 1335 44540000           CC = TNSB             ,RS     /   FROM COMMAND AND SAVE IN RAM.
1902 1336 64001340           BR : SVRAM                    / INTERFACE WANTS TO RELEASE DRIVE.
1903 1337 26637401         BUF3 = 1      OR   BUF3 ,L      / IT WANTS TO HOLD DRIVE, SET HOLD BIT
1904 1340 16421455 SVRAM     DO : RAM    ←   BUF3 ,L       / UPDATE RAM FOR THIS DRIVE
1905 1341 66001611 UNIT1     CA : BSYST                    / ENTRY POINT FROM STATUS OR RQSCT,
1906                                                       /   SET CONTROLLER BUSY
1907 1342 66001640           CA : DISCO                    / DISCONNECT EVERYONE
1908 1343 27422410        DUMMY = 10     AND  STATR,L      / CONNECT DRIVE ONLY IF
1909 1344 44400000           CC = TNZRO                    /   0 <= UNIT <= 7
1910 1345 72000000           RT : 0                        / > 7, RETURN HERE.
1911 1346 17621515           DO : CBUF   ←   COMWD,L       / PUT DRIVE NUMBER ON COMMAND BUS.
1912 1347 07624005 UNIT2     DO : TGBUS  ←   SLECT,L       / ENTRY POINT FROM ATTN ROUTINE.
1913 1350 66001641           CA : STROB                    / SELECT THE DRIVE.
1914 1351 66001551           CA : GSTAT                    / FIND OUT WHAT TYPE IT IS
1915 1352 27502036         BUF1 = 36     AND  BUF2 ,U      /   (IN BUF2 BITS 12-9)
1916 1353 37702204         BUF1 =        PASS BUF1 ,SW     / POSITION IT INTO BUF1(3-0)
1917 1354 37702324         BUF1 =        PASS BUF1 ,SR
1918 1355 07620014           DO : RAMAD  ←   DRTYP,L       /   AND SAVE IT FOR ALL
1919 1356 17620445           DO : RAM    ←   BUF1 ,L       /   OPERATIONS ON THIS DRIVE.
1920 1357 72000000           RT : 0
```

UNIT



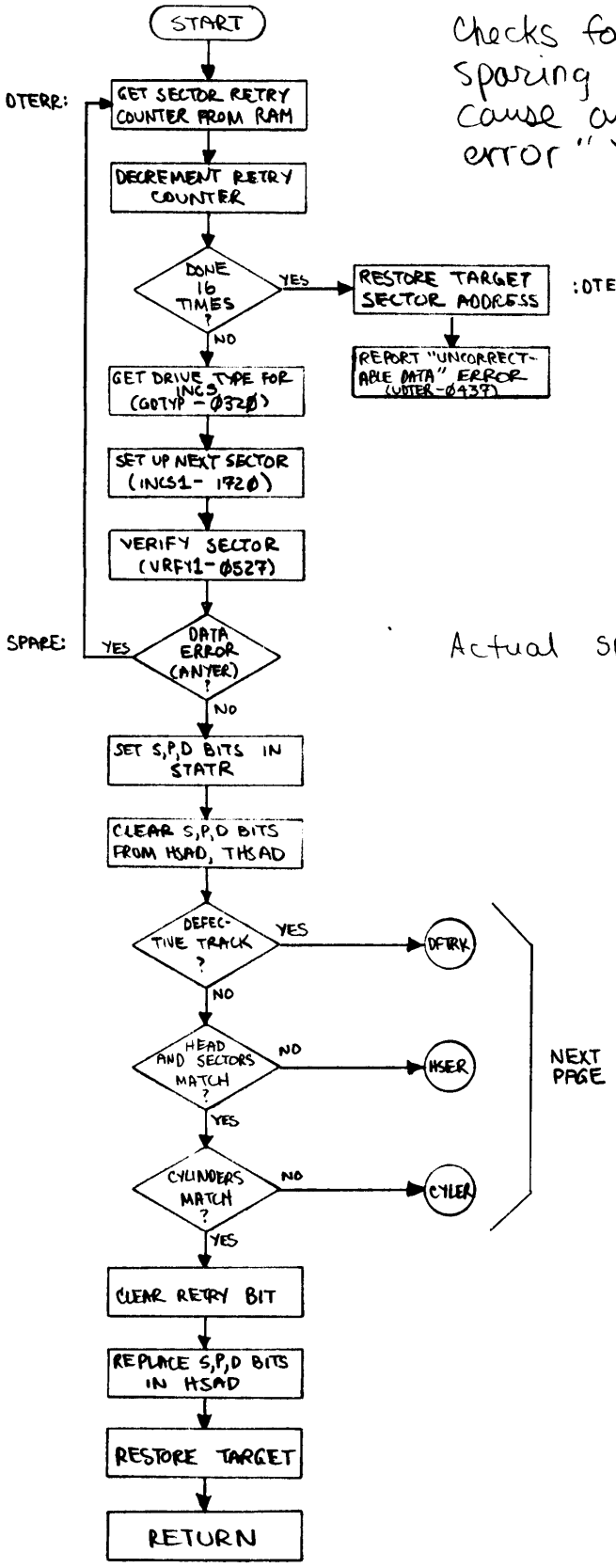
If drive is reserved, command is left pending and controller resumes polling; otherwise connection is made and the controller busy bit is set.

BASIC SPARING SUB-ROUTINE



Note: the next two pages contain the detailed flowchart derived strictly from the μcode

TRACK SPARING ROUTINE
(2 PAGES)

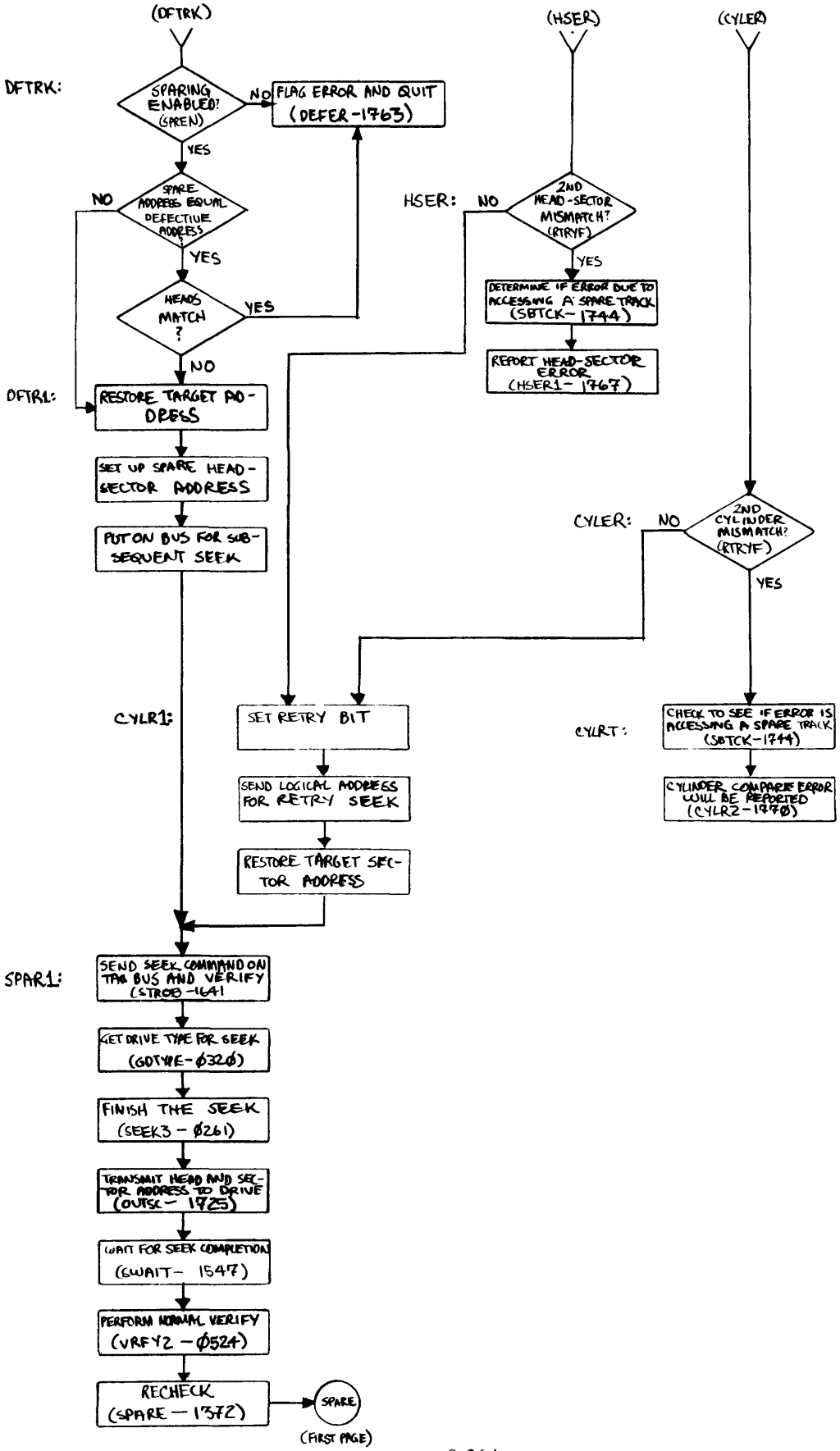


Checks for errors encountered when sparing (16 data errors will cause an "uncorrectable data error").

Actual sparing algorithm.

```
1921                                TRACK SPARING ROUTINE
1922                    /
1923                    /
1924                    /
1925                    /
1926                    /  SUBROUTINE SPARE IS THE ROUTINE THAT IMPLEMENTS THE ACTUAL
1927                    /  SPARING ALGORITHM.  IT FOLLOWS A CALL TO VRFY AND USES THE
1928                    /  ADDRESSES SAVED IN THSAD AND TCYLD TO ACCESS THE SPARE TRACK.
1929                    /  THE ENTRY POINT ("SPARE") IS NOT AT THE TOP OF THE CODE SO
1930                    /  THAT DTERR CAN FALL INTO SPARE IN CASE OF RETRIES.
1931                    /
1932                    /
1933                    /
1934                    /
1935                    /  IN THE PROCESS OF TRYING TO SPARE, A DATA ERROR HAS BEEN ENCOUNTERED
1936                    /  SO WE CAN'T RELY ON THE CONTENTS OF THSAD AND TCYLD BEING VALID
1937                    /  UP TO THE NEXT 15 SECTORS ARE TRIED, UNTIL A GOOD ONE IS FOUND
1938                    /  IF ALL 16 SECTORS HAVE DATA ERRORS, THE PROCESS IS ABORTED WITH AN
1939                    /  ERROR STATUS.
1940                    /
1941 1360 07620015 DTERR     DO : RAMAD  ←   NSEC ,L     / GET SECTOR RETRY COUNTER,
1942 1361 10120440          DI : REGO   ←   RAM  ,L     /   UPDATE AND CHECK.
1943 1362 30120060        REGO =        DEC  REGO ,L     / DECREMENT RETRY COUNTER
1944 1363 44140000          CC = LOVER            ,RS    /   AND CHECK FOR UNDERFLOW
1945 1364 64001416          BR : DTER2                   / TOO MANY RETRIES => QUIT
1946 1365 17620041          DO : RAM    ←   REGO ,L     / STORE UPDATED RETRY COUNT
1947 1366 37702204        BUF1 =        PASS BUF1 ,SW    / RESTORE BUF1 FOR NEXT VRFY
1948 1367 66000320          CA : GDTYP                   / GET DRIVE TYPE FOR INCS
1949                                                     /   (AVOIDS 4-LEVEL NESTING).
1950 1370 66001720          CA : INCS1                   / SET UP NEXT SECTOR
1951 1371 66000527          CA : VRFY1                   /   AND TRY IT FOR SIZE.
1952 1372 37702204 SPARE  BUF1 =        PASS BUF1 ,SW    / TO GET SECT ADDR RIGHT AGAIN.
1953 1373 43340000          CC = ANYER            ,RS    / WAS THERE A DATA ERROR?
1954 1374 64001360          BR : DTERR                   / YES, SEE IF WE'VE TRIED 16 SECTORS
1955 1375 27412340       STATR = 340    AND  THSAD,U     / NO, SET S, P, AND D BITS IN STATR.
1956 1376 27402040       DUMMY = 40     AND  THSAD,U     / CHECK FOR DEFECTIVE TRACK.
1957 1377 44400000          CC = TNZRO                   / SET CC IF D-BIT SET
1958 1400 37616070        BUF3 =        PASS HSAD ,U     / DO A LITTLE COMMON HOUSEWORK
1959 1401 27505437        HSAD = 37     AND  BUF3 ,U     /   BEFORE BRANCHING, CLEAR SPD
1960 1402 27410037       THSAD = 37     AND  THSAD,U     /   BITS FROM HSAD AND THSAD
1961 1403 64001420          BR : DFTRK                   / BRANCH HERE ONLY IF D-BIT SET
1962 1404 36202270       DUMMY = HSAD   XOR  THSAD      / NO D-BIT,
1963 1405 44400000          CC = TNZRO                   /   DO HEAD-SECTORS MATCH?
1964 1406 64001435          BR : HSER                    / NO, THIS TRACK'S IN PAIN
1965 1407 36203260       DUMMY = TCYLD XOR  CYLAD       / HSAD O.K., SET TO CHECK CYLAD
1966 1410 44400000          CC = TNZRO                   / DO CYLINDERS MATCH?
1967 1411 64001441          BR : CYLER                   / NO, WE'RE HURTING BAD
1968 1412 07623377          DO : RETRY  ←   FALSE,L     / ALL OK, CLEAR RETRY BIT
1969 1413 36704470        HSAD = HSAD   OR   STATR,U     / REPLACE S, P, D, BITS IN HSAD
1970 1414 37724064        HSAD =        PASS BUF1 ,L     / RESTORE TARGET (DTERR MAY MODIFY HSAD)
1971 1415 72000000          RT : 0                       /   AND RETURN (NO SPARING NECESSARY)
1972                    /
1973                    /
1974                    /  THERE'S NO HOPE LEFT AT ALL; WE SEEM TO HAVE RUN OUT OF RETRIES
1975                    /  THE ONLY THING WE CAN DO IS TELL SOMEONE ABOUT THE ERROR
1976                    /
1977 1416 37724064 DTER2  HSAD =        PASS BUF1 ,L     / RESTORE TARGET SECTOR ADDRESS
1978 1417 64000437          BR : UDTER                   / REPORT UNCORRECTABLE ERROR.
```

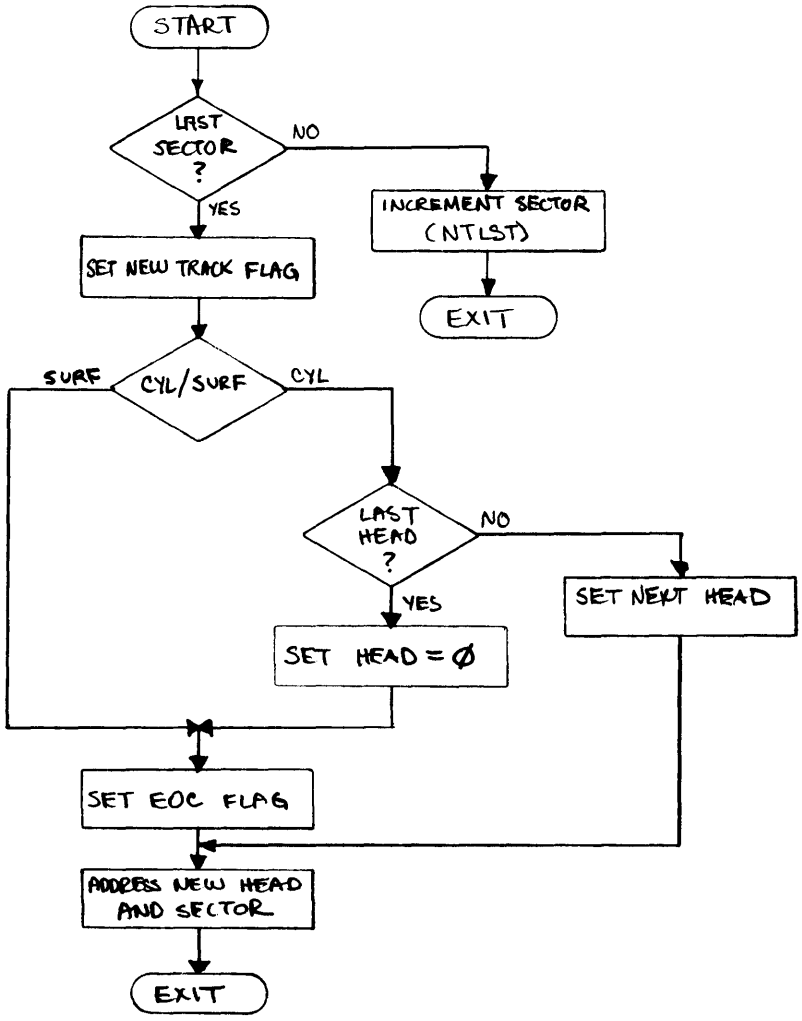
```
1979                          TRACK SPARING ROUTINE
1980                  /
1981                  /
1982                  /
1983                  /    A SECTOR WITH NO ERROR BUT MARKED DEFECTIVE MEANS THAT A SPARE
1984                  /  TRACK SHOULD BE ACCESSED BECAUSE THERE IS AN IRRECOVERABLE ERROR
1985                  /  ON SOME OTHER SECTOR.  SPARE TRACK ACCESS OCCURS HERE   TO AVOID
1986                  /  AN INFINITE LOOP IF THE D-BIT IS SET BUT THE ADDRESS FIELD POINTS
1987                  /  TO THE SAME DEFECTIVE CYLINDER AND HEAD, THIS CONDITION IS TESTED
1988                  /  AND, IF FOUND TO BE TRUE, THE OPERATION IS ABORTED AS IF SPARE
1989                  /  TRACK ACCESS WERE NOT ENABLED
1990                  /
1991 1420 43540000 DFTRK     CC = SPREN            ,RS    / IS SPARING ENABLED?
1992 1421 64001763           BR : DEFER                   / NO, FLAG ERROR AND QUIT
1993 1422 36203260        DUMMY = TCYLD XOR  CYLAD        / SPARING ENABLED, TEST FOR
1994 1423 44400000           CC = TNZRO                   /   SPARE ADDRESS = DEFECTIVE ADDR
1995 1424 64001430           BR : DFTR1                   / CYLAD'S DON'T MATCH, ALL O.K.
1996 1425 36202070        DUMMY = HSAD  XOR  THSAD,U      / CYLAD'S MATCH, HEADS BETTER NOT
1997 1426 44440000           CC = TNZRO           ,RS
1998 1427 64001763           BR : DEFER                   / THEY DO, THROW THE BUM OUT
1999 1430 37630064 DFTR1  THSAD =        PASS BUF1 ,L    / RESTORE TARGET SECTOR ADDRESS
2000 1431 37724064         HSAD =        PASS BUF1 ,L    /   (IN CASE OF VRFY RETRIES)
2001 1432 36416260         BUF3 =        PASS THSAD      / SET UP SPARE HEAD-SECT ADDRESS.
2002 1433 14000301           DO : CBUF    +   TCYLD,C    / SEEK TO THE SPARE TRACK.
2003 1434 64001447           BR : SPAR1                   / DO THE SEEK, THEN RECHECK
2004                  /
2005                  /
2006                  /  AN ADDRESS ERROR--WE MAY HAVE INCREMENTED OFF THE END OF
2007                  /  A SPARE TRACK, SO RETRY ONCE
2008                  /
2009 1435 43140000 HSER     CC = RTRYF            ,RS    / HEAD-SECTOR MISMATCH, 2ND TIME?
2010 1436 64001443           BR : CYLR1                   / NO, WE STILL HAVE A CHANCE.
2011 1437 66001744           CA : SBTCK                   / YES, SHOW NO (MORE) MERCY,
2012                                                      /   CHECK IF S-BIT SET
2013 1440 64001767           BR : HSER1                   / NO, REAL LIVE HEAD-SECTOR ERROR.
2014                  /
2015 1441 43100000 CYLER    CC = RTRYF                   / CYLINDER MISMATCH, 2ND TIME?
2016 1442 64001457           BR : CYLRT                   / YES, THAT'S ONE TIME TOO MANY!
2017 1443 07623000 CYLR1     DO : RETRY   +   TRUE ,L     / SET RETRY BIT (WE WON'T BE BACK!)
2018 1444 15201311           DO : CBUF    +   CYLAD,C     / RETRY THE OPERATION BY SEEKING
2019                                                      /   TO THE LOGICAL ADDRESS
2020 1445 37724064        HSAD =        PASS BUF1 ,L    / RESTORE TARGET SECTOR ADDRESS
2021 1446 37616270        BUF3 =        PASS HSAD       /   (IN CASE OF VRFY RETRIES)
2022 1447 07624007 SPAR1     DO : TGBUS   +   SEEKC,L
2023 1450 66001641           CA : STROB
2024 1451 66000320           CA : GDTYP                   / GET DRV TYPE FOR SEEK3
2025 1452 66000261           CA : SEEK3                   / FINISH THE SEEK.
2026 1453 66001725           CA : OUTSC                   / (REQUIRED IF DFTRK-SPAR1,
2027                                                      /   REDUNDANT IF HSER OR CYLER)
2028 1454 66001547           CA : SWAIT                   / WAIT FOR SEEK COMPLETION,
2029 1455 66000524           CA : VRFY2                   /   THEN RE-VERIFY NORMALLY
2030 1456 64001372           BR : SPARE                   / FINALLY, RECHECK.
2031                  /
2032                  /
2033                  /  CYLINDER ADDRESS ERROR, CHECK IF SPARE TRACK INDICATOR IS SET
2034                  /
2035 1457 66001744 CYLRT    CA : SBTCK                   / CHECK IF S-BIT SET
2036 1460 64001770           BR : CYLR2                   / NO, GEN-U-WINE CYLINDER ERROR
```


(DFTRK)
DFTRK:
SPARING ENABLED? (SPREN)
NO
FLAG ERROR AND QUIT (DEFER-1763)
YES
SPARE ADDRESS EQUAL DEFECTIVE ADDRESS?
NO
YES
HEADS MATCH ?
YES
NO
DFTR1:
RESTORE TARGET ADDRESS
SET UP SPARE HEAD-SECTOR ADDRESS
PUT ON BUS FOR SUBSEQUENT SEEK
(HSER)
HSER:
NO
2ND HEAD-SECTOR MISMATCH? (RTRYF)
YES
DETERMINE IF ERROR DUE TO ACCESSING A SPARE TRACK (SBTCK-1744)
REPORT HEAD-SECTOR ERROR (HSER1-1767)
(CYLER)
CYLER:
NO
2ND CYLINDER MISMATCH? (RTRYF)
YES
CYLR1:
SET RETRY BIT
SEND LOGICAL ADDRESS FOR RETRY SEEK
RESTORE TARGET SECTOR ADDRESS
CYLRT:
CHECK TO SEE IF ERROR IS ACCESSING A SPARE TRACK (SBTCK-1744)
CYLINDER COMPARE ERROR WILL BE REPORTED (CYLR2-1770)
SPAR1:
SEND SEEK COMMAND ON TAG BUS AND VERIFY (STROB-1641
GET DRIVE TYPE FOR SEEK (GDTYE-0320)
FINISH THE SEEK (SEEK3-0261)
TRANSMIT HEAD AND SECTOR ADDRESS TO DRIVE (OUTSC-1725)
WAIT FOR SEEK COMPLETION (GWAIT-1547)
PERFORM NORMAL VERIFY (VRFY2-0524)
RECHECK (SPARE-1372)
SPARE
(FIRST PAGE)

```
                        INCREMENT HEAD-SECTOR
                /
                /
                /
                /  THE FOLLOWING ROUTINES (INCHS, SECTR AND DECS, TOGETHER WITH
                /  INCS) ARE RESPONSIBLE FOR SELECTING THE NEXT CYLINDER, HEAD AND
                /  SECTOR TO BE ACCESSED   INCS (INCREMENT SECTOR) INCREMENTS THE
                /  SECTOR FIELD OF HSAD BEFORE IT IS OUTPUT (THE LAST LOGICAL SECTOR
                /  IS INCREMENTED TO 0 WITHOUT CHANGING THE HEAD ADDRESS)   (INCS IS
                /  LOCATED AFTER STRT2 TO ELIMINATE A BRANCH INSTRUCTION.)  SIMILARLY
                /  DECS DECREMENTS THE SECTOR FIELD OF HSAD, WITH 0 DECREMENTING TO
                /  THE LAST LOGICAL SECTOR WITHOUT CHANGING THE HEAD ADDRESS.  AN
                /  ADDITIONAL USE OF DECS IS DESCRIBED FARTHER DOWN THIS PAGE.  INCHS
                /  (INCREMENT HEAD AND SECTOR) AND SECTR ARE MORE COMPLICATED AND
                /  DEPEND ON A NUMBER OF FACTORS:
                /
                /  IT IS THE FUNCTION OF INCHS TO DETERMINE WHETHER END-OF-CYLINDER
                /  OR END-OF-TRACK HAS BEEN REACHED, BASED ON ADDRESS MODE AND SECTOR
                /  ADDRESS, AND TRANSMIT THE NEXT SECTOR OR HEAD-SECTOR TO THE DRIVE
                /  AS REQUIRED   THE ADDRESS MODES ARE:
                /
                /     1   SURFACE--HEADS WILL NOT BE SWITCHED AT THE END OF
                /         ANY TRACK   THE OPERATION MAY CONTINUE ON THE SAME
                /         HEAD, NEXT CYLINDER.
                /
                /     2.  CYLINDER--A CYLINDER CONSISTS OF ALL TRACKS AT A GIVEN
                /         ADDRESS   HEAD SWITCHING WILL BE ALLOWED IN A DOWNWARD
                /         MANNER, WITH HEAD 0 OF THE NEXT CYLINDER FOLLOWING THE
                /         HIGHEST-NUMBERED HEAD OF THE CURRENT TRACK.  STORAGE IS
                /         CONSIDERED ALL FIXED OR ALL REMOVABLE
                /
                /  THE HEAD ADDRESS IS TRANSMITTED ONLY IF THE CONTROLLER SWITCHES
                /  HEADS, OTHERWISE ONLY THE SECTOR ADDRESS IS TRANSMITTED SINCE
                /  THE LOGICAL AND PHYSICAL HEAD ADDRESSES MAY NOT AGREE IF SPARING
                /  HAS OCCURED   INCHS IS CALLED AT THE END OF EVERY SECTOR.
                /
                /  SECTR IS CALLED AFTER INCHS ONLY IF THERE IS MORE DATA TO TRANSFER
                /  ITS FUNCTION IS TO PERFORM AN INCREMENTAL OR DECREMENTAL SEEK (AND
                /  VERIFY) IF REQUIRED, AND A NOP IF NOT   IF A NEW TRACK IS STARTED
                /  DURING ANY DATA TRANSFER EXCEPT WFS, RFS OR INIT (WHETHER BY SEEK
                /  OR BY SWITCHING HEADS WHILE IN CYLINDER MODE), A SECTOR IS VERIFIED
                /  (AND A SPARE TRACK IS ACCESSED IF NECESSARY) BEFORE CONTROL RETURNS
                /  TO THE DATA TRANSFER COMMAND PROCESSOR   IF INCREMENTAL (DECREMENTAL)
                /  SEEK IS REQUIRED BUT IS NOT ALLOWED BY THE FILE MASK, AN END-OF-
                /  CYLINDER (EOC) ERROR INTERRUPT IS TAKEN
                /
                /  DECS IS CALLED AT THE START OF ALL DATA TRANSFERS   IT OPERATES
                /  AS DESCRIBED IN THE FIRST PARAGRAPH UNLESS EOC OR THE NEW TRACK
                /  FLAG (NWTRF) IS SET   IF EOC IS STILL SET FROM THE PREVIOUS DATA
                /  TRANSFER, THE OPERATION IS CONSIDERED A CONTINUATION (THAT IS,
                /  NO SEEK OR ADDRESS RECORD COMMAND WAS PERFORMED SINCE THEN) AND
                /  INCREMENTAL (DECREMENTAL) SEEK OCCURS IF ALLOWED   IF NWTRF IS
                /  STILL SET, THE OPERATION IS ALSO A CONTINUATION AND DECS IS A
                /  NOP   THAT IS, THE LAST SECTOR PROCESSED WAS NUMBER N-1 (ON AN
                /  N SECTOR PER TRACK DISC), AND THE FIRST SECTOR TO BE VERIFIED
                /  ON THE NEXT TRACK IS ALSO NUMBER N-1
                /
                /  EOC AND NWTRK ARE CLEARED BY SEEK, ADDRESS RECORD, OR INCREMENTAL
                /  SEEK DONE BY SECTR OR DECS
```

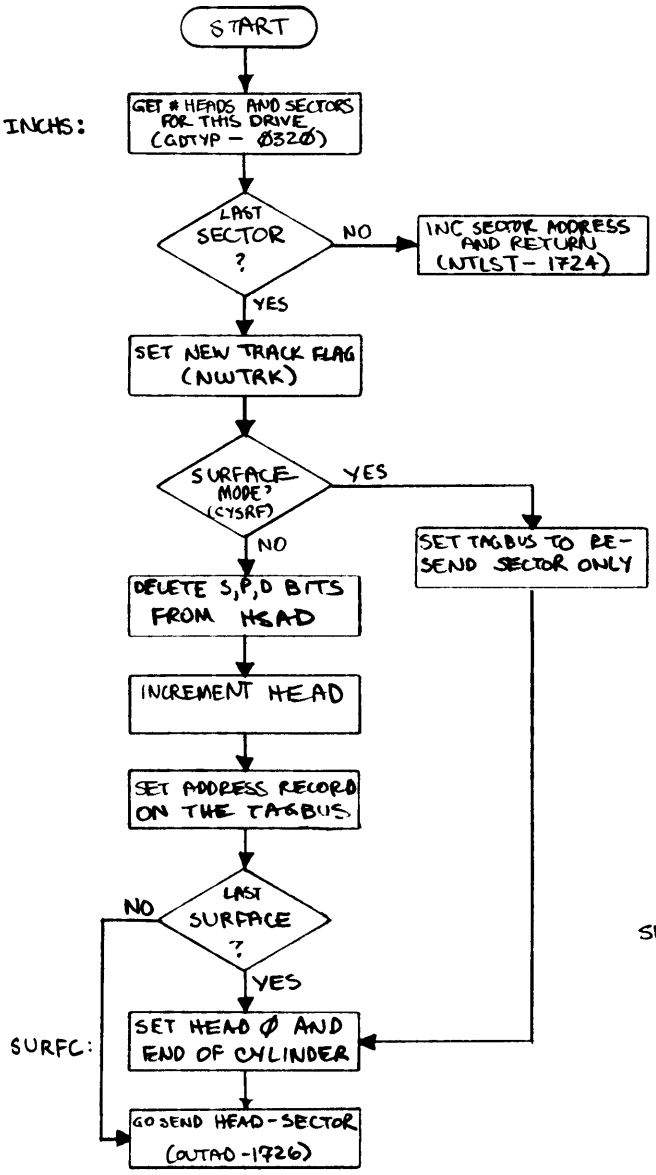
```
2096                          SUBROUTINES:  INCHS, SECTR
2097                 /
2098                 /
2099                 /
2100                 /
2101 1461 66000320 INCHS    CA : GDTYP                  / GET # HDS, SCTRS, THIS DRIVE.
2102 1462 32222070       DUMMY = HSAD  PLUS BUF2 ,L    / CHECK FOR LAST SECTOR.
2103 1463 44140000          CC = LOVER           ,RS
2104 1464 64001724          BR : NTLST                  / NO, JUST INCREMENT SECTOR.
2105 1465 07603400          DO : NWTRK  ←   TRUE ,U     / YES, SET NEW TRACK FLAG.
2106                 /
2107                 /  END OF TRACK.  USE MODE TO DETERMINE WHETHER END-OF-CYLINDER.
2108                 /
2109 1466 43640000          CC = CYSRF           ,RS    / SURFACE MODE?
2110 1467 07624003          DO : TGBUS  ←   XSECT,L     / IF SO, SET TO RE-SEND SECTOR ONLY
2111 1470 64001501          BR : SURFC                  / SUCCEEDS ONLY IF SURFACE MODE.
2112                 /
2113                 /  CYLINDER MODE
2114                 /
2115 1471 37616070       HSADB =       PASS HSAD ,U     / PUT HSAD IN B REGISTER AND
2116 1472 27503437        BUF1 = 37    AND  HSADB,U     /   DELETE S, P, AND D BITS
2117 1473 32202064       DUMMY = BUF1  PLUS BUF2 ,U     / CHECK FOR LAST SURFACE.
2118 1474 44340000          CC = UOVER           ,RS    / SET CC IF NOT LAST SURFACE.
2119 1475 22305401        HSAD = 1     PLUS HSADB,U     / ASSUME NOT (JUST BUMP HEAD)
2120 1476 07624006          DO : TGBUS  ←   ADREC,L     / SET UP HEAD-SECTOR COMMAND
2121 1477 64001726          BR : OUTAD                  / SUCCEEDS ONLY IF NOT LAST SURF
2122 1500 27505740        HSAD = 340   AND  HSADB,U     / LAST SURFACE, SET HEAD 0
2123 1501 07605400 SURFC    DO : EOC    ←   TRUE ,U     /   AND END-OF-CYLINDER.
2124 1502 64001726          BR : OUTAD                  / THEN GO SEND HEAD-SECTOR (CYL)
2125                                                    /   OR SECTOR ONLY (SURFC)
2126                 /
2127                 /
2128                 /  SUBROUTINE SECTR PROPERLY BELONGS IN INCHS, SINCE IT FINISHES
2129                 /  SETTING THE NEXT DISC ADDRESS   IT HAS BEEN SEPARATED OUT TO
2130                 /  AVOID END-OF-CYLINDER ERRORS (AUTO SEEK DISABLED) OR AN EXTRA
2131                 /  SEEK (ENABLED) IF TRANSFER ENDS AT EOC   SECTR MUST BE CALLED
2132                 /  FROM LEVEL 0, SINCE IT CALLS SPARE WHICH IS TWO LEVELS DEEP
2133                 /
2134 1503 43400000 SECTR    CC = EOCF                  / END-OF-CYLINDER?
2135 1504 66001530          CA : DECS2                  / YES, DO AUTO SEEK IF ALLOWED
2136 1505 42540000          CC = NWTRF           ,RS    / NO, DID WE SWITCH TRACKS?
2137                                                    /   (NOTE:  EOCF ==> NWTRF)
2138 1506 72000000          RT : 0                      / NO, RETURN.
2139 1507 07603777          DO : NWTRK  ←   FALSE,U     / YES, CLEAR THE NEW TRACK FLAG
2140 1510 43100000          CC = INITF                  / SECTR CALLED BY INIT, WFS, RFS?
2141 1511 64001717          BR : INCS                   / YES, SET SCTR 0, SKIP VERIFY
2142                                                    /   (SECTOR ADDRESS IS ALREADY
2143                                                    /   HIGHEST NUMBERED SECTOR IF
2144                                                    /   WE'RE HERE, SO "INCS" WILL
2145                                                    /   SET TO 0, AS WE WANT)
2146 1512 64001711          BR : STRT3                  / OTHERWISE VERIFY ONE SECTOR
2147                                                    /   AND ACCESS SPARE IF REQUIRED
```

BASIC INCHS SUB-ROUTINE

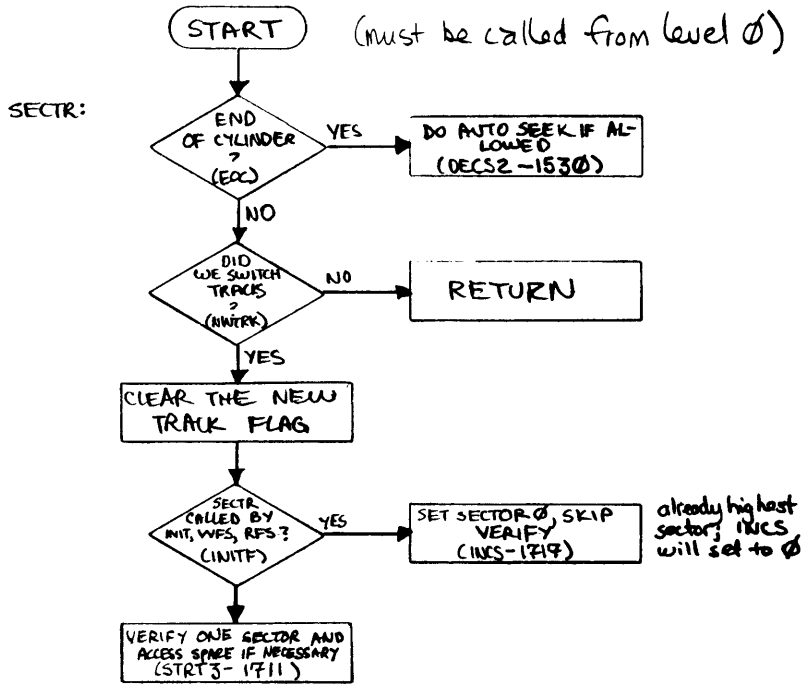


Note: the next page contains the detailed flowchart derived strictly from the μcode

INCHS, SECTR (SUBROUTINES)

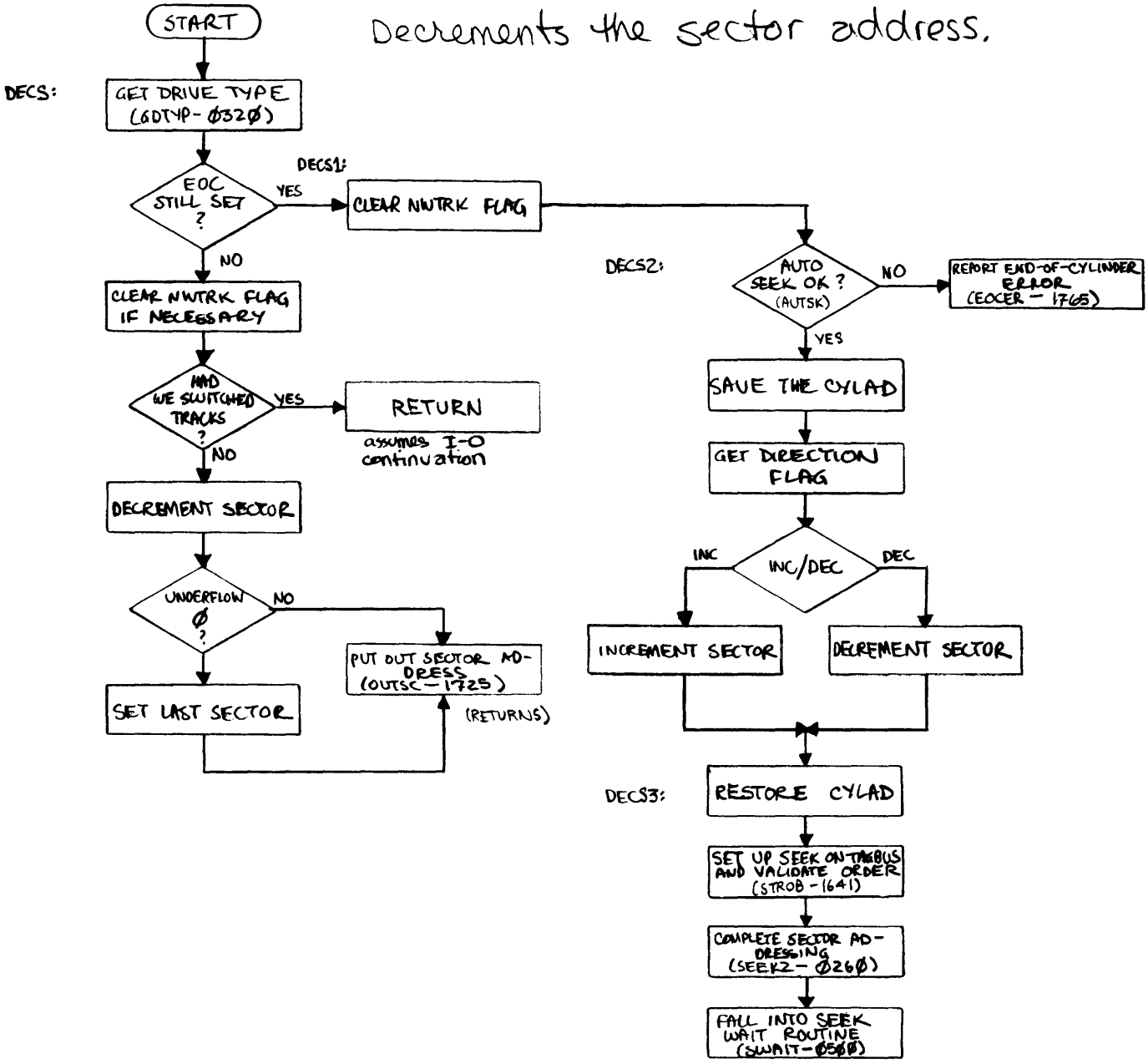


Head and sector is incremented, taking into account the mode the controller is in (cylinder or surface).



DECS, DECS2 SUBROUTINES

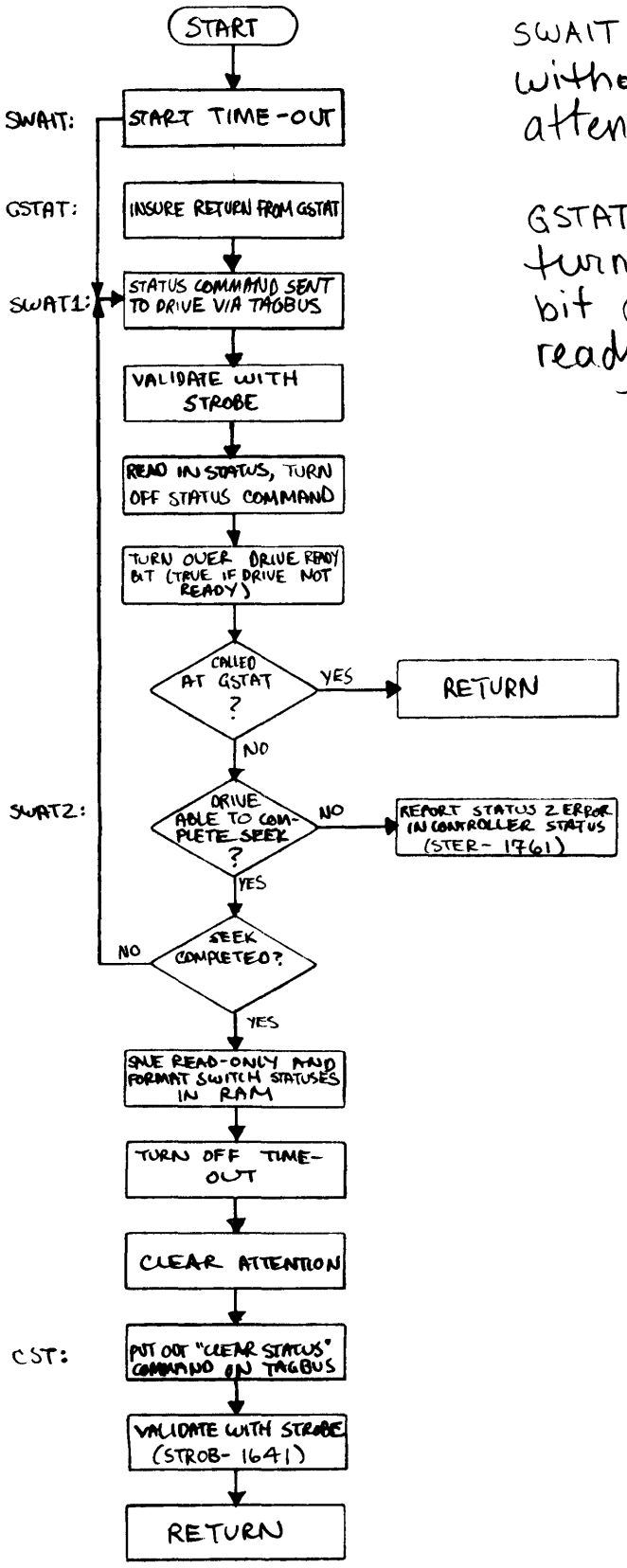
Decrements the sector address.



```
2148                          SUBROUTINES:  DECS, DECS2
2149                  /
2150                  /
2151                  /
2152                  /
2153                  /  DECS DECREMENTS THE SECTOR ADDRESS   FOR FULLER DESCRIPTION,
2154                  /  SEE COMMENTS UNDER "INCREMENT HEAD-SECTOR"
2155                  /
2156 1513 66000320 DECS      CA : GDTYP                    / GET DRIVE TYPE FOR OUTSC, SEEK2.
2157 1514 43400000           CC = EOCF                     / END-OF-CYLINDER STILL SET?
2158 1515 64001527           BR : DECS1                    / YES, ASSUME I-O CONTINUATION.
2159 1516 42500000           CC = NWTRF                    / NO, HAVE WE JUST SWITCHED TRACKS?
2160 1517 07603777           DO : NWTRK  ←   FALSE,U       / YES, CLEAR THE NEW TRACK FLAG
2161 1520 72000000           RT : 0                        /   AND ASSUME AN I-O CONTINUATION.
2162 1521 30124070         HSAD =        DEC  HSAD ,L      / NO, JUST DECREMENT
2163 1522 44100000           CC = LOVER                    / UNDERFLOW SECTOR 0?
2164 1523 64001725           BR : OUTSC                    / NO, DON'T RESET SECTOR FIELD
2165 1524 35236060         BUF3 =        CMP  BUF2 ,L      / YES, SET LAST SECTOR
2166 1525 22325401         HSAD = 1      PLUS BUF3 ,L
2167 1526 64001725           BR : OUTSC                    /      .AND GIVE IT AWAY
2168                  /
2169 1527 07603777 DECS1     DO : NWTRK  ←   FALSE,U       / CLEAR THE NEW TRACK FLAG
2170                                                       /   AND FALL INTO DECS2.
2171                  /
2172                  /
2173                  /  SUBROUTINE DECS2 CHECKS WHETHER AUTO TRACK SWITCHING IS
2174                  /  ALLOWED, AND IF SO, WHICH DIRECTION.  IT THEN PERFORMS THE
2175                  /  INDICATED SEEK AND WAITS FOR COMPLETION BEFORE RETURNING.
2176                  /
2177 1530 43740000 DECS2     CC = AUTSK            ,RS     / AUTO INCR-DECR SEEK OK?
2178 1531 64001765           BR : EOCER                    / NO, END-OF-CYLINDER ERROR
2179 1532 36503260         BUF1 =        PASS CYLAD        / YES, PUT CYLAD IN -A- REGISTER
2180 1533 10000456           DI : BUF3   ←   SKDIR,U       / GET DIRECTION FLAG (BIT 14)
2181 1534 27403500        DUMMY = 100    AND  BUF3 ,U      / ISOLATE IT
2182 1535 44440000           CC = TNZRO            ,RS     / INCREMENT OR DECREMENT?
2183 1536 30102264         BUF1 =        DEC  BUF1         / ASSUME DECREMENT
2184 1537 64001542           BR : DECS3                    / IF TRUE, THIS WILL SUCCEED
2185 1540 33742264         BUF1 =        INC  BUF1         / NO, INCREMENT WANTED, MUST
2186 1541 33742264         BUF1 =        INC  BUF1         /   INC TWICE TO WIPE OUT DEC
2187 1542 37614264 DECS3 CYLAD =        PASS BUF1         / RESTORE CYLAD
2188 1543 15201311           DO : CBUF   ←   CYLAD,C      / MUST DUPLICATE 3 INSTRUCTIONS
2189 1544 07624007           DO : TGBUS  ←   SEEKC,L      /   FROM SEEK1 TO AVOID 4-LEVEL
2190 1545 66001641           CA : STROB                    /   SUBROUTINE NESTING.  SEEK HERE
2191 1546 66000260           CA : SEEK2                    / FINISH ADDRESSING THE SECTOR.
2192                                                       / FALL INTO SWAIT TO WAIT FOR SEEK
2193                                                       /   COMPLETION.
```

```
2194                          SUBROUTINES:  SWAIT, GSTAT, SWAT3, CST
2195                  /
2196                  /
2197                  /    SUBROUTINE SWAIT WAITS FOR A SEEK TO COMPLETE SO THAT THE
2198                  /  CONTROLLER CAN ISSUE ANOTHER COMMAND TO THE DRIVE.  AT COMPLETION,
2199                  /  IT SAVES THE STATUS OF THE READ-ONLY SWITCH (BIT 6) AND THE FORMAT
2200                  /  SWITCH (BIT 5) FOR THE WRITE ROUTINES TO EXAMINE, AND CLEARS THE
2201                  /  ATTENTION BIT   THE ENTRY AT SWAT3 ALLOWS OTHER ROUTINES TO CLEAR
2202                  /  THE DRIVE'S ATTENTION BIT
2203                  /
2204                  /    SUBROUTINE GSTAT GETS STATUS FROM THE DRIVE AND TURNS OVER
2205                  /  THE DRIVE READY BIT SO IT IS TRUE IF THE DRIVE IS NOT READY
2206                  /    SWAIT AND GSTAT ARE AT THE THIRD LEVEL SINCE THEY ARE CALLED
2207                  /  FROM "SPARE" WHICH IS CALLED FROM "SECTR"   GSTAT FIRST SETS THE
2208                  /  CCB FALSE TO INSURE THAT A CALL TO GSTAT WILL RETURN IMMEDIATELY
2209                  /  AFTER FETCHING STATUS
2210                  /
2211 1547 07600500 SWAIT    DO : TIMER  ←   START,U    / TURN ON TIME-OUT CIRCUIT
2212 1550 64001552          BR : SWAT1                /   (ONLY FOR SWAIT)
2213 1551 44700000 GSTAT    CC = FALSE                / INSURE RETURN FROM GSTAT
2214 1552 07624015 SWAT1    DO : TGBUS  ←   STATC,L   / SEND STATUS COMMAND TO DRIVE.
2215 1553 34000000          NO :                      / MUST INSERT PROP DELAY TIME
2216 1554 34000000          NO :                      /   HERE -- SWAIT IS TOO DEEP
2217                                                  /   TO CALL STRB1, ALSO THE CC
2218                                                  /   BIT MAY BE FALSE (GSTAT)
2219 1555 07604477          DO : INTCW  ←   STRB ,U   / VALIDATE THE STATUS COMMAND
2220 1556 34000000          NO :                      / ALLOW 1 USEC FOR STATUS SET-UP
2221 1557 34000000          NO :
2222 1560 34000000          NO :
2223 1561 34000000          NO :
2224 1562 10002202          DI : BUF2   ←   CBSIN     / READ IN STATUS
2225 1563 07604437          DO : INTCW  ←   CSTRB,U   /   AND TURN OFF COMMAND
2226 1564 26230002        BUF2 = 2      XOR  BUF2 ,L  / TURN OVER DRIVE READY
2227                                                  /   (READY _ NOT READY)
2228 1565 35210260        BUF2 =        CMP  BUF2     /   AND THEN THE WHOLE THING.
2229 1566 64001570          BR : SWAT2                / IF SWAIT, DON'T RETURN YET
2230 1567 72000000          RT : 0                    / IF GSTAT, THIS WILL SUCCEED
2231 1570 27422026 SWAT2 DUMMY = 26     AND  BUF2 ,L  / CHECK IF DRIVE IS
2232 1571 44400000          CC = TNZRO                /   ABLE TO COMPLETE SEEK.
2233 1572 64001761          BR : STER                 / NO, DRIVE NRDY, SK CHK OR FAULT
2234 1573 27422001       DUMMY = 1      AND  BUF2 ,L  / YES, IS ACCESS READY
2235 1574 44400000          CC = TNZRO                /   (SEEK COMPLETED)?
2236 1575 64001552          BR : SWAT1                / NO, WAIT UNTIL IT IS.
2237 1576 27520140        REGO = 140    AND  BUF2 ,L  / YES, ISOLATE READ-ONLY
2238 1577 37720120        REGO =        PASS REGO ,L,SR /   AND FORMAT SWITCH STATUSES
2239 1600 37720120        REGO =        PASS REGO ,L,SR /   AND SAVE THEM IN RAM.
2240 1601 37720120        REGO =        PASS REGO ,L,SR
2241 1602 07620013          DO : RAMAD  ←   RDONL,L
2242 1603 17620041          DO : RAM    ←   REGO ,L
2243 1604 07600600 SWAT3    DO : TIMER  ←   STOP ,U   / TURN OFF TIME-OUT CIRCUIT
2244 1605 07621376          DO : CBUF   ←   CATN ,L   / THEN CLEAR ATTENTION TO AVOID
2245                                                  /   2ND INTERRUPT   FALL INTO CST
2246                  /
2247                  /
2248                  /  CST CLEARS DRIVE ATTENTION AND-OR FIRST STATUS BIT   IT ASSUMES
2249                  /  THE APPROPRIATE CLEAR BIT(S) ARE IN CBUF ON ENTRY
2250                  /
2251 1606 07624001 CST      DO : TGBUS  ←   CLST ,L   / PUT OUT CLEAR STATUS COMMAND
2252 1607 64001641          BR : STROB                / VALIDATE IT AND RETURN
```

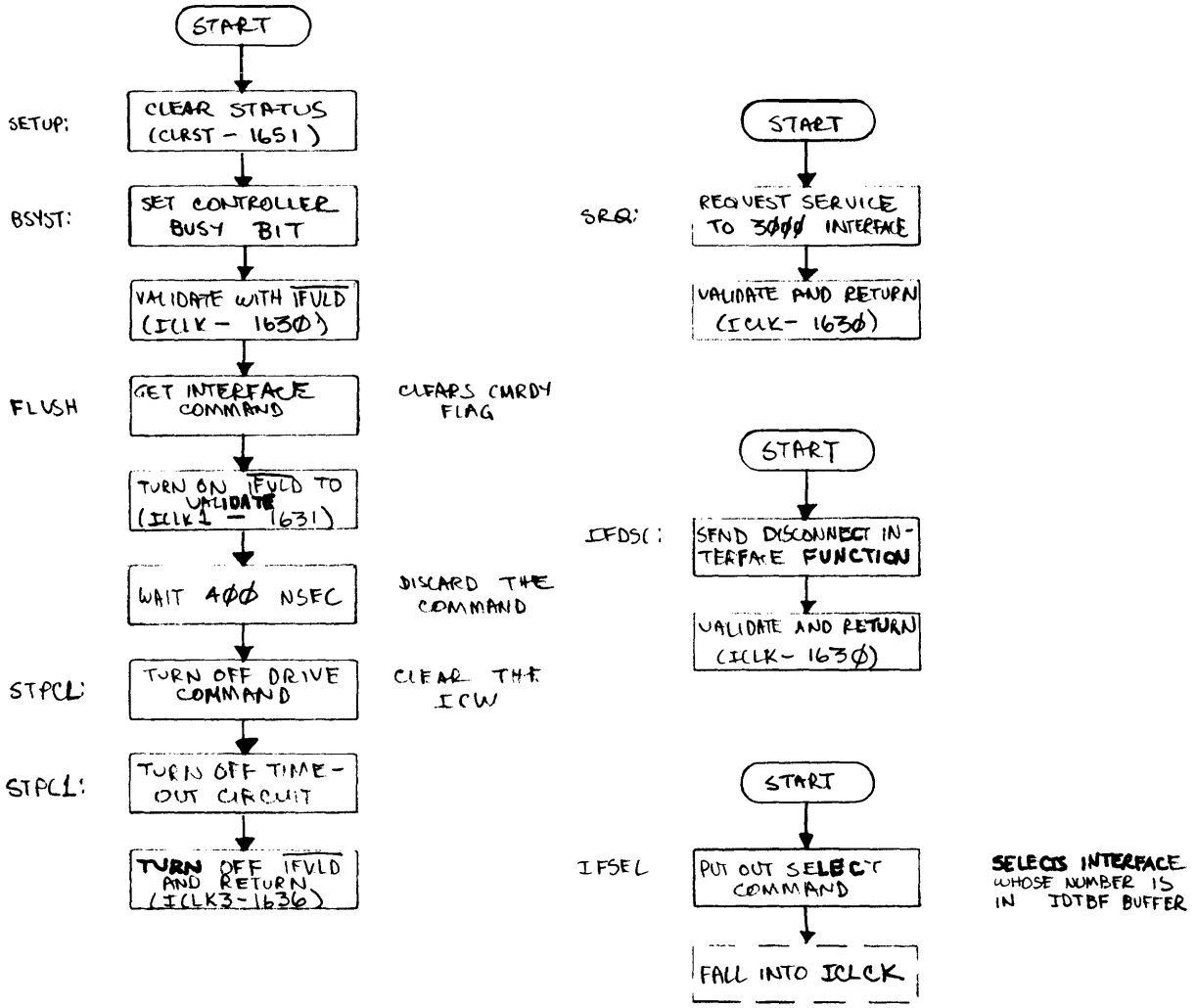
SWAIT, GSTAT, SWAT3, CST



SWAIT waits for SEEK completion without subsequent polling; the attention bit is cleared.

GSTAT gets drive status and turns over the "drive ready" bit (true if the drive is not ready).

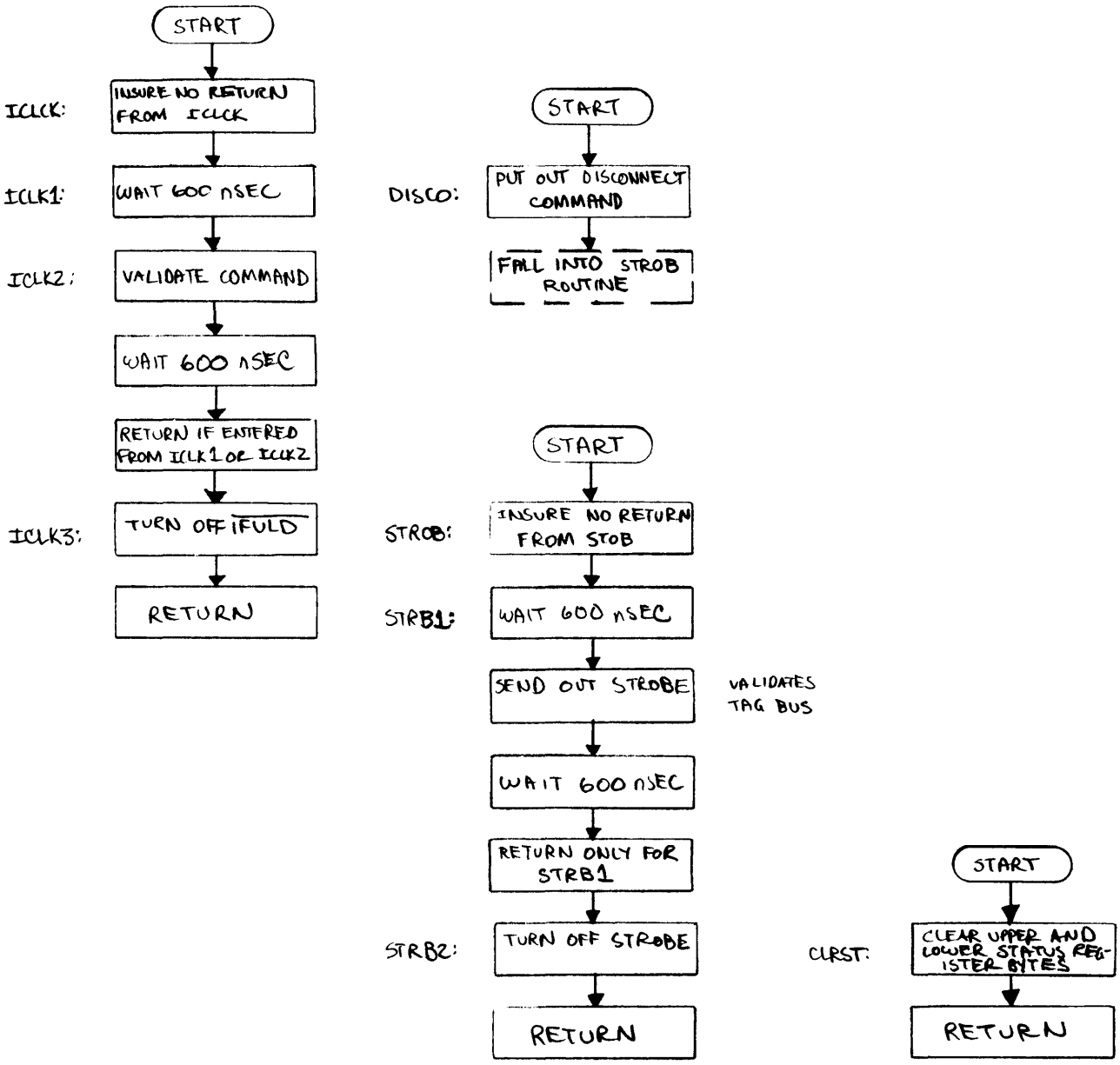
SETUP, BSYST, FLUSH, STPCL, SRQ, IFDSC, IFSEL SUBROUTINES



```
2253                          SUBROUTINES:  SETUP, BSYST, FLUSH, STPCL, SRQ, IFDSC, IFSEL
2254                  /
2255                  /
2256                  /
2257                  /
2258                  /  SUBROUTINE BSYST SETS THE CONTROLLER BUSY BIT ON THE CURRENT
2259                  /  INTERFACE, THEN CLEARS THE CURRENT COMMAND FROM THE INTERFACE.
2260                  /  THE SEPARATE ENTRY POINT AT FLUSH CLEARS THE COMMAND WITHOUT
2261                  /  SETTING THE CONTROLLER BUSY BIT (REQUIRED FOR UNIT UNAVAILABLE
2262                  /  AND ILLEGAL OPCODE ERRORS)   CLEARING THE COMMAND HERE ALLOWS
2263                  /  THE CONTROLLER TO REPEATEDLY ACCESS COMMANDS ON THE INTERFACE.
2264                  /  BSYST IS ONLY CALLED WHEN ALL PERTINENT COMMAND INFORMATION HAS
2265                  /  BEEN TRANSFERRED TO THE CONTROLLER AND IT IS ABLE TO BEGIN
2266                  /  EXECUTION.  THE ENTRY POINT AT SETUP CLEARS THE CONTROLLER STATUS
2267                  /  REGISTER FIRST   SUBROUTINE STPCL (STOP CLOCKS) IS SEPARATED FROM
2268                  /  TRHOF SO THAT THE POLL LOOP CAN CALL IT WITHOUT UPDATING THE 3000
2269                  /  TIO REGISTER.  PLACING STPCL HERE ELIMINATES ONE BRANCH TO ICLK3
2270                  /  THE FIRST TWO INSTRUCTIONS ARE IRRELEVANT IF WE FALL IN FROM FLUSH.
2271                  /
2272 1610 66001651 SETUP    CA : CLRST
2273 1611 07621400 BSYST    DO : IDTBF  ←   STBSY,L     / SET THE CONTROLLER BUSY BIT
2274 1612 07622441          DO : IFNBF  ←   BUSY ,L
2275 1613 66001630          CA : ICLCK
2276 1614 07622622 FLUSH    DO : IFNBF  ←   IFCTC,L     / FETCH COMMAND AND DISCARD IT
2277 1615 66001631          CA : ICLK1                  /   (CLEARS I'FC COMMAND BUFFER)
2278 1616 10001744          DI : DUMMY  ←   IDTBF
2279 1617 10001744          DI : DUMMY  ←   IDTBF       / (400 NSEC CLOCK PULSE)
2280 1620 07604437 STPCL    DO : INTCW  ←   CLICW,U     / TURN OFF THE DRIVE COMMAND
2281 1621 07600600 STPC1    DO : TIMER  ←   STOP ,U     / TURN OFF TIME-OUT CIRCUIT
2282 1622 64001636          BR : ICLK3                  / TURN OFF INTERFACE FUNCTION
2283                  /
2284                  /
2285                  /  SUBROUTINE SRQ FORCES A SERVICE REQUEST TO THE 3000 I-O
2286                  /  CHANNEL AFTER EVERY TRANSFER OF CONTROL INFORMATION OTHER THAN
2287                  /  THE COMMAND WORD, AND AFTER EVERY DATA TRANSFER.
2288                  /
2289 1623 07622670 SRQ      DO : IFNBF  ←   RQSRV,L
2290 1624 64001630          BR : ICLCK
2291                  /
2292                  /
2293                  /  SUBROUTINE IFDSC DISCONNECTS ALL CPU INTERFACES.
2294                  /
2295 1625 07622666 IFDSC    DO : IFNBF  ←   DSCIF,L     / SEND "DISCONNECT INTERFACE" FUNCTION
2296 1626 64001630          BR : ICLCK
2297                  /
2298                  /
2299                  /  SUBROUTINE IFSEL SELECTS THE INTERFACE WHOSE NUMBER IS IN IDTBF
2300                  /
2301 1627 07622454 IFSEL    DO : IFNBF  ←   SELIF,L     / PUT OUT SELECT COMMAND
2302                                                     /   AND FALL INTO IFCLK.
```

```
2303                          SUBROUTINES:  ICLCK, DISCO, STROB, CLRST
2304                  /
2305                  /
2306                  /  SUBROUTINE ICLCK SENDS A 600 NSEC CLOCK (IFVLD) TO THE INTERFACE TO
2307                  /  VALIDATE THE COMMAND IN IFNBF   THE LEADING EDGE OF THE CLOCK
2308                  /  IS ALSO DELAYED 600 NSEC TO ALLOW THE CONTENTS OF IFNBF TO
2309                  /  PROPAGATE DOWN THE CABLE.  ENTERING AT ICLK1 INSERTS ALL OF
2310                  /  THE ABOVE DELAYS BUT TRANSMITS ONLY THE LEADING EDGE OF IFVLD.
2311                  /  THIS FEATURE IS USED BY THE DATA TRANSFER COMMANDS AND BY THE
2312                  /  GET, PUT, AND FLUSH ROUTINES   THE ENTRY AT ICLK3 SIMPLY TURNS
2313                  /  OFF IFVLD.
2314                  /
2315 1630 44700000 ICLCK     CC = FALSE                    / INSURE NO RETURN FROM ICLK1.
2316 1631 34000000 ICLK1     NO :                          / ALLOW 600 NSEC PROP TIME.
2317 1632 34000000           NO :
2318 1633 07606000 ICLK2     DO : IFVLD  ←   SETCL,U       / VALIDATE THE COMMAND ON IFNBF
2319 1634 34000000           NO :                          / LEAVE IT ON FOR 600 NSEC.
2320 1635 72000000           RT : 0                        / THIS SUCCEEDS FOR ICLK1 OR ICLK2.
2321                  /
2322 1636 07606001 ICLK3     DO : IFVLD  ←   CLRCL,U       / DISABLE THE IFNBF COMMAND
2323 1637 72000000           RT : 0                        /   AND RETURN.
2324                  /
2325                  /
2326                  /  SUBROUTINE DISCO DISCONNECTS A DRIVE AT THE END OF AN OPERATION
2327                  /
2328 1640 07624013 DISCO     DO : TGBUS  ←   DCCOM,L       / PUT OUT DISCONNECT COMMAND
2329                                                       /   AND FALL INTO STROB.
2330                  /
2331                  /
2332                  /  SUBROUTINE STROB OPERATES SIMILARLY TO ICLCK, WITH CORRESPONDING
2333                  /  ENTRY POINTS, BUT VALIDATES THE TAG BUS COMMAND TO THE DISC
2334                  /
2335 1641 44700000 STROB     CC = FALSE                    / INSURE NO RETURN FROM STRB1.
2336 1642 34000000 STRB1     NO :                          / ALLOW 600 NSEC PROP TIME.
2337 1643 34000000           NO :
2338 1644 07604477           DO : INTCW  ←   STRB ,U       / VALIDATE THE TAG BUS COMMAND
2339 1645 34000000           NO :                          / LEAVE THERE FOR 600 NSEC
2340 1646 72000000           RT : 0                        / THIS SUCCEEDS ONLY FOR STRB1.
2341                  /
2342 1647 07604437 STRB2     DO : INTCW  ←   CSTRB,U       / DISABLE THE TAG BUS COMMAND
2343 1650 72000000           RT : 0                        /   AND RETURN.
2344                  /
2345                  /
2346                  /  SUBROUTINE CLRST CLEARS STATUS FOR ALL COMMANDS BUT
2347                  /  STATUS REQUEST
2348                  /
2349 1651 27612000 CLRST STATR = 0     PASS       ,U      / CLEAR UPPER BYTE.
2350 1652 27632000       STATR = 0     PASS       ,L      / CLEAR LOWER BYTE.
2351 1653 72000000           RT : 0
```

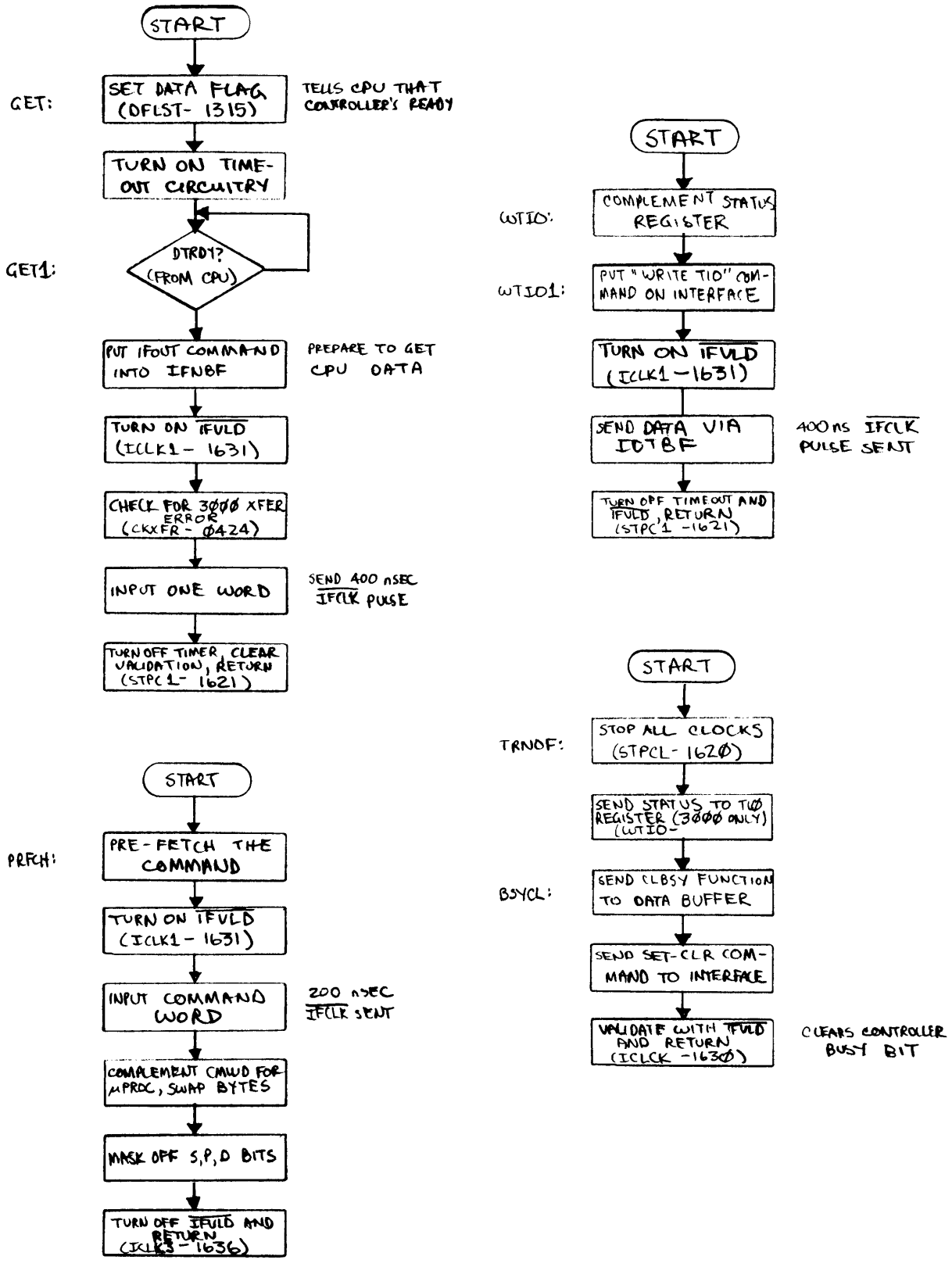
ICLCK, DISCO, STROB, CLRST SUBROUTINES



ICLCK sends $\overline{\text{IFVLD}}$ pulse to validate IFN bus contents.

STROB uses the $\overline{\text{STROBE}}$ line to validate the tagbus Colong with any corresponding CBUS data.

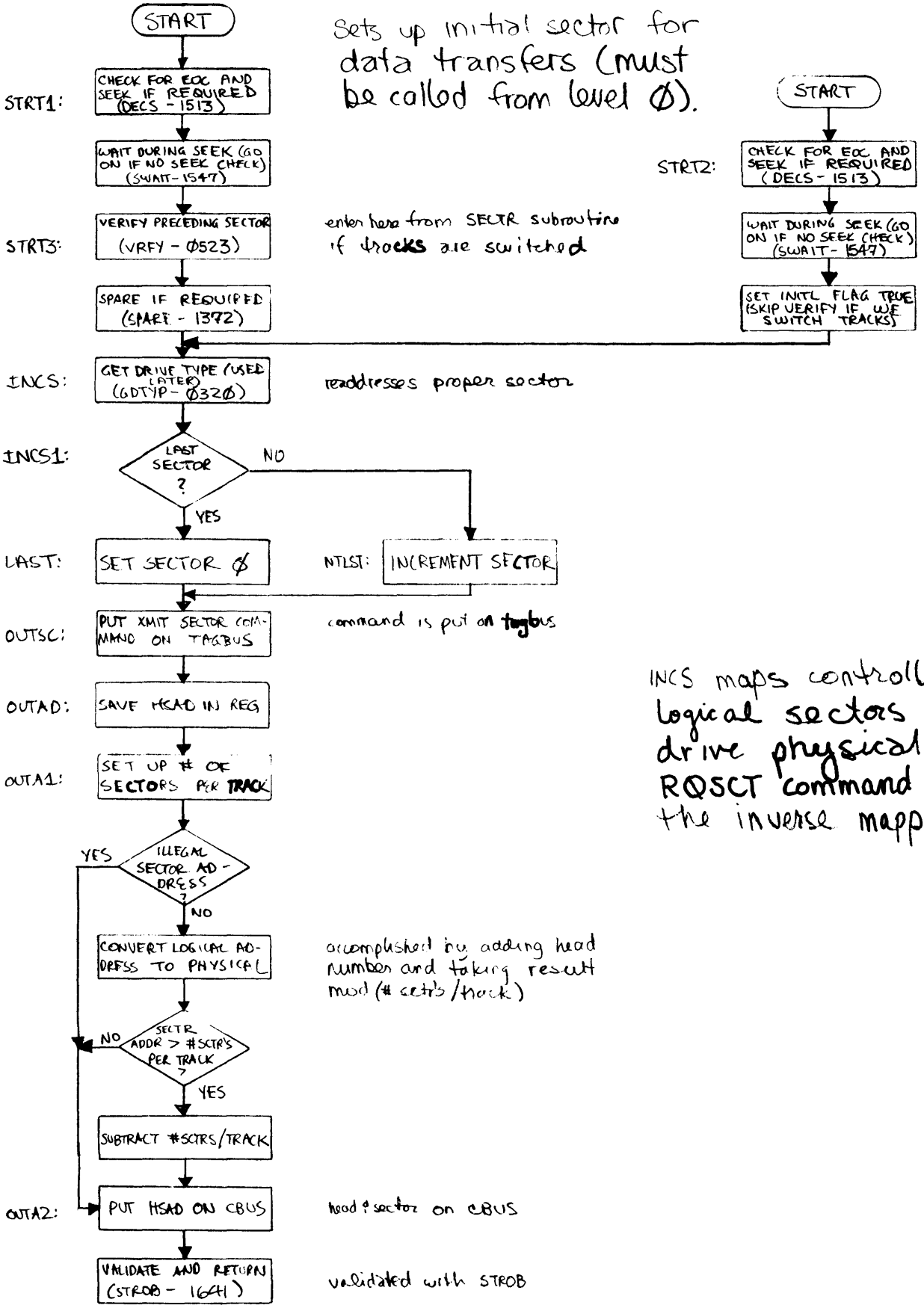
GET, PRFCH, WTIO, TRNOF, BSYCL SUBROUTINES



```
2352                          SUBROUTINES:  GET, PRFCH, WTIO, TRNOF, BSYCL
2353                 /
2354                 /
2355                 /
2356                 /
2357                 /  SUBROUTINE GET READS ONE WORD FROM THE INTERFACE AND RETURNS IT
2358                 /  IN BUF1.  GET IS A SECOND-LEVEL SUBROUTINE.
2359                 /
2360 1654 66001315 GET      CA : DFLST                    / TELL CPU WE'RE READY.
2361 1655 07600500          DO : TIMER  ←   START,U      / TURN ON TIME-OUT CIRCUIT.
2362 1656 42140000 GET1     CC = DTRDY           ,RS     / WAIT FOR TRANSFER
2363 1657 64001656          BR : GET1                    /   OR TIME-OUT INTERRUPT.
2364 1660 07622624          DO : IFNBF  ←   IFOUT,L      / CAN'T CALL DSTR1 -- TOO DEEP
2365 1661 66001631          CA : ICLK1                   / BUT WE CAN CALL ICLK1.
2366 1662 66000424          CA : CKXFR                   / CHECK FOR 3000 CHANNEL ERROR.
2367 1663 10101744          DI : BUF1   ←   IDTBF        / INPUT ONE WORD
2368 1664 10101744          DI : BUF1   ←   IDTBF        /   (400 NSEC CLOCK PULSE)
2369 1665 64001621          BR : STPC1                   / TURN OFF TIMER, CLEAR VALIDATION.
2370                 /
2371                 /
2372                 /  SUBROUTINE PRFCH PRE-FETCHES THE NEXT COMMAND FROM THE INTER-
2373                 /  FACE, THAT IS, IT OBTAINS THE COMMAND BUT DOES NOT TELL THE
2374                 /  INTERFACE ABOUT IT   THIS ALLOWS COMMANDS TO BE ACCESSED
2375                 /  REPEATEDLY IN CASE THE DESIRED DRIVE IS NOT AVAILABLE.  ALL
2376                 /  COMMANDS ARE EVENTUALLY CLEARED VIA A CALL TO SUBROUTINE FLUSH
2377                 /  OR BSYST
2378                 /
2379 1666 07622635 PRFCH    DO : IFNBF  ←   IFPRF,L      / PRE-FETCH THE COMMAND (ENABLES
2380 1667 66001631          CA : ICLK1                   /   INTERFACE DRIVERS, BUT
2381 1670 10101754          DI : COMWD  ←   IDTBF        /   FUNCTION IS NOT ASSIGNED)
2382 1671 34010214       COMAD =        CMP  COMWD,SW   / COMPLEMENT COMMAND, EXCHANGE BYTES
2383 1672 27430037       COMAD = 37     AND  COMAD,L    / MASK OFF S, P, AND D BITS.
2384 1673 64001636          BR : ICLK3                   / TURN OFF IFVLD, RETURN.
2385                 /
2386                 /
2387                 /  SUBROUTINE WTIO WRITES THE CONTROLLER STATUS REGISTER (STATR)
2388                 /  TO THE 3000 TIO REGISTER.
2389                 /
2390 1674 35302660 WTIO   BUF1 =        CMP  STATR
2391 1675 07622445 WTIO1    DO : IFNBF  ←   WRTIO,L      / SEND "WRITE TIO" TO INTERFACE.
2392 1676 66001631          CA : ICLK1                   / VALIDATE THE INTERFACE COMMAND
2393 1677 17600745          DO : IDTBF  ←   BUF1         / NOW SEND THE DATA WORD
2394 1700 17600745          DO : IDTBF  ←   BUF1         /   (400 NSEC IFCLK PULSE)
2395 1701 64001621          BR : STPC1                   / TURN OFF TIME-OUT AND IFVLD
2396                 /
2397                 /
2398                 /  SUBROUTINE TRNOF DOES A LOT OF THE BUSY WORK OF SHUTTING
2399                 /  THINGS DOWN AT THE END OF A CONTROLLER OPERATION.
2400                 /
2401 1702 66001620 TRNOF    CA : STPCL                   / STOP ALL THE CLOCKS
2402 1703 66001674          CA : WTIO                    / SEND STATUS TO 3000 TIO REGISTER.
2403 1704 07621401 BSYCL    DO : IDTBF  ←   CLBSY,L      / SEND CLBSY FUNCTION TO DATA BUFFER.
2404 1705 07622441          DO : IFNBF  ←   BUSY ,L      / SEND SET-CLR COMMAND TO INTERFACE.
2405 1706 64001630          BR : ICLCK                   / CLEAR THE CONTROLLER BUSY BIT
```

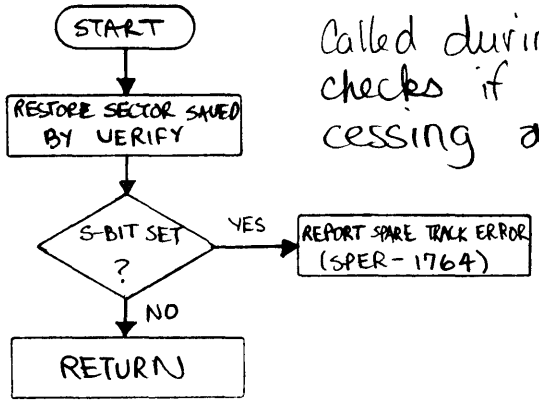
```
2406                          SUBROUTINES:  STRT1, STRT2, INCS
2407                  /
2408                  /
2409                  /
2410                  /
2411                  /  STRT1 AND STRT2 SET UP THE INITIAL SECTOR FOR DATA TRANSFER
2412                  /  OPERATIONS.  THEY MUST BE CALLED FROM LEVEL 0.  STRT1 IS CALLED IF
2413                  /  PREVIOUS SECTOR VERIFICATION AND-OR SPARE TRACK ACCESSING IS DONE
2414                  /  BEFORE DATA TRANSFER.  STRT2 SKIPS THIS PROCESS.  THE ENTRY AT
2415                  /  STRT3 IS USED BY THE SECTR SUBROUTINE WHENEVER WE SWITCH TRACKS
2416                  /  DURING A DATA TRANSFER.
2417                  /
2418 1707 66001513 STRT1     CA : DECS                    / CHECK FOR EOC, SEEK IF REQ'D
2419 1710 66001547           CA : SWAIT                   / MAKE SURE OF NO SEEK CHECK.
2420 1711 66000523 STRT3     CA : VRFY                    / VERIFY PRECEDING SECTOR.
2421 1712 66001372           CA : SPARE                   / ACCESS SPARE TRACK IF REQD
2422 1713 64001717           BR : INCS                    / RE-ADDRESS PROPER SECTOR.
2423                  /
2424 1714 66001513 STRT2     CA : DECS                    / CHECK FOR EOC, SEEK IF REQ'D
2425 1715 66001547           CA : SWAIT                   / MAKE SURE OF NO SEEK CHECK.
2426 1716 07623000           DO : INITL  ←    TRUE, L     / SKIP VERIFY IF WE SWITCH TRACKS.
2427                                                       / FALL INTO INCS.
2428                  /
2429                  /
2430                  /  SUBROUTINE INCS INCREMENTS THE SECTOR ADDRESS WITHOUT CHANGING
2431                  /  THE HEAD OR CYLINDER ADDRESSES.  THE VARIOUS OTHER ENTRY POINTS
2432                  /  (NTLST, OUTSC, OUTAD, OUTA1) ARE USED BY OTHER ROUTINES TO
2433                  /  TRANSMIT SECTOR ADDRESSES TO THE DRIVE.  THE MAPPING FROM
2434                  /  CONTROLLER LOGICAL TO DRIVE PHYSICAL SECTOR ADDRESSES OCCURS
2435                  /  HERE ONLY.  (THE INVERSE MAPPING FOR THE RDSCT COMMAND IS DONE IN
2436                  /  THAT COMMAND PROCESSOR)
2437                  /
2438 1717 66000320 INCS      CA : GDTYP                   / GET DRIVE TYPE FOR LATER.
2439 1720 32222070 INCS1  DUMMY = HSAD  PLUS BUF2 ,L     / CHECK FOR LAST SECTOR.
2440 1721 44140000           CC = LOVER           ,RS
2441 1722 64001724           BR : NTLST
2442 1723 27724377 LAST    HSAD = 377   PASS      ,L     / YES, SET SECTOR 0.
2443 1724 33764070 NTLST   HSAD =       INC  HSAD ,L     / NO, JUST INCREMENT SECTOR.
2444 1725 07624003 OUTSC     DO : TGBUS  ←   XSECT,L     / PUT OUT SECTOR ADDRESS ONLY
2445 1726 37616270 OUTAD   BUF3 =       PASS HSAD        / INTO BUF3 FOR COMPATIBILITY
2446                                                       /   WITH SEEK2, SEEK3
2447 1727 22322377 OUTA1   BUF1 = 377   PLUS BUF2 ,L     / SET UP -(# SECTORS PER TRACK)
2448 1730 32223464        DUMMY = BUF1  PLUS BUF3 ,L     / CHECK FOR ILLEGAL
2449 1731 44100000           CC = LOVER                  /   SECTOR ADDRESS.
2450 1732 64001742           BR : OUTA2                  / YES, DON'T MODIFY IT
2451 1733 27501437         REGO = 37    AND  BUF3 ,U     / O.K., CONVERT LOGICAL ADDRESS
2452 1734 37700200         REGO =       PASS REGO ,SW    /   TO PHYSICAL ADDRESS BY ADDING
2453 1735 32237460         BUF3 = REGO  PLUS BUF3 ,L     /   HEAD ADDRESS AND TAKING THE
2454 1736 32223464        DUMMY = BUF1  PLUS BUF3 ,L     /   RESULT MOD (# SCTRS PER TRACK)
2455 1737 44140000           CC = LOVER           ,RS    / IS SCTR ADDR > # SCTRS PER TRACK?
2456 1740 64001742           BR : OUTA2                  / NO, SAFE TO SEND IT TO DRIVE.
2457 1741 32237464         BUF3 = BUF1  PLUS BUF3 ,L     / YES, SUBTRACT (# SCTRS PER TRACK)
2458 1742 15201715 OUTA2     DO : CBUF   ←   BUF3 ,C     / SHIP OUT HEAD-SECTOR TO DRIVE.
2459 1743 64001641           BR : STROB
```

STRT1, STRT2, and INCS SUBROUTINES

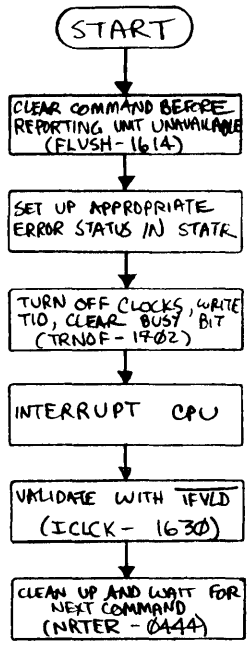


INCS maps controller logical sectors to drive physical (the RQSCT command does the inverse mapping)

SBTCK, USTAT, SUBROUTINES
CONTROLLER ERROR STATUS SIEVE



Called during disc address miscompares; checks if miscompare is due to accessing a spare track.



(send STINT on function bus)

STATUSES:

BSYER:	UNIT UNAVAILABLE	(27)
WPER:	WRITE ON PROT/DEF CYL	(26)
STER:	STATUS 2 ERROR	(23)
ACRER:	ACCESS READY ERROR	(22)
DEFER:	DEFECTIVE TRACK ERROR	(21)
SPER:	SPARE TRACK ERROR	(20)
EOCER:	END-OF-CYLINDER	(14)
IOPER:	IO PROG. ERROR (3000)	(12)
HSER1:	HEAD-SECTOR MISCOMPARE	(11)
CYLR1:	CYLINDER COMPARE ERROR	(07)
OPCER:	ILLEGAL OPCODE	(01)

```
2460                          SUBROUTINES:  SBTCK, USTAT, CONTROLLER ERROR STATUS SIEVE
2461                  /
2462                  /
2463                  /
2464                  /
2465                  /  SUBROUTINE SBTCK IS CALLED FOR DISC ADDRESS MISCOMPARES.  IT
2466                  /  CHECKS WHETHER THE MISCOMPARE IS DUE TO TRYING TO DIRECTLY
2467                  /  ADDRESS A SPARE TRACK (S-BIT SET)   IF SO, WE BRANCH DIRECTLY
2468                  /  TO SPER (SPARE TRACK ERROR), OTHERWISE WE RETURN.
2469                  /
2470 1744 37724064 SBTCK  HSAD =       PASS BUF1 ,L     / RESTORE SECTOR SAVED BY VRFY
2471 1745 27402600       DUMMY = 200   AND  STATR,U     / CHECK IF S-BIT SET
2472 1746 44400000          CC = TNZRO
2473 1747 64001764          BR : SPER                   / YES, REPORT SPARE TRACK ERROR.
2474 1750 72000000          RT : 0                      / NO, RETURN.
2475                  /
2476                  /
2477                  /  SUBROUTINE USTAT SETS THE CURRENT UNIT NUMBER (BUT NOT THE
2478                  /  HOLD BIT) IN THE LOWER BYTE OF STATR.  IT THEN CHECKS THE
2479                  /  USER-REQUESTED DRIVE NUMBER TO SEE THAT IT IS WITHIN THE LIMITS
2480                  /  OF THE CONTROLLER.  IF NOT, A "DRIVE UNAVAILABLE" ERROR RETURN
2481                  /  IS TAKEN.
2482                  /
2483 1751 34032074 USTAT STATR =       CMP  CONWD,L     / PUT UNIT # IN STATR,L.
2484 1752 27432417       STATR = 17    AND  STATR,L
2485 1753 22222765       DUMMY = MXDRV PLUS STATR,L     / MUST BE 10 OR LESS (OPERATING
2486 1754 44140000          CC = LOVER           ,RS    /   SYSTEM MAY IMPOSE A LESSER
2487                                                    /   MAXIMUM)
2488 1755 72000000          RT : 0                      / DRIVE NUMBER O.K., RETURN.
2489                                                    / NO_GOOD, FALL INTO BSYER
2490                  /
2491                  /  THIS SECTION SETS UP CONTROLLER ERROR STATUS IN STATR AND
2492                  /  REQUESTS AN INTERRUPT
2493                  /
2494 1756 66001614 BSYER    CA : FLUSH                  / CLR CMND BUFR BEFORE REPORTING
2495 1757 22212401       STATR = 1     PLUS STATR,U    /   UNIT UNAVAILABLE ERROR    (27)
2496 1760 22212403 WPER  STATR = 3     PLUS STATR,U    / WRITE ON PROT-DEF CYLINDER  (26)
2497 1761 22212401 STER  STATR = 1     PLUS STATR,U    / STATUS-2 ERROR              (23)
2498 1762 22212401 ACRER STATR = 1     PLUS STATR,U    / ACCESS READY ERROR          (22)
2499 1763 22212401 DEFER STATR = 1     PLUS STATR,U    / DEFECTIVE TRACK             (21)
2500 1764 22212404 SPER  STATR = 4     PLUS STATR,U    / SPARE TRACK                 (20)
2501 1765 22212402 EOCER STATR = 2     PLUS STATR,U    / END-OF-CYLINDER ERROR       (14)
2502 1766 22212401 IOPER STATR = 1     PLUS STATR,U    / I-O PROG ERROR (3000 ONLY)  (12)
2503 1767 22212402 HSER1 STATR = 2     PLUS STATR,U    / HEAD-SECTOR COMPARE ERROR   (11)
2504 1770 22212406 CYLR2 STATR = 6     PLUS STATR,U    / CYLINDER COMPARE ERROR      (07)
2505 1771 22212401 OPCER STATR = 1     PLUS STATR,U    / ILLEGAL OPCODE ERROR        (01)
2506 1772 66001702          CA : TRNOF                  / CLOCKS OFF, WRT TIO, CLEAR BUSY
2507 1773 07622677          DO : IFNBF  ←   STINT,L     / NOW INTERRUPT THE CPU.
2508 1774 66001630          CA : ICLCK
2509 1775 64000444          BR : WRTER                  / CLEAN UP, WAIT FOR NEXT COMMAND

                           ORG = 1777
     1777 06026505    CHECKSUM = 06026505

   0 ERRORS, LAST ADDRESS USED = 1775
```

APPENDIX I
MICROASSEMBLER INSTRUCTION DESCRIPTION

Described below is each type of instruction used by the 13037 firmware. These instructions are categorized as to type, and reference should be made to the instruction format of figure 1. The actual listing is organized as follows:

332	0001	17620405	CLHLD	DO : RAMAD ← COUNT,L	/
listing line number	*ROM address*	*microcode (octal)*	*label*	*microcode instruction*	*comment field*

ARITHMETIC INSTRUCTIONS

FORM:	TARGET REGISTER	=	REG	OPERATION	REG, BYTE, SHIFTER OPERATION
EXAMPLES:	HSAD	=	HSAD	AND	BUF3, U *(shifter defaults to PASS mode)*
	HSAD	=		PASS	REG0, SL *(second register is not needed so it is left unspecified; operation is full word so no byte need be specified; shifter will shift left one bit)*
	DUMMY	=	REG0	XOR	BUF3, L *(no target register; operation meant solely to update T register and process status register for subsequent indirect branch or conditional test)*
FORM:	TARGET REGISTER	=	IMMEDIATE OPERAND	OPERATION	BREG, BYTE, SHIFTER OPERATION
EXAMPLES:	COMWD	=	377	PASS	,L *(immediate operand from firmware written directly into lower byte of register COMWD)*
	DUMMY	=	351	PLUS	COMWD, L *(T register and process status register updated with masked bits of register COMWD; immediate operand always replaces an A register)*

I/O (INPUT/OUTPUT) INSTRUCTIONS

FORM:	DO	:	HARDWARE	←	REGISTER, BYTE, COMP
					(data output form; register can be replaced by an immediate operand)
EXAMPLES:	DO	:	INITL	←	FALSE, L
					(reset INITL flip-flop on the device controller; note that FALSE is a lower byte immediate operand)
	DO	:	RAM	←	IFCNO, L
					(RAM is updated with lower byte contents of register IFCNO)
	DO	:	IDTBF	←	BUF3, L, C
					(IBUS data buffer is updated with the complement of the lower byte of register BUF3)
FORM:	DO	:	HARDWARE	←	IMMEDIATE OPERAND, BYTE
EXAMPLES:	DO	:	TIMER	←	START, U
					(timer hardware receives the immediate operand pattern START over the upper byte of the MIO bus to enable the timer to count)
	DO	:	CBUF	←	CFST, L
					(control bus output buffer is updated with immediate operand pattern CFST over the lower MIO bus byte to cause the drive to clear first status)
FORM:	DI	:	REGISTER	←	HARDWARE, BYTE
					(no shifter field is available as this hardware is bypassed during all data input operations)
EXAMPLES:	DI	:	TSTTN	←	TIMER, U
					(timeout circuitry is monitored by inputting status via the MIO bus; register TSTTM is updated with these contents)

SET CC (CONDITIONAL) INSTRUCTIONS

FORM:	CC	=	CONDITION SELECT	, REVERSE SENSE
EXAMPLES:	CC	=	LOVER	
				(condition code bit is set with the state of the lower byte overflow bit of the process status register)
	CC	=	CMRDY	,RS
				(condition code bit is set with the complement of the state of the command ready flag from the interface)

BRANCH INSTRUCTIONS

FORM:	BR	:	ADDRESS	
EXAMPLES:	BR	:	ATTN3	*(branch to address labeled ATTN3; the actual address can be found in the right-most four digits of the microcode; as with all branches, its success depends on the condition of the CCB)*
	BR	:	I	*(a previous arithmetic instruction computes a twelve bit address used to replace the normal ROM address field for branching)*
FORM:	CA	:	ADDRESS	
EXAMPLES:	CA	:	TRNOF	*(a subroutine call is made to the address labeled TRNOF)*
	CA	:	I	*(a previous arithmetic instruction computes a twelve bit address used to replace the normal ROM address field for subroutine calls)*
FORM:	RT	:	O	*(this is the only form of a subroutine return)*

NOP INSTRUCTIONS

FORM:	NO	:	REGISTER	,BYTE
EXAMPLE:	NO	:	BUF3	,L *(register BUF3, lower byte, is complemented)*
FORM:	NO	:		
EXAMPLE:	NO	:		*(no operation is performed except to delay subsequent instruction execution by 200 nanoseconds)*

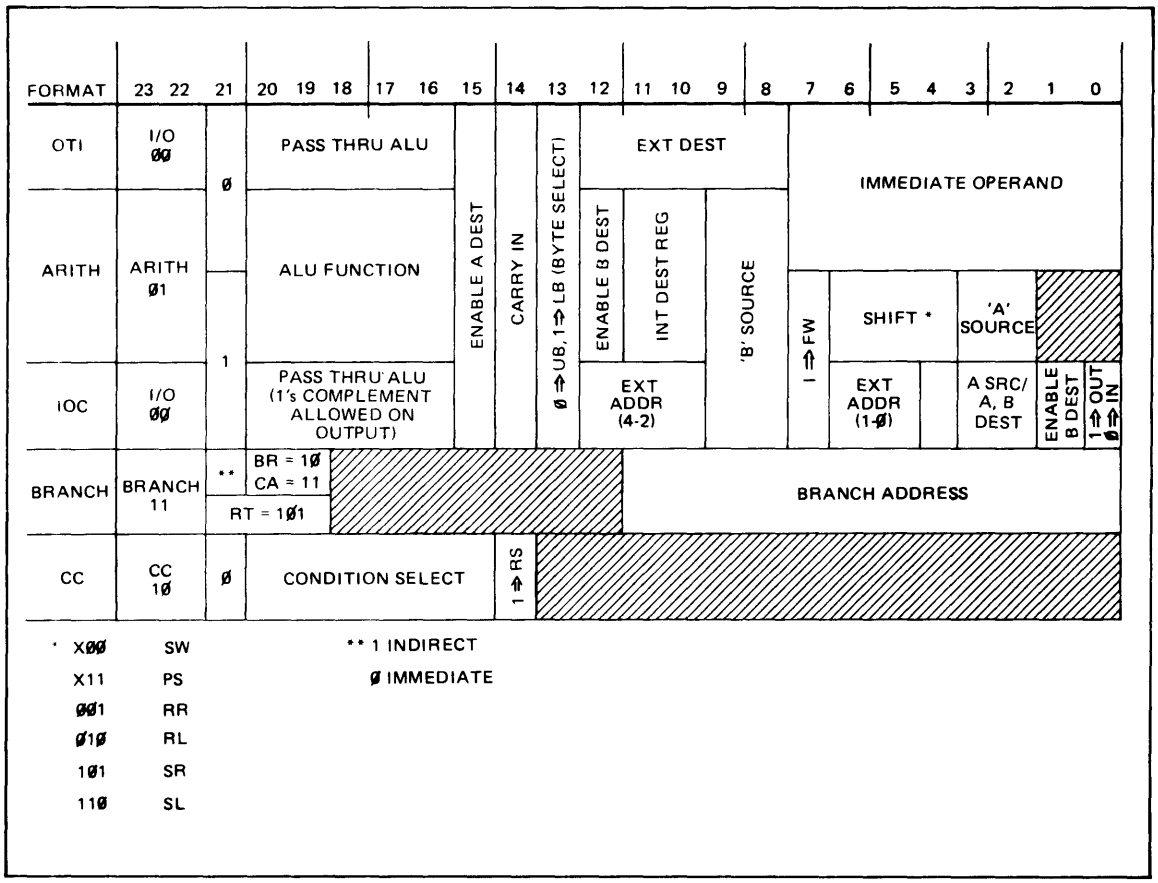


Figure 1. MICROCODE INSTRUCTION FORMAT

APPENDIX II
LABEL CALL ADDRESSES

ACMOD	(1200)	1130,1212
ACRER	(1762)	0542,0611,0626,0720,1050
ADJX	(1250)	1246
ATTN1	(0076)	0101
ATTN2	(0102)	0106
ATTN3	(0131)	0124
ATTN4	(0140)	0453
BOOT	(0215)	0164
BSYCL	(1704)	0041,1104
BSYER	(1756)	1755*
BSYST	(1611)	1106,1266,1341
CDER1	(1140)	1236
CDTER	(0435)	0434*
CKXFR	(0424)	0056,0121,0143,0266,1311,1662
CKWRT	(0775)	0644,1034
CLER	(1441)	1411
CLHLD	(0011)	0023
CLOOP	(1122)	1177
CLR	(1262)	0176
CLRAM	(0026)	0032
CLROF	(0454)	0445,0502
CLRST	(1651)	0044,0157,0313,0346,0426,1317,1610
CLR1	(0035)	0024
CMDWT	(0141)	0271,1105,1261
CMDW1	(0143)	0145
COMP1	(1171)	1167
COMP2	(1172)	1161
COMP3	(1230)	1225
CST	(1606)	0316
CVECT	(0164)	

(*) denotes a call to the corresponding label as a result of "falling through" the previous routine.

```
CYLER   (1441)   1411
CYLRT   (1457)   1442
CYLR1   (1443)   1436
CYLR2   (1770)   1460

DECS    (1513)   1707,1714
DECS1   (1527)   1515
DECS2   (1530)   1504
DECS3   (1542)   1537
DEFER   (1763)   1421,1427
DFLST   (1315)   0463,0505,1315,1654
DFTRK   (1420)   1403
DFTR1   (1430)   1424
DISCO   (1640)   0042,0141,1342
DRVOK   (1333)   1327
DSTRT   (0422)   0411,0473,0615
DSTR1   (0423)   0663,1006,1036
DTERR   (1360)   1374
DTER2   (1416)   1364
DVECT   (0343)

EOCER   (1765)   1531
EWRFS   (0770)   0637,1074
EWRF1   (0771)   0413,1010
EXEC    (0147)   0060,0146*
EXEC1   (0150)   0130
EXEC2   (0161)   0155

FLUSH   (1614)   0037,0156,1756

GDTYP   (0320)   0257,0362,0660,1367,1451,1461,1513,1717
GET     (1654)   0274,0276,0461,0510,1101
GET1    (1656)   0247,1657
GSTAT   (1551)   0304,0447,1351
GTPAT   (1205)   1173
```

(*) denotes a call to the corresponding label as a result of "falling through" the previous routine.

```
HSER    (1435)   1406
HSER1   (1767)   1440

ICLCK   (1630)   0231,0442,1256,1316,1613,1624,1626,1627*,1706,1774
ICLK1   (1631)   0423,1310,1615,1661,1667,1676
ICLK2   (1633)   0136
ICLK3   (1636)   1622,1673
IFDSC   (1625)   0001,0043,0061
IFSEL   (1627)   0055,0116
ILLGL   (0156)   0204,0205
INCHS   (1461)   0475,0515,0673,0771,1150
INCS    (1717)   1511,1713,1716*
INCS1   (1720)   1370
INIT    (0642)   0177
INIT1   (0662)   0654
INIT2   (0664)   0704
INIT3   (0665)   0701
INIT4   (0700)   0675
INTRP   (1257)   0214,1265
IOPER   (1766)   0427

LAST    (1723)
LTIO    (1100)   0207

MOREC   (1120)   1133
MOREP   (1162)   1175

NOERR   (0311)   0307
NRTER   (0444)   1775
NTEQL   (0021)   0016
NTLST   (1724)   1464,1722
NXTAD   (0001)   0000

OPCER   (1771)   0160
OUTAD   (1726)   1477,1502
```

(*) denotes a call to the corresponding label as a result of "falling through" the previous routine.

```
OUTA1   (1727)   0263
OUTA2   (1742)   1732,1740
OUTSC   (1725)   0661,1453,1523,1526
OVERR   (0436)   0606

PLOOP   (1152)   1121
POLL    (0037)   0036*,0211
POLL1   (0040)   0135,0240,0246
POLL2   (0044)   0067
POLL3   (0061)   1332
PRFCH   (1666)   0125,0147
PUT     (1304)   0303,0312,0370,1136,1141,1143,1145,1147,1206,1275
PUT1    (1305)   1306
PWRON   (0025)   0005

RBOOT   (0410)   0232
RCORD   (0272)   0242,0265
READ    (0407)   0171
READ1   (0411)   0415,0421
READ2   (0412)
READ3   (0530)   0430
RECAL   (0233)   0165
RECRD   (0264)   0200
REDE1   (0430)   0412,0474
RFDAT   (0627)   0630,0636
RFS     (0613)   0172
RFULL   (0616)   0641
RNVFY   (0416)   0206
ROFST   (0460)   0202
ROFS1   (0473)   0501
ROFS2   (0502)   0477
ROFS3   (0504)   0520,0667,0773
RQAD    (1266)   0210
RQAD1   (1271)   1137,1207,1267
RQAD2   (1275)   1273
RQAD3   (1303)   1301
```

(*) denotes a call to the corresponding label as a result of "falling through" the previous routine.

```
RQSCT   (0346)   0170
RQSC1   (0366)   0361
RQSC2   (0371)   0317,1151,1270
RQSC3   (0375)   0354,0655
RQSC4   (0400)   0404
RQSC5   (0372)   0373
RQSYN   (1106)   0201

SBTCK   (1744)   1437,1457
SECTR   (1503)   0414,0500,0521,0640,0702,1011,1075
SEEK    (0241)   0166
SEEK1   (0247)   0225,0243
SEEK2   (0260)   1546
SEEK3   (0261)   1452
SETUP   (1610)   0264,1100,1252,1262
SFMSK   (1252)   0203
SHFTX   (1244)   1242
SPARE   (1372)   1456,1712
SPAR1   (1447)   1434
SPER    (1764)   1747
SRQ     (1623)   0245,0270,0443,0462,1103
STATS   (0301)   0167
STER    (1761)   0252,0353,1000,1030,1572
STPCL   (1620)   0040,1702
STPC1   (1621)   1314,1665,1701
STRB1   (1642)   0063,0376,0617
STRB2   (1647)   0406
STROB   (1641)   0034,0236,0255,0457,0470,1264,1350,1450,1545,1607,
                 1640*,1743
STRT1   (1707)   0410,0472,0512,1003
STRT2   (1714)   0417,0614,0643,1033
STRT3   (1711)   1512
SURFC   (1501)   1470
SVRAM   (1340)   1336
SWAIT   (1547)   0234,0464,0471,0503,1454,1546*,1710,1715
SWAT1   (1552)   1550,1575
SWAT2   (1570)   1566
SWAT3   (1604)   0140,0444
```

(*) denotes a call to the corresponding label as a result of "falling through" the previous routine.

```
TERM    (0266)   0374,0506
TRNOF   (1702)   0132,0267,0440,1257,1702

UDTER   (0437)   1417
UNIT    (1317)   0212,0217,0233,0241,0407,0416,0460,0507,0613,0642,
                 1002,1032
UNIT1   (1341)   0301,0350
UNIT2   (1347)   0120
USTAT   (1751)   0314,0347,1751

VCHK    (0431)   0430*,0514
VCYLD   (0547)   0550
VDATA   (0557)   0560,0566
VDTA1   (0567)   0570
VERWD   (0577)   0600,0604
VHSAD   (0553)   0554
VLOOP   (0513)   0522
VRFCM   (0507)   0173
VRFY    (0523)   1711
VRFY1   (0527)   0513,1371
VRFY2   (0524)   1455
VRFY3   (0605)   0767,0770
VSYNC   (0543)   0544

WAKUP   (0212)   0211*
WCYLD   (0733)   0734
WDATA   (0741)   0742,0750
WDTA2   (0751)   0752
WFDAT   (1057)   1060,1066
WFS     (1032)   0175
WFSYN   (1051)   1052,1056
WFULL   (1037)   1077
WFWAT   (1067)   1070
WFWA2   (1072)   1073
WHSAD   (0736)   0737
WLOOP   (1234)   1251
WPER    (1760)   1023
```

(*) denotes a call to the corresponding label as a result of "falling through" the previous routine.

WRITE	(1002)	0174
WRLWD	(0765)	0766
WRONE	(0705)	0670,1007
WRTOK	(1007)	1013
WSTA1	(1014)	1004,1012
WSTA2	(1024)	0703,0775,1016,1023*,1076
WSYNC	(0721)	0722,0726
WSYN1	(0727)	0730
WTATN	(0447)	0452
WTEWD	(0757)	0760,0764
WTIO	(1674)	0237,0244,1703
WTIO1	(1675)	1102

(*) denotes a call to the corresponding label as a result of "falling through" the previous routine.

CONTENTS

		Page
1.0	INTRODUCTION	9-1
2.0	MULTIPLE CPU DISC DRIVE OPERATION	9-1
3.0	THE FILE MASK	9-3
4.0	SPARE TRACKS AND THE 13037	9-6
	4.1 Why Spare Tracks?	9-6
	4.2 How to Generate a Spare Track	9-7
	4.3 How a Spare Track is Accessed	9-9
	4.4 Directly Accessing a Spare Track	9-12
5.0	AUTOMATIC HEAD AND/OR TRACK SWITCHING	9-12
6.0	SOME ROUTINE OVERVIEWS	9-14

MAJOR 13037
DISC CONTROLLER FEATURES

1.0 INTRODUCTION

The 13037 Disc Controller for the 79XX family of disc drives is designed to interface up to eight disc drives with up to eight CPU's. The 13037 may interface with either 3000 or 21XX CPU's (or both) with provisions for future CPU designs.

One of the primary design goals of the 13037 was to relieve the CPU of much of the busy work associated with data transfer. In previous designs, the CPU would have to interact with the disc drive on long data transfers whenever head and/or track switching was required, or whenever an additional seek to a spare track was required. All these functions can now be handled automatically by the 13037 (although it may be programmed as desired to turn these functions on and off).

In addition to these features, the 13037 is capable of operating in two addressing modes: cylinder mode and surface mode. In cylinder mode (figure 1A), once the heads have been positioned over a particular track, data is recorded starting with the lowest numbered head (0) and continuing to the highest numbered head before the heads are moved to a different track. In this way, a "cylinder" of data is generated. In surface mode (figure 1B), only one particular head is used. When the end of the track is reached, a new track is begun using the same head. Thus, data is recorded only on one surface of the disc.

Another time-saving feature of the controller is the mapping of the bit-per-line drive attention request into a drive unit number before transmitting the attention interrupt to the CPU.

2.0 MULTIPLE CPU DISC DRIVE OPERATION

As mentioned in the first paragraph, the 13037 serves as a clearing house for up to eight CPU interfaces and up to eight disc drives. This requires some special design considerations, which will now be described.

Interface selection: interfaces are numbered from 0 to 7 and are polled by (attached to) the controller serially from 0 to 7 and around again. Any interface which has a command ready when it is attached to the controller will remain connected and have its command serviced.

Attention request: after a SEEK or RECALIBRATE command is put out to the drive, the controller disconnects both the interface and that drive and returns to the interface selection (polling) loop to service other interfaces while waiting for the SEEK or RECALIBRATE to complete. When the drive completes its operation, it sets up an attention request to the controller. The controller checks for these requests in between polls to the interfaces, and connects the next drive in sequence that requests attention to the interface which last accessed that drive.

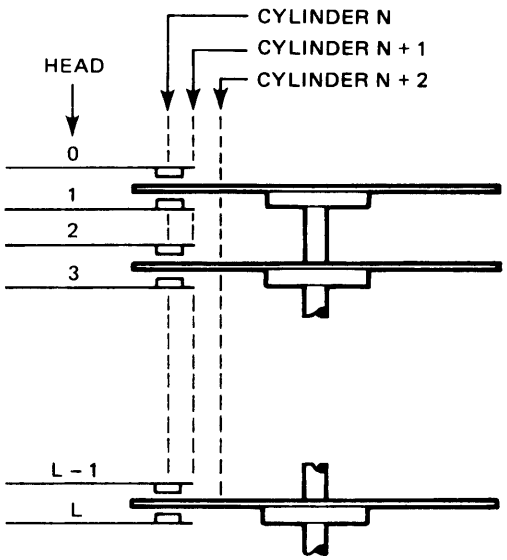


FIGURE 1A. CYLINDER MODE

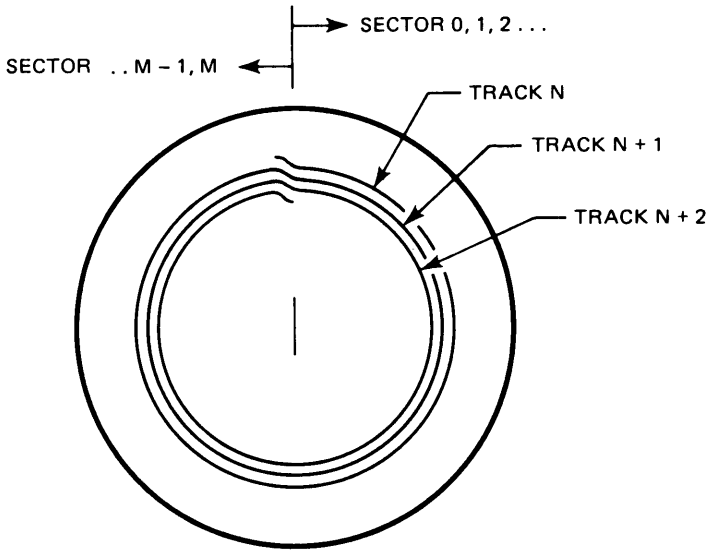


FIGURE 1B. SURFACE MODE

Hold bit: since the controller may service other interfaces between a SEEK (or RECALIBRATE) command from one interface to a given drive and the attention request signaling the end of that operation, what is to stop another interface from accessing that same drive, unknown to the first interface? To prevent this, each drive has a hold bit associated with it. Each command to the controller which references a drive includes a one-bit "hold" field which the programmer may set or clear and which is retained by the controller. While a hold bit is set for a particular drive, no other interface may access it. An attempt to access a held drive will cause the controller to resume polling until that function can be accomplished.

The disc-drive-to-interface mapping is implemented in a small read/write memory on the controller (see figure 2). Each word address (from 0 to 7) in the RAM corresponds to a disc drive, while the contents correspond to the interface which last accessed the drive (left-most three bits) and the hold bit. Figure 2 details what functions the other RAM addresses are assigned.

The entire poll/attention request servicing sequence is shown in the flow-chart of figure 3.

Another consideration of multiple-interface operation is when to disconnect an interface from the controller. In general, the interface cannot be disconnected at the completion of all commands, since abnormal completion status (as well as relevant temporary quantities such as the file mask and disc address registers) would disappear if another interface were allowed to begin a command. Yet, if an interface were always to remain connected, no interface polling could take place.

The 13037 handles this situation by disconnecting from a particular interface only during SEEK, END, or RECALIBRATE instructions, or after a timeout occurs. Note that SEEK and RECALIBRATE disconnects allow holding onto a particular drive for subsequent interface use, while the END command is unconditional.

3.0 THE FILE MASK

The file mask is a four-bit register (bits 3 – 0 of figure 4) which may be set to any desired combination by the programmer. Bits 7 – 4 in the same command word are a retry counter used by the 3000 interface and selector channel to retry data operations in case of an error.

Bit 0, when set, allows the controller to automatically seek to the next higher or lower cylinder address (depending on bit 3) when a data operation continues through the end of the current logical cylinder. The new track is subjected to disc address and track status verification before any further operation is performed. When bit 0 is clear, the option is prohibited, and any data operation which exceeds the end of the current cylinder is aborted with an end-of-cylinder error status.

Bit 1, when set, indicates that the controller is operating in the cylinder mode. In this mode, the first head address is 0 (the top-most head) and head switching occurs automatically following the last data sector of each track. The head address increases incrementally from 0 to the last head address of the particular disc drive. As each new head is switched in, the verification described in the previous paragraph is performed. The last data sector of the last head address of the current track address is the end of the logical cylinder.

When bit 1 is clear, the controller is operating in the surface mode, where the head address never changes. The last sector of the current track address is the end of cylinder. If bit 0 is set (incremental/decremental seek allowed), a data operation which exceeds the end of the cylinder will continue at the next higher/lower cylinder address (subject to address and track status verification).

The following diagram is the layout of the 64-bit (16 x 4) read/write memory which maps the disc unit number (same as the R/W memory address for addresses 0 – 7) into the number of the interface which last accessed that drive. Word 15 contains the number of the interface last polled to see if a command was pending. Word 14 contains the number of the interface currently connected to the controller. Word 13 is a sector counter used by the verification algorithm. Word 12 holds the drive type, returned in bits 12-9 of the drive status word. This word determines how many heads per drive and sectors per track the drive has. If bit 3 of word 11 is set, the platter protect switch for the current surface (7920, 7925) is on, locking out writing of any kind. If bit 2 is on, the drive's Format switch is set to override. Word 8 holds the number of the last drive for which the controller processed an attention request. Command words should not refer to unit 8 or errors may occur.

BIT 3	2	1	0	WORD
X	I	I	I	15
X	I	I	I	14
C	C	C	C	13
D	R	V	T	Y	P	12
R	D	O	N	L	Y	11
I	I	I	H	10
I	I	I	H	9
P	R	V	A	T	N	8
I	I	I	H	7
.	.	.	.	
.	.	.	.	
.	.	.	.	
I	I	I	H	1
I	I	I	H	0

WHERE I is a 3-bit number (0 – 7) representing the interface to which the associated drive (word number) was last connected. For words 15 and 14 only, the I-field is as described above the diagram. Words 15 and 14 are the same except when the controller is responding to a drive attention bit. There can be no disc drive 8 – 15.

H if set means that the interface has reserved (held) the drive for a series of operations. While H is set, no other interface may access that drive.

C is a sector counter used by subroutine "spare".

X is not used.

Figure 2. READ/WRITE Memory Layout

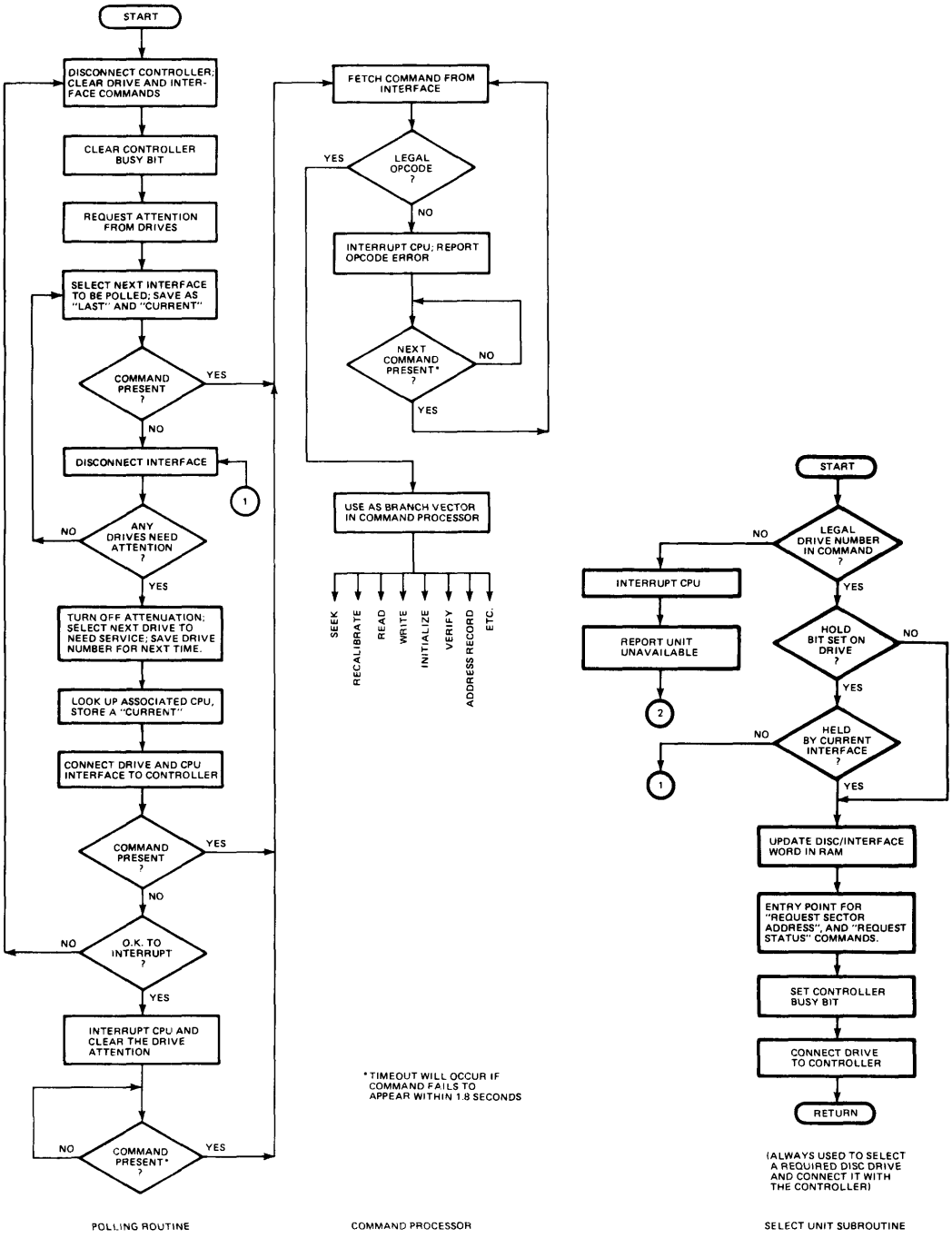


Figure 3. Interface Poll Loop, Command Processor, Select Unit Subroutine

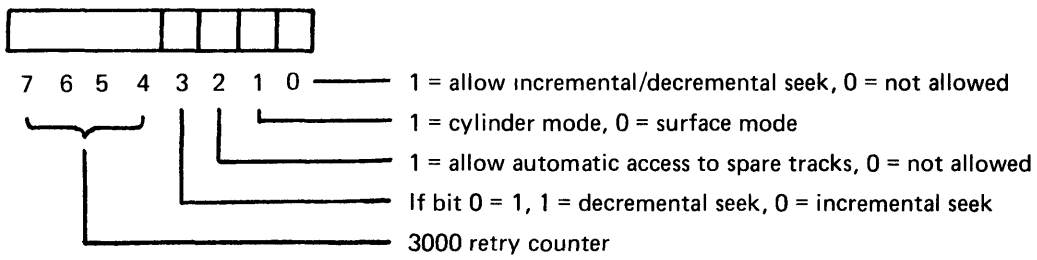


Figure 4. File Mask and Retry Counter

When bit 2 is set, the controller is allowed to automatically seek to previously initialized spare tracks when a defective track (that is, one which has been initialized defective) is encountered. (The entire spare track algorithm will be described later.) If bit 2 is clear, the automatic sparing will not occur and a defective track error status will be reported to the interface.

Bit 3 operates in conjunction with bit 0 and determines whether an automatic end-of-cylinder seek will be to the next higher or lower track address. If bit 3 is 0, the next higher track is selected; if it is 1, the next lower track is selected. Note: If bit 0 is 0, bit 3 is not examined.

4.0 SPARE TRACKS AND THE 13037

4.1 WHY SPARE TRACKS?

Why spare anything? In a disc drive the heads do not contact the magnetic surface (floppy discs excepted) but fly a small distance above it. Even this small distance compounds the complexity of accurate data recovery. Errors, while not common, do occur (for example when a microscopic particle intervenes between the disc surface and the head). The sparing process, used on most (if not all) high-quality disc systems, has two objectives: to recover as much of the data from the bad area as possible, and to flag the bad area so that it will not be used again.

Although the smallest addressable space on the disc is the sector, most files take up many times this space. It would be impractical to maintain the system overhead (including increased access times) necessary to assign and remember spare areas on a sector-by-sector basis. A large part of this overhead includes an address and sector status field which must by physically separate from the data field of the sector. Without this, the address and status could not be verified on the same rotation as the data transfer. The gap between the two fields would be wasted space, thus lowering the overall capacity of the disc.

On the other hand, if an error caused an entire cylinder to be spared and marked defective because of a microscopic area which faulted one sector, vast areas of the disc might soon be marked defective and similarly large spare areas might be required.

As in most other situations, a compromise has been achieved, whereby one track is made to answer for the sins of a dust particle. A track is defined as the area accessible by one head with the head access mechanism positioned at a given cylinder. In the 13037, spare areas are assigned on a track-for-track basis. Although the spare track need not be on the same surface as the defective track, a systematic procedure still must be adhered to by the operating system when assigning and generating the spare track in order for the automatic spare track access algorithm to work properly.

Briefly, when a defective track is first discovered (via a disc parity error), the operating system must assign and initialize a spare track and initialize the bad track as defective. If this is done properly (and automatic track sparing is enabled in the file mask), the system can forget about the spare track from then on; the controller will take care of the extra access required to get to the spare track whose logical address is that of the defective track.

So first we'll examine how to generate a spare track, and then how the 13037 accesses it.

4.2 HOW TO GENERATE A SPARE TRACK

Suppose the operating system, while reading cylinder 100, head 0, sector 0 (abbreviated (100,0,0) from now on), as in figure 5A, determines that a permanent data error exists, and that a spare track must be generated. The system looks up the next available spare track (e.g., (406,1)) in an appropriate table.

The system initializes each sector of the spare track with the disc address of the defective track (note the difference in addresses) with sectors of the spare and defective tracks corresponding one-for-one. (The detailed steps of how to do this are shown below.) The S-bit (spare bit) is set to 1. See figure 5B. Optionally, data may be copied from the defective track to the spare track during the initialization process by reading one sector at a time, ignoring all error status, and then initializing the corresponding sector of the spare track with the data from the defective track. This process risks copying a data error, but preserves the remainder of the valid data in a track if only one sector is defective.

Following the initialization of the spare track, the system then initializes the defective track with the disc address of the spare track (again, note the difference in addresses). This time the D-bit (defective bit) is set to 1. See figure 5C. The system then deletes the just-assigned spare track from its table of available tracks and then forgets about the track completely.

The command steps necessary to generate a spare track are:

1. Enable automatic track sparing.
2. Seek to the first sector of the defective track.
3. Read the sector, ignoring all error status.
4. Seek to the same sector of the spare track.
5. Perform an ADDRESS RECORD command with the defective track address. This sets controller registers to the desired disc address but does not talk to the drive.
6. Perform an INITIALIZE command, transferring the data from the defective sector to the spare sector. Be sure the S-bit is set in the INITIALIZE command word.
7. Repeat steps 2 through 6 for each sector of the track.
8. Seek to the defective track.
9. Verify one sector. This will get the controller to any spare track which may exist as the result of a previous spare track generation.
10. Perform an ADDRESS RECORD command with the cylinder address set to 177777 (octal) (i.e., garbage).
11. Initialize the entire track without intervening seeks. Make sure the S- and D-bits are clear.
12. Seek to the defective track. Do NOT verify, as was done in step 9.
13. Perform an ADDRESS RECORD command with the spare track address.
14. Initialize as many sectors at a time as feasible (the data field is irrelevant). Be sure the D-bit is set in the INITIALIZE command word.
15. Repeat steps 13 and 14 until the entire track has been initialized defective.

Figure 5. Generating a Spare Track

Although it seems that the defective track is being initialized twice (true in most cases), this sequence is required in case a track previously initialized spare fails. This sequence assures that the spare track which failed is given a garbage address so that it can never be accessed during normal operation.

If data is not being copied to the spare track, the spare track can be initialized spare as many sectors at a time as is feasible, just as steps 13 and 14 were used above to initialize the defective track.

4.3 HOW A SPARE TRACK IS ACCESSED

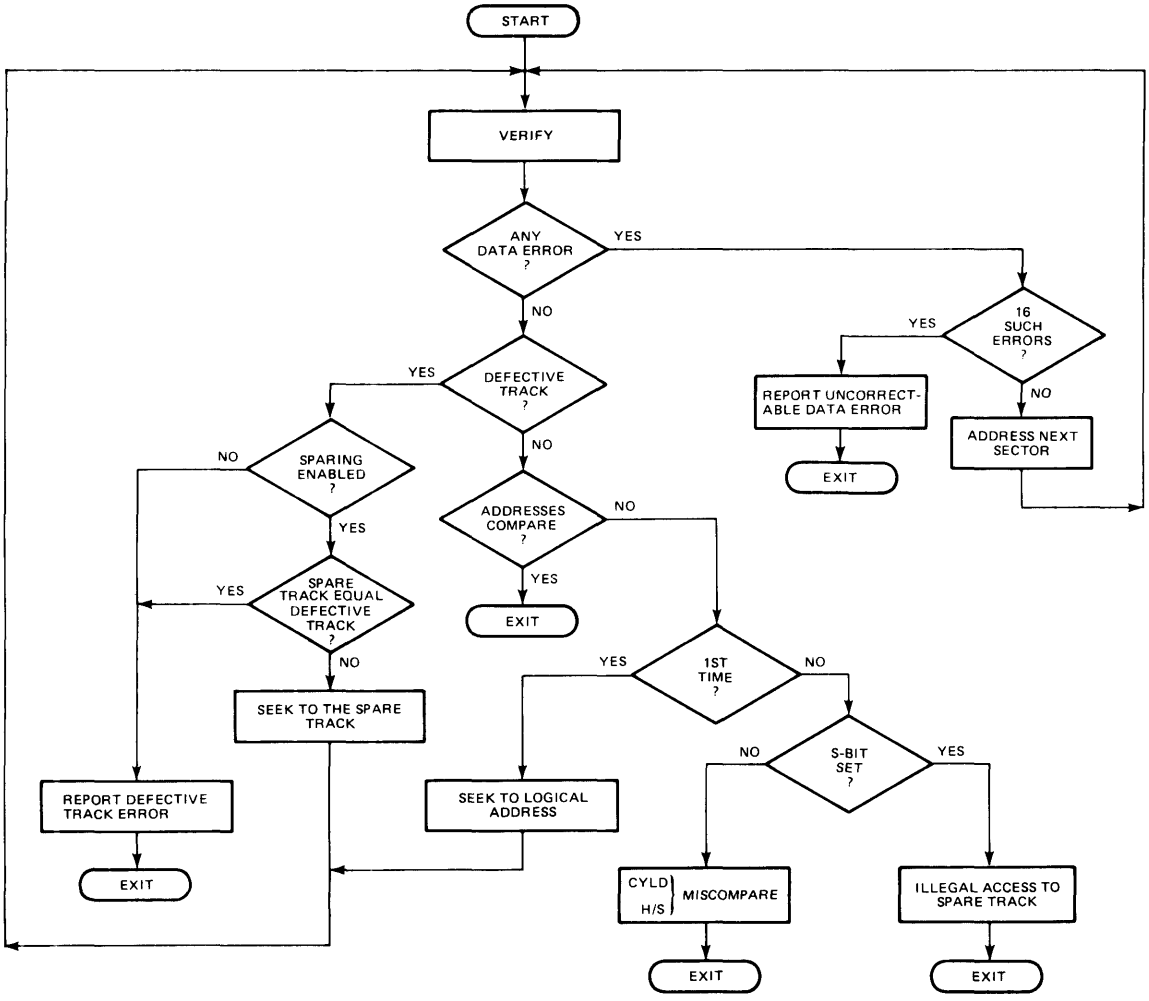
To assure that data is transferred to/from the proper area of the disc, the desired address (in CYLAD and HSAD) is periodically compared to that in the address field of the sector on the disc. The comparisons are made before each transfer and whenever a track boundary is crossed for a VERIFY command and all data transfer commands except INIT, WFS, and RFS. For RNVFY, the comparison is omitted at the start of transfer only.

In addition to address verification, a spare track access algorithm (figure 6) provides automatic 13037 accessing of spare tracks if the feature is enabled in the file mask. With this feature, a computer system need only assign a spare track when a regular track proves defective. It can then forget the spare track and make all accesses through the original logical track address, even though the physical track has a defect. Both spare track accesses and address verification are implemented in subroutine SPARE.

Subroutine SPARE is called only after a verify operation has read the address area of a sector into temporary storage. The subroutine's algorithm is shown below:

```
SPARE:    WHILE DATA'ERROR DO
              BEGIN IF NUMBER'OF'ERRORS >= 16 THEN
                GO TO UNCORRECTABLE'DATA'ERROR;
              INCS;    & NOT AT LIMIT YET, TRY NEXT SECTOR.
              END OF DATA'ERROR;
          IF D'BIT THEN
              BEGIN IF NOT SPARING'ENABLED THEN GO TO
                DEFECTIVE'TRACK'ERROR;
              IF CYLAD = TCYLD AND HSAD'UPPER = THSAD'UPPER
                THEN GO TO DEFECTIVE'TRACK'ERROR;
              SEEK'TO'TCYLD'AND'THSAD;
              VERIFY'SECTOR;
              GO TO SPARE;
              END OF D'BIT;
          IF CYLAD <> TCYLD OR HSAD <> THSAD THEN
            IF ADDRESS'ERROR'FLAG
              THEN GO TO ADDRESS'ERROR
              ELSE BEGIN ADDRESS'ERROR'FLAG  := TRUE;
                   SEEK'TO'CYLAD'AND'HSAD;
                   VERIFY'SECTOR;
                   GO TO SPARE;
                   END OF ADDRESS'ERROR;
          ADDRESS'ERROR'FLAG  := FALSE;
          END OF SPARE;
```

The first thing we must do is check for a read error. If there is one, we can't trust the address area we just read. So we remember our original target sector (done externally), increment to the next sector, and try again. To avoid looping indefinitely, we limit the number of re-reads to 15 (the highest count we can store in word 13 of our scratch-pad RAM.



NOTE THAT ON POSSIBLE ADDRESS MISCOMPARES, THE CONTROLLER WILL SEEK TO THE TARGET ADDRESS IT DESIRES IN AN ATTEMPT TO CORRECT THE MISCOMPARE. IN MULTIPLE CPU ENVIRONMENTS, THIS CAPABILITY CAN CAUSE TRANSFERS ON UNWANTED AREAS OF THE DISC; FOLLOWING EACH "SEEK" OR "RECALIBRATE" INSTRUCTION BY AN ADDRESS RECORD COMMAND WILL PREVENT SUCH OCCURRENCES.

Figure 6. Basic Sparing Subroutine

Once we have a valid address area, we check the defective bit (D-bit). If it's set, we're on a track which was flagged (initialized) defective earlier. If we're allowed to access the spare track, and the defective and spare track addresses are not the same, we seek to the spare track on our own, read (verify) a sector, then start over again. Thus we can go through as many defective tracks as required to get to the spare, as long as we don't get back to where we started (else we would loop endlessly).

If the D-bit isn't set, we compare the address (cylinder, head, and sector) read from the disc (TCYLD and THSAD) with that in CYLAD and HSAD. If they match, we're done. If not, we set a flag, seek on our own to CYLAD and HSAD, and try once more. If the comparison fails again, we report an address error of some kind (cylinder miscompare, head/sector miscompare, or illegal access to spare track).

An example will show the required disc format and how it is used to access the spare track. Consider the two sectors shown (address field only) and the following sequence of events:

PHYSICAL ADDRESS			DISC ADDRESS FIELD					
CYL	HEAD	SECTR	CYL	S	P	D	HEAD	SECTR
100	0	23	406			1	1	23
406	1	23	100	1			0	23

1. 13037 seeks to cylinder 100, head 0, sector 24 (100,0,24).
2. Back up one sector, verify 100,0,23.
3. No errors, but D-bit set.
4. Logical address (100,0,23) ≠ disc address (406,1,23), so seek to spare (disc) address (406,1,23), then forget it. Retain logical address (100,0,23) only.
5. Verify (read) physical sector 406,1,23.
6. Assume no error. Also no D-bit, so compare addresses.
7. Logical address (100,0,23) matches disc address (100,0,23), so bump to sector 24 and begin transfer.
8. At end of track, assume cylinder mode. 13037 will bump its address from 100,0,47 to 100,1,47, while drive will be addressed to 406,2,47 (head carriage doesn't move here, only head and sector are addressed).
9. Because of track crossing, a verify is made and the disc address (406,2,47) is found to differ from the controller target address (100,1,47).
10. A controller generated seek is issued to the target address (100,1,47) and a subsequent verify is made.
11. Disc address read from verify (100,1,47) now matches target address (100,1,47), so the transfer begins with the next sector (100,1,0). (If the verify had produced a set D-bit, sparing would again take place.)

Note that by using this scheme, we can detect a defective track, get to its spare track, transfer data, return to the track following the defective track, and continue transferring data, all without CPU or channel intervention.

4.4 DIRECTLY ACCESSING A SPARE TRACK

What if the channel causes a seek directly to a spare track? The following sequence then takes place (using our earlier address):

1. 13037 seeks to 406,1,24.
2. Back up one, verify 406,1,23.
3. No errors, no D-bit, 406,1,23 ≠ 100,0,23,
4. Set address error flag, seek to logical address 406,1,23, verify.
5. No errors, no D-bit, 406,1,23 ≠ 100,0,23.
6. Flag set, address miscompare established.
7. S-bit set, so report attempt to directly access spare track, rather than address miscompare.

Thus a spare track can only be accessed through its corresponding defective track (except , of course, for commands such as READ FULL SECTOR, which do not perform address comparisons or track status verification).

5.0 AUTOMATIC HEAD AND/OR TRACK SWITCHING

Earlier controllers required CPU intervention to change the head and track addresses whenever a multiple-sector operation (READ, WRITE, VERIFY, INITIALIZE) continued beyond the end of a disc track. The 13037 eliminates the need for this handshake (if automatic head and/or track switching is enabled in the file mask), thus leaving the CPU free until the end of the transfer. The basic assumption made is that logical sector 0 of the next track follows the last logical sector of the current track (whether in cylinder or surface mode).

Consider the hypothetical situation shown in figure 7A, with the controller reading while in cylinder mode. The controller finishes (45,0,47), discovers it has more data to transfer, and is allowed to switch heads. It switches to head 1, but it must verify the disc address before continuing the data transfer (the reason for this will be clear shortly). It must also verify (for WRITE operation only) that the upcoming track has not been initialized protected. The controller could verify sector 0 of the new track to assure itself of proper address and track status. Normally these fields would check, but sector 0 would then have passed and we would have to wait out one rotation of the disc to continue the data transfer.

To prevent this, logical sectors are "staggered" as tracks progress downward on the cylinder (see figure 7B). Thus, as the disc rotates, sector 47 of the next head follows sector 47 of the current head. Address and track status verification can be performed on sector 47 of the new track, then (normally) data transfer can continue immediately with sector 0. Note that the physical sector address (the one the drive itself sees) does not change from track to track. The mapping from logical sector to physical sector is done at only one point in the microcode (at the moment of truth when the address is transmitted to the drive); therefore the controller deals only with logical sectors.

The only other time the difference arises is during the "REQUEST SECTOR" command. The drive returns the physical sector address, which must be inverse-mapped into the logical address before transmitting it to the interface.

The mapping itself is straightforward, and consists of adding the head address to the logical sector address and taking the result Mod (# Sectors/Track). This is the physical sector address sent to the drive (see figure 7B).

Note that all the spare track generation and access algorithms still work, because the controller does all its operations on logical sectors.

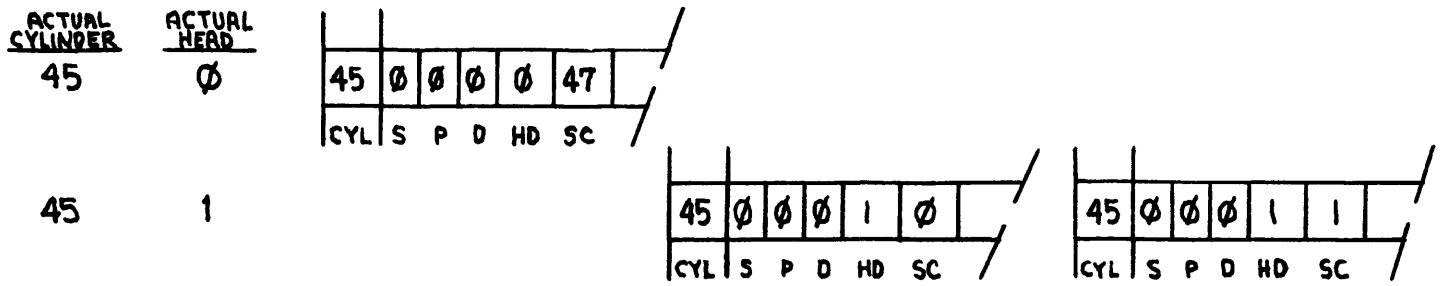


Figure 7A. Hypothetical Disc Layout, Sectors Not Staggered

HEAD	SECTORS				
Ø	47	Ø	1	2	LOGICAL
	47	Ø	1	2	PHYSICAL
1	46	47	Ø	1	LOGICAL
	47	Ø	1	2	PHYSICAL
2	45	46	47	Ø	LOGICAL
	47	Ø	1	2	PHYSICAL

Figure 7B. Logical vs. Physical Sectors

Now why is address verification required at all? (We've already seen why the P-bit must be checked.) Because of the possibility of automatic track sparing. Consider a similar example to the above one (figure 8). The controller has read logical (100,0,47) (spared to physical track and head (406,1), logic sector 47) and has more to do. In cylinder mode it will switch to (406,2,47), another spare track. If there were no verification, the controller would transfer logical (200,1,47) (actually (200,1,0), since without verification no sector offset would be required). This is wrong, since the system expects logical (100,1,0).

What actually happens is as follows: when the controller seeks to the spare track (as described earlier), it immediately forgets the physical cylinder and head address, retaining only the logical address (100,0). When it finishes sector 47, it switches to (it thinks) logical address (100,1,47) (last logical sector, head 1), then attempts to verify that sector. Since it actually switched to (406,2,47) it will read logical address (200,1,47) which fails when compared to (100,1,47).

So even with verification, addresses may not compare. What then? The controller has retained the logical next address (100,1,47), so just in case the address mis-comparison resulted from such a situation, it automatically issues a seek (with wait) to the logical address, then tries once more to verify the sector at that address. If it is successful, the transfer continues. If not, and the track has not been initialized defective, the address error is assumed to really exist and is reported as such to the system. (If it has been initialized defective, the address field contains a spare track address, and a spare track access operation begins anew.)

For an overview of the track verification and sparing operation, see the flowchart, figure 6.

6.0 SOME ROUTINE OVERVIEWS

The following set of routines, DECS, INCHS, INCS, and SECTR, are all used to send the proper address to the disc before all data transfers and between sectors of a multiple-sector transfer. Each routine is described in detail adjacent to its coding. These comments are an overview of their group function.

The user need not re-address the 13037 or disc drive (via an ADDRESS RECORD or SEEK command) between data transfers which progress in either cylinder mode or surface mode. (The user must set the mode using the SET FILE MASK command before starting the transfer.) These terms are defined as follows:

1. CYLINDER MODE — Data is transferred in ascending order of sectors, then in ascending order of heads, and finally in ascending or descending order of cylinders. All heads at a given head carriage position are accessed before the heads are moved. Algorithmically speaking, cylinder mode can be written:

```
FOR CYLINDER  := CYL1 STEP +/-1 UNTIL CYL2 DO
  FOR HEAD  := 0 10 M--1 DO        & M HEADS IN THE DRIVE.
    FOR SECTOR  := 0 TO N--1 DO        & N SECTORS PER TRACK.
      TRANSFER (CYLINDER, HEAD, SECTOR);
```

2. SURFACE MODE — For a given head, data is transferred in ascending order of sectors, then in ascending or descending order of cylinders. Only one head is used, then the heads must be moved to continue the transfer. Algorithmicly:

```
HEAD  := 1;        & 0 <= 1 <= M-1
FOR CYLINDER  := CYL1 STEP +/-1 UNTIL CYL2 DO
  FOR SECTOR  := 0 TO N-1 DO TRANSFER (CYLINDER, HEAD, SECTOR);
```

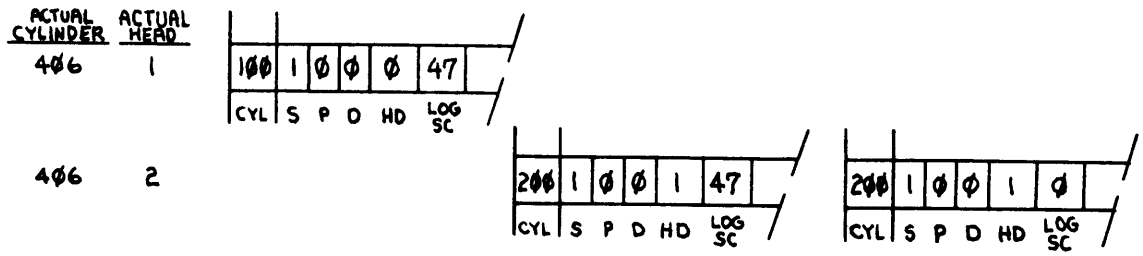


Figure 8. Head Switching at End of Spare Track

The end of logical cylinder occurs whenever the heads must be moved to continue a transfer (whenever the "FOR CYLINDER . . ." statement is executed) in either cylinder or surface mode. Thus, in surface mode, a logical cylinder and a track are equivalent.

The 13037 will automatically maintain the next addressed to be transferred:

1. When a transfer completes normally (no errors), the address in the 13037 is that of the next sector to be transferred. Thus a new transfer request will continue the transfer.
2. When an error occurs, the address in the 13037 is that of the erroneous sector. The system may then retry the transfer, starting with the bad sector.

In either case, the REQUEST DISC ADDRESS (REQAD) command will return the address pointed to by the 13037 (current sector if error, next sector if no error).

By clearing bit 0 of the file mask, the user may prevent the automatic seek at the end of logical cylinder. Transfers which try to continue beyond the end of logical cylinder are aborted with an end-of-cylinder (EOC) error status, although a REQAD command will return the address of the first sector of the new cylinder.

This conflicts with our earlier statement. If a transfer ends without error at the end of a logical cyliner, the 13037 should point to an address on the next cylinder, implying that a seek has occurred. But if the automatic seek bit in the file mask is clear, the seek attempt will cause an EOC error. The user will be puzzled because the data transfer didn't cross a cylinder boundary.

To avoid a possible end-of-cylinder (EOC) error when a transfer ends normally at the end of a logical cylinder, the address update is performed in three steps:

1. The next head and sector address are set by subroutine INCHS (increment head and sector), based on the current address and on cylinder or surface mode. The algorithm is:

```
INCHS:      IF NOT LAST'SECTOR
              THEN SECTOR  := SECTOR + 1
              ELSE BEGIN NEW'TRACK'FLAG  := TRUE;
                   IF CYLINDER'MODE THEN
                     IF NOT LAST'HEAD
                       THEN BEGIN HEAD  := HEAD + 1;
                                  GO EXIT;
                                  END
                       ELSE HEAD  := 0;
                   END'OF'CYLINDER'FLAG  := TRUE;
                   END OF LAST SECTOR OF TRACK;
EXIT: END OF INCHS;
```

Note that 1) a true end-of-cylinder flag (EOCF) implies that the new track flag (NWTRF) is also true, 2) we haven't tried to perform any seek (which could generate an EOC error), we've just left EOCF set to tell us it needs doing if we go on, and 3) if NWTRF is set, we haven't changed sector. This is because we just finished sector N−1, and (usually) we next verify sector N−1 of the next track.

2. The data transfer is checked for completion (end of transmission) in the individual command processors. If so, the 13037 completes command processing leaving EOCF and NWTRF as they were set (or cleared) by INCHS. A REQUEST DISC ADDRESS (REQAD) command issued here will examine EOCF and NWTRF to report the proper next address, not the in-between one actually contained in the 13037.
3. If the transfer is not complete, the user is committed to crossing a cylinder boundary if required, and we can now check the auto seek bit, perform the seek, and generally finish the address updating process. This is done in subroutine SECTR, using the EOCF and NWTRF conveniently left lying around by INCHS:

```
SECTR:      IF END'OF'CYLINER'FLAG THEN     & NEXT CODE IS SUBR DECS2.
                BEGIN IF NOT AUTO'SEEK'ALLOWED THEN GO TO
                  END'OF'CYLINDER'ERROR;
                IF SEEK'DIRECTION = 1
                  THEN CYLINDER  := CYLINDER - 1
                  ELSE CYLINDER  := CYLINDER + 1;
                SEEK2;    & RESETS EOCF, NOT NWTRF.
                SWAIT;    & WAIT FOR SEEK TO COMPLETE.
                END OF DECS2;
            IF NEW'TRACK'FLAG THEN    & WE'RE STARTING A NEW TRACK.
                BEGIN NEW'TRACK'FLAG  := FALSE;
                IF INITIALIZE'GLAG
                  THEN GO TO INCS   & INIT, WFS OR RFS, NO VERIFY.
                  THEN GO TO STRT3;    & MUST VERIFY SECTOR.
                END OF NEW'TRACK'FLAG;
            END OF SECTR;
```

This takes care of multiple-sector transfers, including those which end on a track or cylinder boundary. Now what about a new transfer without (re-)addressing the drive. We generally want to back up one sector, verify one, restore the original sector address, then begin the transfer. This can be done with the following sequence:

```
JSB DECS
JSB SWAIT
JSB VRFY
JSB SPARE
JSB INCS
```

. . . as long as DECS can cope with EOCF and NWTRF if either or both are set. In these cases, DECS functions in much the same way as SECTR. If neither EOCF nor NWTRF is set, we merely decrement the sector:

```
DECS:       IF END'OF'CYLINDER'FLAG    & THEN IT MUST BE A CONTINUATION.
              THEN BEGIN NEW'TRACK'FLAG  := FALSE;
                   DECS2;    & SEE EXPANSION IN SECTR.
                   END
              ELSE IF NEW'TRACK'FLAG    & THEN IT'S ALSO A CONTINUATION.
                     THEN NEW'TRACK'FLAG  := FALSE
                     ELSE BEGIN SECTOR  := SECTOR - 1;
                                IF SECTOR < 0 THEN SECTOR  := MAX'SECTOR;
                                END OF NORMAL DECREMENT;
            END OF DECS;
```

For an INIT, WFS, or RFS command, we don't verify a sector preceding transfer, but we must still call DECS and INCS in case either EOCF or NWTRF is set, so as to treat continuations properly.

Note that a SEEK, ADDRESS RECORD, or RECALIBRATE command resets both EOCF and NWTRF (because the drive and 13037 have been re-addressed). Also, an error during a sector is detected and handled before INCHS is called; therefore neither EOCF nor NWTRF will be set.

CONTENTS

Page

Command Words 10-1
Control Commands 10-3
RECALIBRATE 10-3
SEEK 10-4
CLEAR 10-5
ADDRESS RECORD 10-6
SET FILE MASK 10-7
END 10-8
WAKEUP 10-9
Sense Commands 10-10
REQUEST STATUS 10-10
REQUEST SECTOR ADDRESS 10-14
REQUEST SYNDROME 10-15
LOAD TIO REGISTER 10-19
REQUEST DISC ADDRESS 10-20
Read Commands 10-20
COLD LOAD READ 10-21
READ 10-22
READ FULL SECTOR 10-23
VERIFY 10-24
READ WITH OFFSET 10-25
READ WITHOUT VERIFY 10-26
Write Commands 10-26
WRITE 10-27
WRITE FULL SECTOR 10-28
INITITALIZE 10-29

PROGRAMMING INFORMATION

COMMAND WORDS

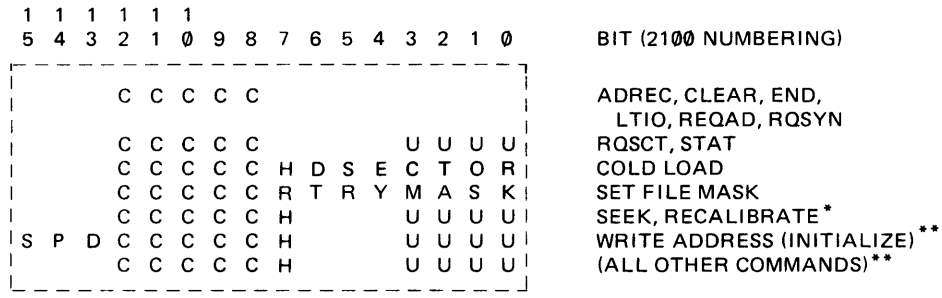
To initiate an operation, the controller accepts a 16-bit command word from the CPU interface, decodes, and executes the operation specified. The command may pertain to the controller only, a selected disc drive only, or both. Some commands require additional information from the interface for proper execution. Each command is discussed separately in the following paragraphs. The command word format relating to a specific command is shown at the beginning of each paragraph. Bits 8 through 12 of the command are used for the opcode (that is, the octal representation that identifies each command). The U referred to in the command format is the disc drive unit number. (The crosshatched bits indicated in some of the command words are not processed by the controller.) Table 10-1 is a listing of command codes and commands. The commands are listed functionally as control, sense, read, and write groups. They are also discussed in the following paragraphs in functional groups. The timeout function referred to in the discussion is approximately 1.8 seconds, and is initiated when the controller must wait more than that time for a subsequent CPU command.

Table 10-1. Command Codes

CODE (OCTAL)	COMMAND AND GROUP			
	CONTROL	SENSE	READ	WRITE
00			Cold Load Read	
01	Recalibrate			
02	Seek			
03		Request Status		
04		Request Sector Address		
05			Read	
06			Read Full Sector	
07			Verify	
10				Write
11				Write Full Sector
12	Clear			
13				Initialize
14	Address Record			
15		Request Syndrome		
16			Read with Offset	
17	Set File Mask			
22			Read without Verify	
23		Load TIO Register		
24		Request Disc Address		
25	End			
26	Wakeup			

Each disc drive has a "hold" bit associated with it to prevent two or more CPU interfaces from accessing the same disc drive at the same time. Each command to the controller that references a disc drive (except REQUEST STATUS and REQUEST SECTOR ADDRESS) includes a one-bit hold field which is retained by the controller. While a hold bit is set for a particular disc drive, no other CPU interface may access it with a command that could modify the disc drive status. An attempt to access a held disc drive will cause the controller to leave the command pending on the interface until the desired drive becomes available.

COMMAND FORMATS



WHERE C = FIVE-BIT COMMAND OPCODE:

AS SHOWN	OCTAL	DESCRIPTION
0	0	COLD LOAD READ (BOOT)
400	1	RECALIBRATE
1000	2	SEEK
1400	3	REQUEST STATUS
2000	4	REQUEST SECTOR ADDRESS
2400	5	READ
3000	6	READ FULL SECTOR
3400	7	VERIFY
4000	10	WRITE
4400	11	WRITE FULL SECTOR
5000	12	CLEAR
5400	13	WRITE ADDRESS (INITIALIZE)
6000	14	ADDRESS RECORD
6400	15	REQUEST SYNDROME
7000	16	READ WITH OFFSET
7400	17	SET FILE MASK
10000	20	(NOT AVAILABLE IN 13037 INSTRUCTION SET)
10400	21	(NOT AVAILABLE IN 13037 INSTRUCTION SET)
11000	22	READ WITHOUT VERIFY
11400	23	LOAD TIO REGISTER (3000 SYSTEM)
12000	24	REQUEST DISC ADDRESS
12400	25	END (RETURNS CONTROLLER TO POLL LOOP)
13000	26	WAKEUP

S = FLAG AS SPARE TRACK.
P = FLAG AS PROTECTED TRACK (SUBSEQUENT WRITE COMMAND MAY FAIL).
D = FLAG AS DEFECTIVE TRACK.
HD = HEAD ADDRESS FOR COLD LOAD READ COMMAND.
H = HOLD BIT OF DRIVE
RTRY = DATA TRANSFER RETRY COUNTER (3000 ENVIRONMENTS).
MASK = FILE MASK BITS (SEE DESCRIPTION IN SFMSK PROCESSOR).
U = DISC DRIVE (UNIT) ADDRESSED BY THE COMMAND. ERRORS MAY OCCUR IF U = 10 (OCTAL).
BIT 7 = HOLD BIT. IF SET, RESERVES DRIVE "U" FOR INTERFACE ISSUING THE COMMAND. COMMANDS FROM OTHER INTERFACES TRYING TO ACCESS THIS DRIVE WILL BE DEFERRED UNTIL THE DRIVE IS AVAILABLE.

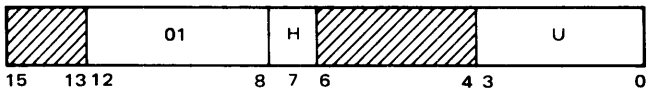
*HOLD BIT (BIT 7) USUALLY SET TO 1
**HOLD BIT (BIT 7) USUALLY SET TO 0

CONTROL COMMANDS

Control commands start operations not involving a transfer of data sectors between the controller and computer. Instead these commands are used to establish certain known conditions within the controller or disc drive. In multi-CPU environments, the ordering and inclusion of certain of these commands warrant special considerations if software is to function as desired; these considerations will be pointed out as they apply to the various commands.

It should be noted that when a command is accepted by the controller, the busy bit of the calling interface is set (and remains set until command completion). In addition, RQSRV is issued after every transfer of control information other than the command word, and after every data transfer. The characteristics of the busy bit and RQSRV issuance apply to all commands of each functional group.

RECALIBRATE



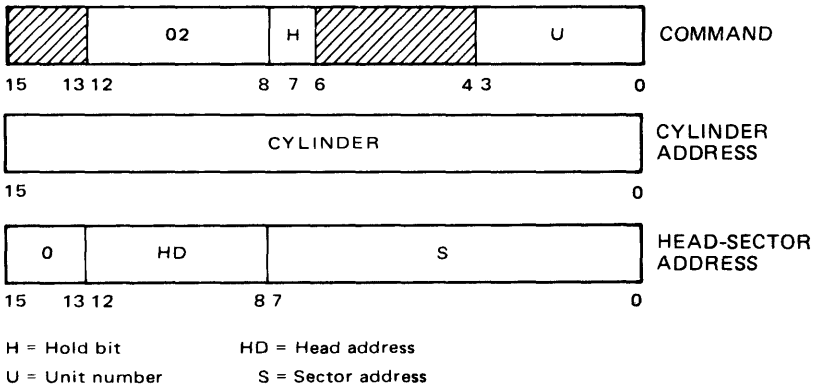
H = Hold bit
U = Unit number

The RECALIBRATE (SEEK HOME) command provides the operating system with a means of restoring the disc drive's heads over a known cylinder (always 0) after that drive is suspected of having lost track of its exact position. To perform this command, only the command word is necessary. The word contains only the opcode, the hold bit, and unit number. If the addressed unit is available and ready, the controller issues a RECALIBRATE command and returns to the poll loop. The disc drive positions its heads over cylinder 0 and clears its "current cylinder address" register.

If the desired drive is found to be "held" by another interface, the controller will leave the RECALIBRATE command pending at the current interface and resume polling. Further, if a unit number greater than 10 is requested, the CPU will be interrupted with a "unit unavailable" error. If the drive unit is available but will not respond, STINT is sent to the interface (and the appropriate Status 2 word is generated). The controller then waits for a new command (or a timeout to occur).

As with the SEEK command, the mechanical process of moving the heads consumes enormous amounts of time relative to execution of CPU instructions; thus the controller will disconnect the current interface and return to polling. In this way, the controller can service other CPU's while the current CPU waits for the desired drive to finish its seek. If another CPU has an available command which can be executed (that is, does not require the use of a drive held by another CPU), the controller will service that command. Eventually the original drive indicates to the controller that its heads are positioned by setting its attention bit. The controller recognizes the attention bit whenever it is polling. (If another CPU has been serviced during the seek, it should eventually issue an END command to cause the controller to resume polling.) The controller reconnects the CPU and the drive. Sometimes, however, the CPU will have no command pending (the CPU, too, may elect to perform other duties while waiting for the drive to complete its mechanical seek); in this case, the controller will determine if it may interrupt the CPU by interrogating the INTOK (Interrupt O.K.) flag. If true, STDFL will be flagged to the CPU; if false, the controller will continue to poll until a command becomes available or an interrupt is allowed.

SEEK



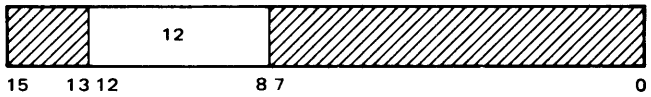
The SEEK command will cause positioning of the disc drive's heads over the desired cylinder; at the same time the controller and drive will store the transmitted cylinder, head, and sector address in their internal registers to allow subsequent verification of the actual address transmitted from the drive prior to any data transfer. This instruction is initiated by issuing the command word followed by two additional words in the order shown. The first contains the cylinder address and the second contains the head and sector address. The controller requests each of these words by transmitting STDFL to the interface. The controller then transmits them to the disc drive.

If the addressed unit is available and ready, the controller accepts the two address words and correspondingly issues the appropriate information to the disc drive to initiate the seek operation. The controller then returns to the poll loop. When the drive completes its seek, an attention bit is set to notify the controller that the drive is ready. The controller, upon recognizing this bit (see corresponding description under the RECALIBRATE command), reconnects the CPU to the drive. If no command is pending, the CPU generated INTOK flag is checked to see if a subsequent interrupt is allowed. If true, STDFL is sent to the CPU and the controller waits for the next command. If INTOK is false, the controller will continue to poll until a command becomes available or an interrupt is allowed.

If the desired drive is found to be "held" by another interface, the controller will leave the SEEK command pending at the current interface and resume polling (the two address words will not be requested at this time). Further, if a unit number greater than 10 is requested, the CPU will be interrupted with a "unit unavailable" error. If the drive unit is available but not ready, STINT is sent to the interface after acceptance of the address words. The controller then waits for a new command (or a timeout to occur).

Note that the target head, sector, and cylinder address are retained in the controller for future data operations, but will be overwritten by a subsequent ADDRESS RECORD or SEEK command. Since the controller polls other interfaces before reporting a seek completion, the programmer should issue an ADDRESS RECORD command immediately preceding a disc drive transfer to refresh the controller's memory as to the current position of that drive.

CLEAR

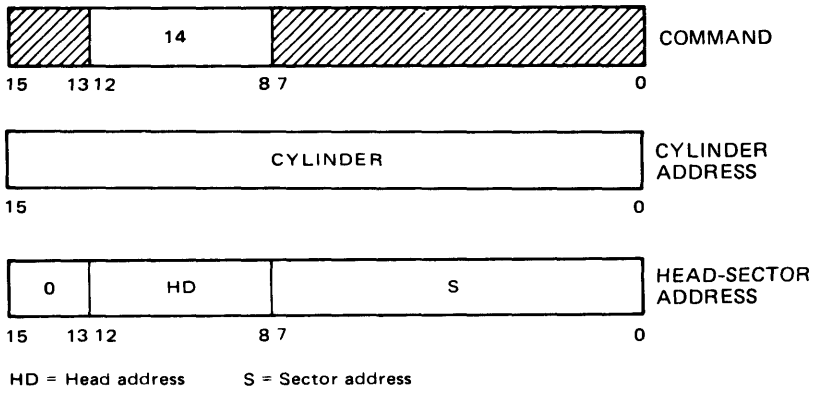


Upon receipt, the controller will issue a CLEAR to all drives, clear status, clear any clock or head offset, turn off the timer, clear the interface busy bit, disconnect all disc drives, transmit Set Data Flag (STDFL) to the interface, and wait for the next command (or a timeout). A unit number is not required.

Because the CLEAR command issues a clear to all disc drives simultaneously (regardless as to whether they are selected), this command should be used with caution in multi-CPU applications.

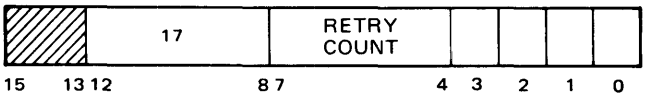
Note that the software clear command differs from the "hard clear" sent to the controller by the interface. The latter unconditionally resets the controller to its power-on state (i.e., all CPU/drive mapping is reset, polling returns to its initial state, current command processing is lost, etc.). For this reason, only one CPU interface should be enabled to issue a "hard clear", such that conflicts will not arise where more than one CPU can unconditionally reset the controller.

ADDRESS RECORD



This command is used to set a logical address in the controller without transmitting it to the disc drive. The issuance of the command word is followed by two words in the order shown. The first contains the cylinder address and the second contains the head and sector address. The controller requests each of these words by transmitting STDFL to the interface. Upon receipt, the controller transmits Request Service (RQSRV) to the interface and waits until either a command is received or a timeout occurs. At completion of this command, the controller waits for a new command (or a timeout). If used in a multiple computer environment, an ADDRESS RECORD should follow each SEEK or RECALIBRATE command, or should precede a data transfer operation if the SEEK or RECALIBRATE is not used. Single CPU environments should take this same precaution if more than one SEEK or RECALIBRATE command is issued without intervening data transfers. Note that reading or writing on unintended portions of the disc can occur if such precautions are not taken.

SET FILE MASK



Bit 0, when set, allows the controller to automatically seek to the next higher or lower cylinder address (depending on bit 3) when a data operation continues through the end of the current logical cylinder. The new track is subjected to disc address and track status verification before any further operation is performed. When bit 0 is clear, the option is prohibited, and any data operation which exceeds the end of the current cylinder is aborted with an end-of-cylinder error status.

Bit 1, when set, indicates that the controller is operating in the cylinder mode. In this mode, the first head address is 0 (the top-most head) and head switching occurs automatically following the last data sector of each track. The head address increases incrementally from 0 to the last head address of the particular disc drive. As each new head is switched in, the verification described in the previous paragraph is performed. The last data sector of the last head address of the current track address is the end of the logical cylinder.

When bit 1 is clear, the controller is operating in the surface mode, where the head address never changes. The last sector of the current track address is the end of cylinder. If bit 0 is set (incremental/decremental seek allowed), a data operation which exceeds the end of the cylinder will continue at the next higher/lower cylinder address (subject to address and track status verification).

When bit 2 is set, the controller is allowed to automatically seek to previously initialized spare tracks when a defective track (that is, one which has been initialized defective) is encountered. (The entire spare track algorithm will be described later.) If bit 2 is clear, the automatic sparing will not occur and a defective track error status will be reported to the interface.

Bit 3 operates in conjunction with bit 0 and determines whether an automatic end-of-cylinder seek will be to the next higher or lower track address. If bit 3 is 0, the next higher track is selected; if it is 1, the next lower track is selected. Note: If bit 0 is 0, bit 3 is not examined.

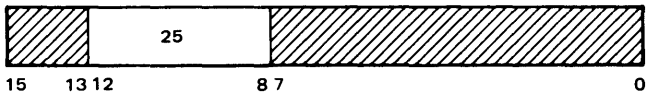
Bits 4 through 7 indicate how many retries are allowed.

The mask sets the mode of operation for the controller. The controller transfers bits 0 – 3 into its "mask" register which is used to control the action taken while transferring data. The entire word is transmitted to the interface via a Set Retry Counter (SRTRY) order. For computers with a data channel separate from the CPU, the retry counter allows the channel program to retry a data transfer in case of an error. The programmer sets the counter with bits 7 through 14 of this command. After the specified number of retries, the interface interrupts the CPU. After sending SRTRY, the controller transmits Set Data Flag (STDFL) to the interface. The controller takes no further action until a command is received or a timeout occurs. At power up, the mask is set to 0 (no-automatic-seek, surface mode, and no sparing).

Because the file mask affects both sparing operations and data transfers that require crossing over the last sector of a particular cylinder, the condition of the file mask always must be known by the operating system. A timeout error will reset the file mask to the "no automatic seek, surface mode, no sparing" state. Also, in multiple CPU environments, one

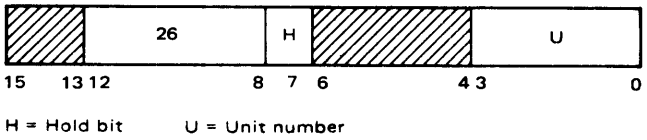
CPU is not given any direct indication that another CPU has changed the file mask (or timed out, since the effect of a timeout error is to disconnect the offending interface and return to polling). Thus it is suggested that directly prior to any data transfer, the SET FILE MASK instruction (as well as ADDRESS RECORD, mentioned previously) be issued to put the file mask in the desired state.

END



This command is used to avoid a timeout if no other command is expected to be outputted from an interface and the controller is waiting for a command from that interface. When the controller accepts this command from an interface, no action is taken except to resume polling. This command should follow any string of commands when they have been completed.

WAKEUP



This command checks if the specified unit is available (attached to current interface or hold bit clear). If not, the command is left pending on the interface and the controller resumes polling of other interfaces.

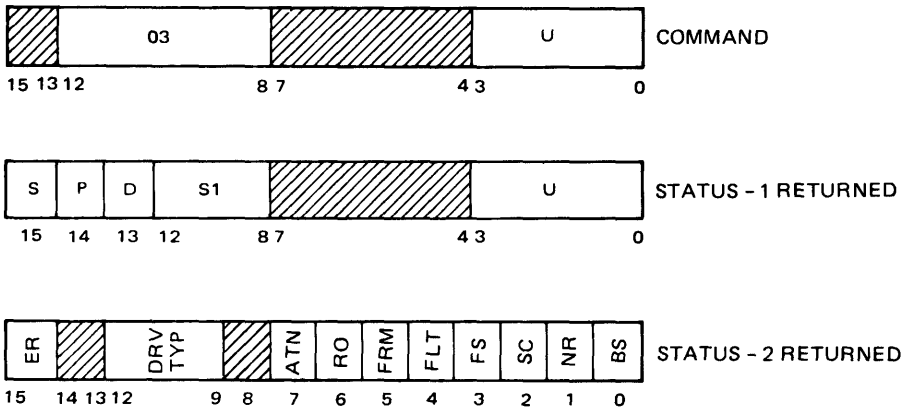
If the unit is available, the status register is set to indicate "unit available" and STDFL is transmitted to the interface. The controller then waits until a command is received or until timeout occurs.

Because the WAKEUP routine is incorporated in all commands that access a disc drive, this command is no longer necessary in multi-CPU systems (if a different CPU issues a command that attempts to access a "held" disc drive, the command will remain pending at the interface until that drive becomes available). It is suggested that if the WAKEUP command is used, a REQUEST STATUS command should follow to determine the condition of the accessed drive prior to its use.

SENSE COMMANDS

Sense commands are included as a means of providing feedback to the operating system as to the condition of the controller, disc drive, or various operations. Included in this group are diagnostic and data recovery commands that expand the versatility of the 13037 controller and enhance the reliability of data transfers. Returned information is accompanied by a STDFL, telling the interface that data has been returned by the controller.

REQUEST STATUS



U — Unit number to which status on last operation applies; if S1 is 37 (drive attention), U is number of interrupting drive. If no unit number is appropriate, U will be zero.

S1 — Encoded termination status (octal).

After receipt of the command, the controller returns two status words to the interface. The first (Status-1) contains information relating to the last operation performed, and the second (Status-2) contains information pertaining to the disc drive addressed in the command word. Any hold bit is ignored, and the First Status bit in Status-2 is cleared by this command after it has been returned. The controller then clears Status-1 and waits for a command from the same interface or a timeout to occur. Note that the unit field of the command word determines the drive that the returned Status-2 word will describe, while the unit field of the Status-1 word relates to that associated with the last operation performed.

Note: The Status-1 word is also transmitted to the interface at the completion of all commands or at an error interrupt (the WRTIO function bus command is used).

The various encoded termination status values in the S1 field are explained below.

00 — NORMAL COMPLETION. This status is transmitted in one of two situations:

a. When command has been fully executed without error.

b. At completion of a REQUEST STATUS command whenever the command immediately follows another REQUEST STATUS command or when it is the first command issued after interface is connected to controller during a polling sequence. For the latter case, the U field will be zero.

01 — ILLEGAL OPCODE. A command word has been received by the controller of which bits 12-8 contain a command code which is not one of controller's command set.

02 — UNIT AVAILABLE. Controller transmits this status after interface has put out a WAKEUP command for a specific drive and that drive has become available.

07 — CYLINDER COMPARE ERROR. During verification of address of sector previous to first sector to be read from or written to, the contents of cylinder address field of that sector do not match contents of controller's cylinder address register. This status is transmitted only after the sequence of events listed below.

a. Addresses do not compare as described above.

b. Controller generates a seek to address in its cylinder address register and head sector address register.

c. Controller again attempts to verify a sector.

d. Addresses still do not compare.

e. The S bit is not set at new track address.

When this status is received, the system should issue a RECALIBRATE command and then retry data transfer sequence.

10 — UNCORRECTABLE DATA ERROR. This status is generated by the error correction circuits and is transmitted in one of three cases:

a. Immediately following a data transfer (or VERIFY) command if error is uncorrectable.

b. In response to a REQUEST SYNDROME command whenever a Possibly Correctable Data Error has proved uncorrectable.

c. During verification of address of sector previous to first sector to be read from or written to, controller is unable to read (verify) any of 16 consecutive sectors without error.

11 — HEAD-SECTOR COMPARE ERROR. Similar to Cylinder Compare Error, including controller's recovery attempt sequence described for that status, except that head and/or sector address field of disc sector does not compare with corresponding field in controller's head sector address register. The system need not issue a RECALIBRATE command when this status is received.

12 — I/O PROGRAM ERROR. Systems containing a programmable data channel separate from CPU may have their interface detect abnormal channel operations and notify controller. At that time, controller will interrupt CPU with this status. An example of such an error might be an inconsistent direction of data transfer (a read command has been transmitted to controller, but channel has been programmed to write).

14 — END OF CYLINDER. A multiple-sector data transfer must continue beyond end-of-logical-cylinder, but file mask will not allow controller to automatically seek to next logical cylinder and continue.

16 — OVERRUN. Detected by interface (read) or controller (write) whenever instantaneous data rate of controller exceeds that of CPU-interface combination. The overrun is reported at end of sector in which it occurred. The contents of that sector, either on disc (write) or in I/O buffer (read) should be considered invalid.

Note: The controller always transfers complete sectors between itself and the disc. If the CPU or data channel wishes to transfer less than a complete sector, it must notify interface (or controller) when the transfer is complete so that subsequent controller requests for data transfer do not cause an Overrun error.

17 — POSSIBLY CORRECTABLE DATA ERROR. This status is generated by the error correction circuits and is transmitted in one of two cases:

a. Immediately following a data transfer (or VERIFY) command if error is possibly correctable.

b. In response to a REQUEST SYNDROME command if error is in fact correctable. In this case, proceed as described in REQUEST SYNDROME command.

20 — ILLEGAL ACCESS TO SPARE TRACK. The same conditions and sequence of events described for a Cylinder Compare Error or Head-Sector Compare Error have occurred, except that S bit is set at new track address. This error usually results from trying to directly access (via a SEEK command) a spare track in active use. The addresses will not compare because of the way in which spare tracks are set up and this status merely differentiates between this situation and other address errors.

21 — DEFECTIVE TRACK. This status is transmitted in one of two situations:

a. During verification of track status of sector previous to first sector to be read from or written to, the D bit is found to be set but File Mask will not allow automatic seeking to a spare track.

b. In the same situation, the File Mask does allow automatic seeking but the address field contains the defective track address (in other words, the D bit was set without assigning a spare track). See the section on SPARE TRACKS and ADDRESS VERIFICATION.

22 — ACCESS NOT READY DURING DATA OPERATION. While in process of transferring data to or from disc, the track center detector in drive detected head motion. The transfer should be retried.

Note: If heads moved during a write operation, the drive will fault and must be manually reset.

23 — STATUS-2 ERROR. The controller is unable to complete a command due to some condition in disc drive. The Status-2 word may be examined for reason. Examples of Status-2 Errors are:

a. An Initialize command, but Format switch is off or Read Only switch is on.

b. A command is issued to a drive which is Not Ready (heads unloaded) or for which a Drive Fault has occurred.

26 — ATTEMPT TO WRITE ON PROTECTED TRACK. During verification of track status of sector previous to first sector to be written to using a Write command, the P bit is found to be set and the Format switch is off.

27 — UNIT UNAVAILABLE. This status is returned whenever the U field of the command word is greater than 12 (octal).

Note: The interface busy bit is false whenever this status is returned.

37 — DRIVE ATTENTION. Controller generates an interrupt (issues STINT) to interface which last accessed drive that is requesting attention (or interface 0 if this is first attention after power-on or hard clear) whenever:

a. Drive is requesting attention.

b. Interface does not have a subsequent command pending in its command buffer excepting Wakeup, which is ignored here.

c. Interface flag INTOK (Interrupt O.K.) is set, thereby allowing attention interrupts.

Briefly, conditions causing a drive to request attention are:

a. Seek completion.

b. Drive becomes ready (heads load).

c. Drive becomes not ready (heads unload).

d. Seek check.

e. Drive Fault.

S — Spare track

P — Protected track

D — Defective track

S2 — Unit status

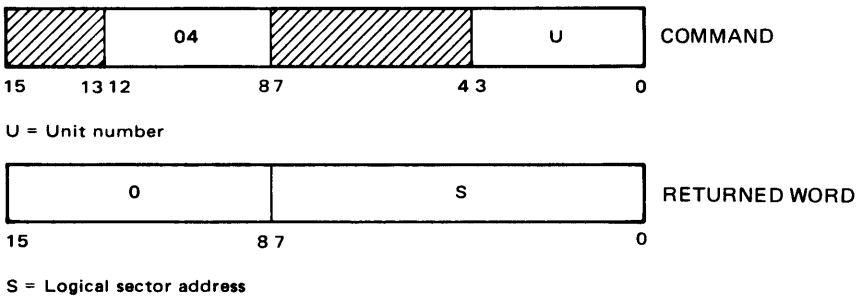
Bit

0* — Drive busy
1* — Drive not ready
2* — Seek check
3 — First status
4* — Fault
5 — Format
6 — Protected (drive cannot write)
7 — Attention
8 — (Reserved)
9-12 — Encoded drive type (used by controller to determine last available head and sector) as described below.
15 — Status-2 error (true if any bit marked * is true)

Drive types:

0 - 7906 (4 heads, 48 sectors)
1 - 7920 (5 heads, 48 sectors)
2 - 7905 (3 heads, 48 sectors)
3 - 7925 (9 heads, 63 sectors)

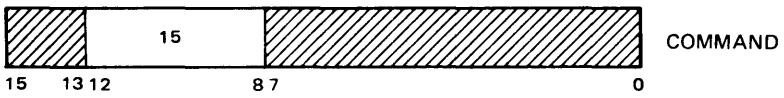
REQUEST SECTOR ADDRESS



After receipt of the command, the controller returns the logical address of the sector currently passing under the heads of the specified unit. The existing hold bit is not checked or altered. At completion, the controller waits for the next command (or a timeout).

Besides use in wraparound read operations, this command also can be used to allow the CPU to perform other operations while waiting for the desired sector to pass underneath the accessed disc drive's heads (348 microseconds are required for each sector to pass by the heads, allowing as much as 16.3 milliseconds (21.9 milliseconds for the 7925 disc drive)for the CPU to do other operations). However, users are cautioned in that improper use of this command can create timing conflicts that unnecessarily delay access to the desired sector for subsequent data transfer.

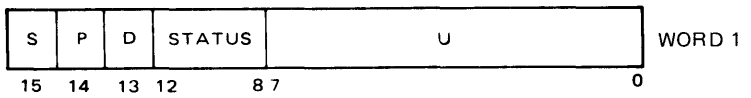
REQUEST SYNDROME



To provide greater reliability in data transfer through the 13037 controller, an error correction process (involving both hardware and firmware) is included that can be invoked by the REQUEST SYNDROME command. This command is used when errors have been detected by the controller after transferring data from the disc drive to the computer. The command may be issued after a READ, COLD LOAD READ, READ WITH OFFSET, VERIFY, or READ WITHOUT VERIFY command which terminates with a Status-1 word indicating "Possibly Correctable". The software correction routine should not try to correct the preamble or postamble since these areas have not been transmitted to the data buffer in the computer (if used following a VERIFY command, no attempt should be made to correct data, since none has been transmitted).

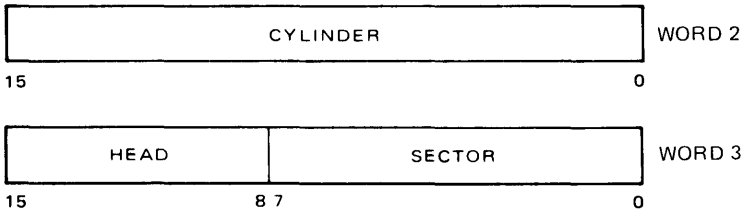
This command should only be issued if the Status-1 field immediately following a data transfer (or VERIFY command) contains Possibly Correctable Error status. False results will be obtained if this command is issued at any other time (including after a previous REQUEST SYNDROME command). Figure 10-2 outlines a suggested use of the REQUEST SYNDROME command (the retry counter indicated on the flowchart can be that of the interface, or a scratch pad register within the operating system).

This error correction routine will provide all of the information needed to correct a "correctable" data error. However, the operating system must use the returned displacement to align the correction mask properly with the appropriate section of the erroneous data. Seven words are returned, with the following significance:

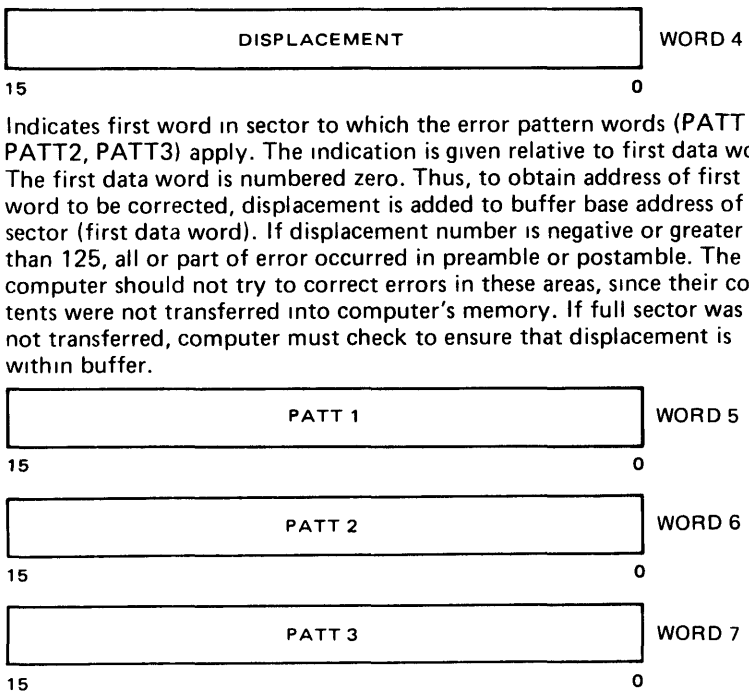


S = Spare track
P = Protected track
D = Defective track
U = Unit number

Status – May be "Correctable" or "Uncorrectable" (Ø17 or Ø1Ø octal) at this point. If uncorrectable, ignore displacement and pattern words. If correctable (Ø17), correction data is available in displacement and pattern words.



Cylinder, Head, Sector – The logical address of sector in which error occurred.



Displacement – Indicates first word in sector to which the error pattern words (PATT1, PATT2, PATT3) apply. The indication is given relative to first data word. The first data word is numbered zero. Thus, to obtain address of first word to be corrected, displacement is added to buffer base address of sector (first data word). If displacement number is negative or greater than 125, all or part of error occurred in preamble or postamble. The computer should not try to correct errors in these areas, since their contents were not transferred into computer's memory. If full sector was not transferred, computer must check to ensure that displacement is within buffer.

Three words, PATT1, PATT2, and PATT3, are generated by the controller for error correction. These words are "exclusive-or'ed" with the data word errors, beginning with the word indicated by the displacement number. Be sure that the displacement refers to words actually present in the data buffer (see above description entitled "Displacement"). Performance of the "exclusive-or" function of the computer corrects the errors. Figure 10-3 outlines a suggested method of error correction.

The command will complete in less than 700 microseconds. When the process is complete, the controller addresses the next logical sector and waits for a command or until timeout occurs. If the transfer was not complete, the interface may issue a READ without an intervening SEEK or ADDRESS RECORD to continue the transfer. Polling is not resumed when REQUEST SYNDROME is completed; after command completion, the controller waits for a new command (or a timeout).

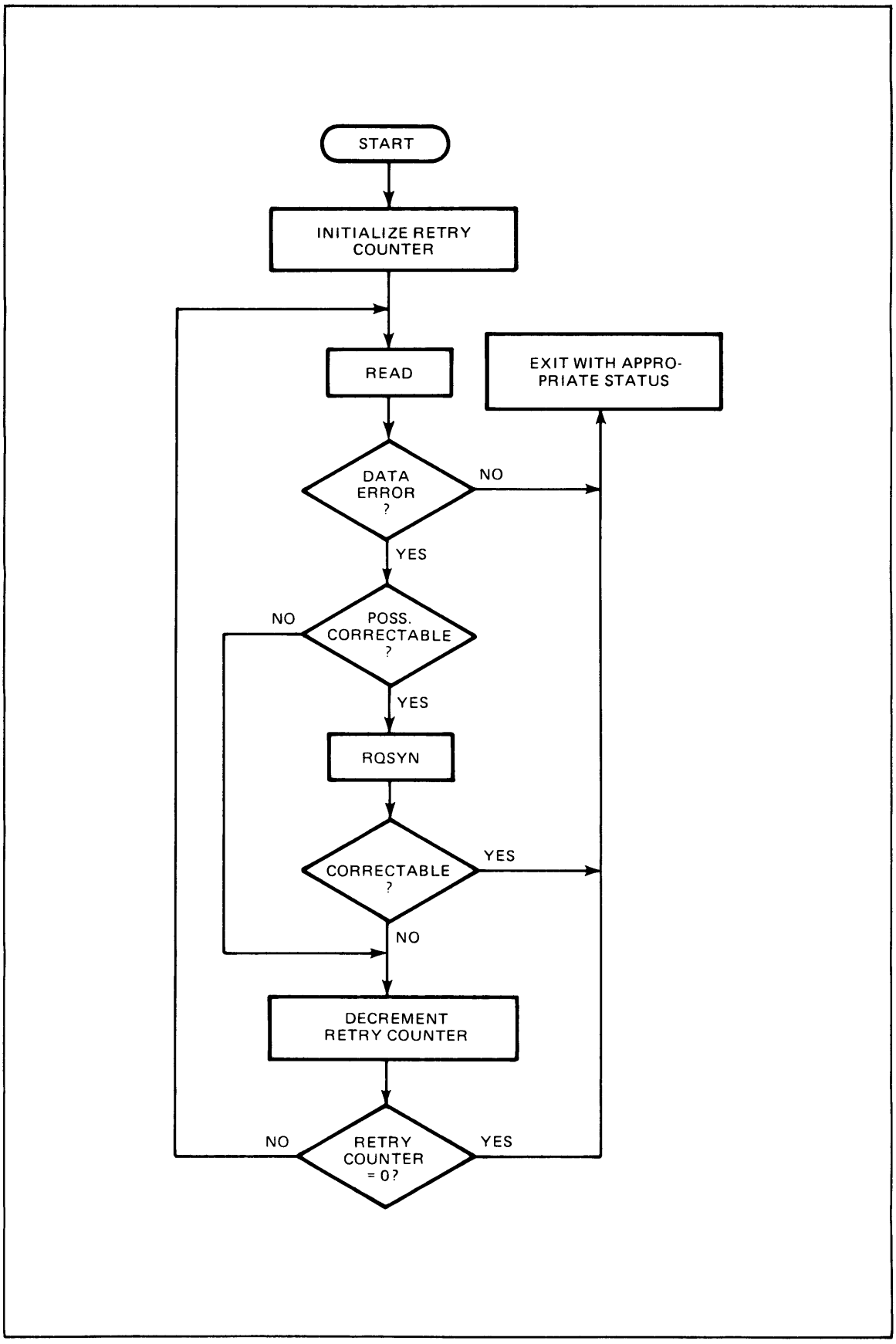


Figure 10-2. Suggested Request Syndrome Routine

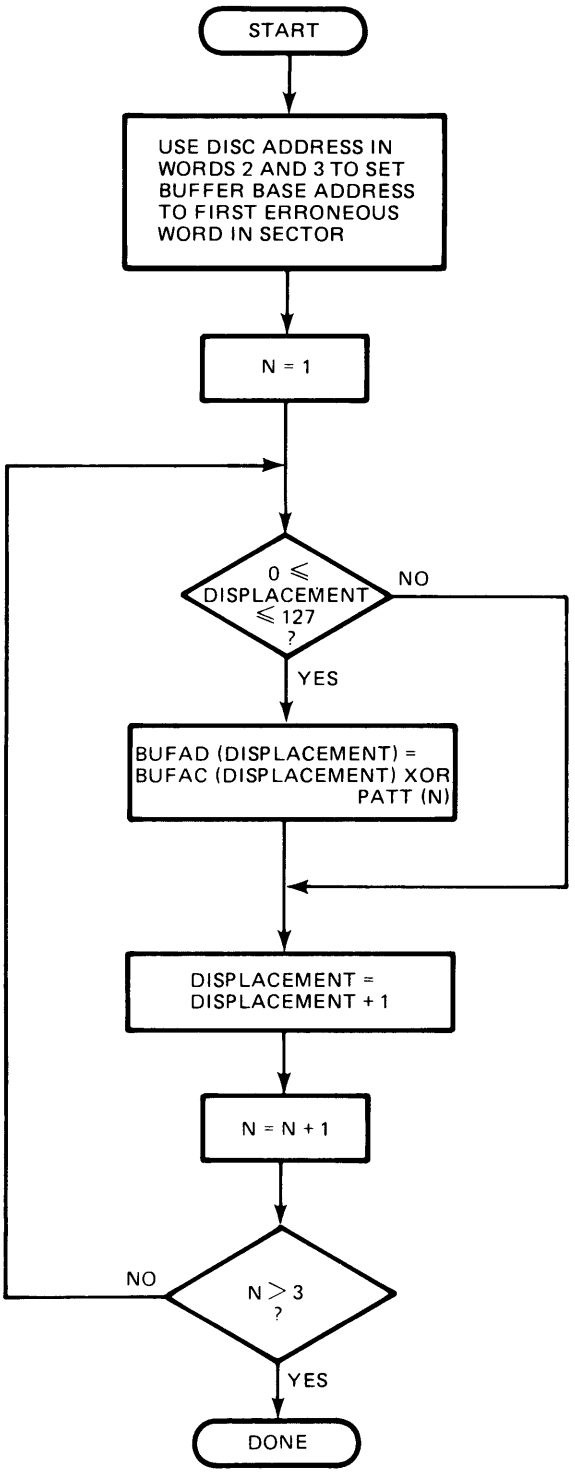
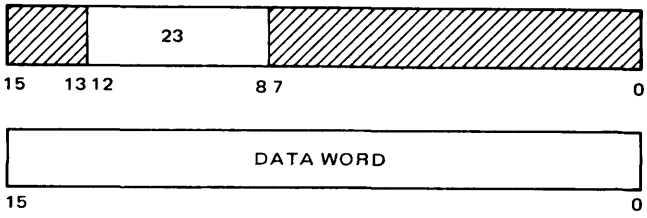


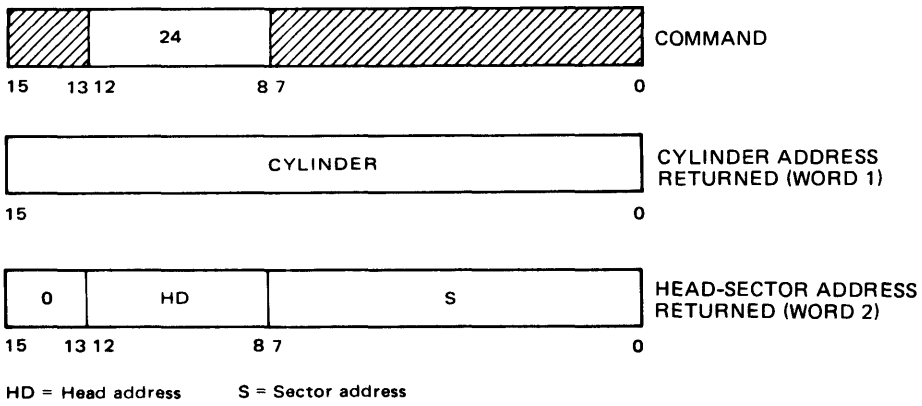
Figure 10-3. Suggested Error Correction Routine

LOAD TIO REGISTER



Included as another diagnostic tool, the LOAD TIO REGISTER command allows the CPU to accept information and write it into the interface's TIO register much as the Status-1 word is automatically written into that register after every controller operation. The controller requests a data word by issuing STDFL. This data word is then written into the TIO (status) register on the interface by a Write Interface Status Register (WRTIO) order. The controller then transmits Request Service (RQSRV) to the interface and waits for a new command (or timeout).

REQUEST DISC ADDRESS



The controller returns two words in the order and format of the address words passed in a SEEK command. The command may be used at any time, but is most useful following a multiple-sector I/O or VERIFY command which aborted with an error. This command allows the operating system to determine where the abort occurred. After completion, the controller then transmits Request Service (RQSRV) to the interface and waits for a command or until timeout occurs.

The returned address is that of the current disc address stored in the controller. This will be the address of the current sector if a data error occurred. or the address of the next logical sector if no data error occurred.

Note that if either word is not taken by the CPU within 1.8 seconds after the command is accepted, a timeout will occur.

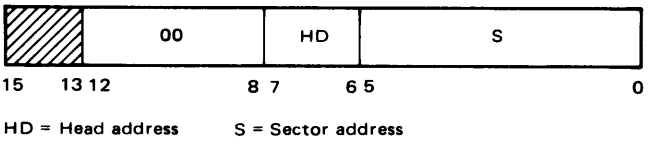
READ COMMANDS

Read commands transfer information from a disc drive to the computer. On all read commands (except READ FULL SECTOR), the controller examines correction and cyclic code words to check the validity of each record area. Previous to all operations (except READ FULL SECTOR and READ WITHOUT VERIFY), the sector prior to that in which the transfer begins is checked to see if the written address (on the disc) agrees with that in the controller register. On multiple sector data transfers, if a track boundary is crossed another address verification takes place. Such address verification is used by the controller to determine if sparing operations need to be performed. Sparing will occur, if enabled and necessary, only for COLD LOAD READ, VERIFY, READ, READ WITH OFFSET, and (only when a track boundary is crossed) READ WITHOUT VERIFY commands.

Because the controller always transfers complete sectors (128 words normally, 138 words for READ FULL SECTOR), any error indications will occur at the end of that sector. Note that EOD can be asserted at any time during a sector if only part of that sector is to be read.

Normal read transfers result in STDFL and RQSRV being sent to the interface. Data errors cause DVEND and RQSRV to be sent to the interface. STINT is sent to the interface on any other error condition. Because some interfaces combine DVEND, STDFL, and/or STINT, the operating system should inspect status on apparent completion to check the state of the preceding data transfer.

COLD LOAD READ



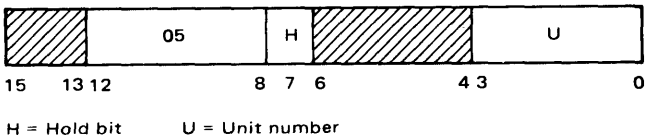
The controller first checks that unit 0 is available (hold bit clear) or attached to the current interface. If not, it resumes polling until unit 0 is available, then executes the command.

After issuing a SEEK to unit 0, cylinder 0 and the head and sector specified in the command word, and waiting for seek completion, the controller sets the FILE MASK to Sparing Enabled, Incremental Seek Not Allowed, and Surface Mode. The controller also transmits a 0 retry count to the interface and then begins reading, starting with the sector and head addressed in the command word.

The controller continues to transfer 128 words per sector until the interface sets End of Data (EOD) or the end-of-logical-cylinder is reached. The last sector does not have to be completely transferred. At the end of each sector, checks are made for overrun (detected by the interface) and data errors. If any errors are detected, the operation will be aborted regardless of End of Data (EOD). Sparing will occur if it is necessary.

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun or data error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

READ



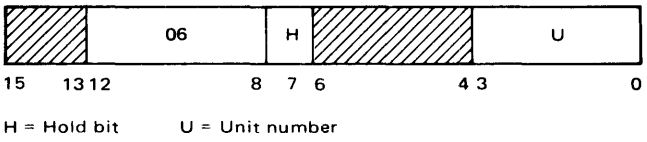
The controller first checks that the specified unit is available (if the hold bit is set, the controller will resume polling, leaving the command pending at the interface). The following description assumes the unit is available.

After sparing (if necessary and enabled) and waiting for seek completion, the controller begins reading from (1) the sector last addressed by a SEEK command; (2) the sector last addressed by an ADDRESS RECORD command; or (3) the sector following the last one transferred, whichever occurred most recently.

The controller continues to transfer 128 words per sector until the interface sets End of Data (EOD). The last sector does not have to be completely transferred. At the end of each sector, checks are made for overrun (detected by the interface) and data errors. If any errors are detected, the operation will be aborted regardless of End of Data (EOD). Sparing will occur at the start of any track if necessary and enabled.

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun or data error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

READ FULL SECTOR



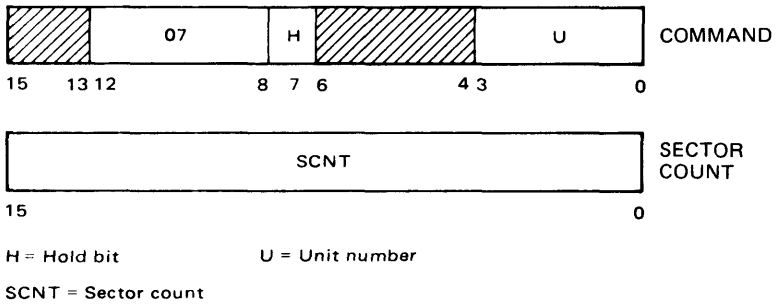
The controller first checks that the specified unit is available (if the hold bit is set, the controller will resume polling, leaving the command pending at the interface). The following description assumes the unit is available.

After waiting for seek completion (without sparing), the controller begins reading from (1) the cylinder, head and sector last addressed by a SEEK command, (2) the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command, or (3) the sector following the last sector transferred, whichever occurred most recently.

The controller then transfers 138 words per sector (sync word, cylinder address, head-sector address, 128 data words, CRC word, and 6 ECC words) to the computer until the interface sets End of Data (EOD). The last sector does not have to be completely transferred. At the end of each sector, a check is made for overrun (detected by the interface). If an error is detected, the operation will be aborted regardless of End of Data (EOD).

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun error, Device End (DVEND) and Request Service (RQSRV) are sent to the interface. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

VERIFY



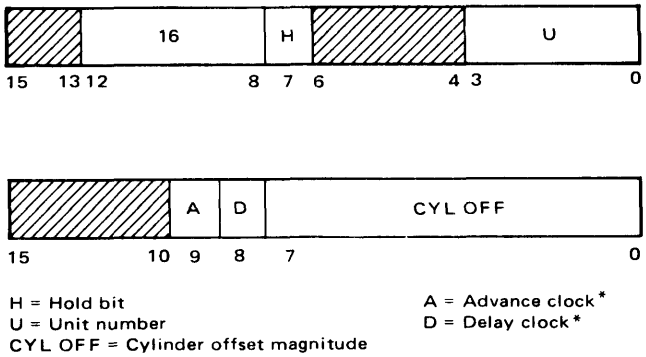
The controller first checks that the specified unit is available (if the hold bit is set, the controller will resume polling, leaving the command pending at the interface). The following description assumes the unit is available.

After acceptance of the command word, the controller requests the sector count (SCNT) by issuing STDFL to the interface. Starting with the currently addressed sector, the controller reads from the disc without passing data to the computer. At the end of each sector, a check is made for data errors. If any errors are detected, the operation will be aborted regardless of sector count word. The controller continues to scan sectors until SCNT has decremented to zero. The SCNT designates how many sectors are to be verified. If SCNT is zero, the interpretation is 65,536 (decimal) sectors.

After sparing (if necessary and enabled) and waiting for seek completion, the controller begins reading (without transmitting to the interface) from (1) the sector last addressed by a SEEK command; (2) the sector last addressed by an ADDRESS RECORD command; or (3) the sector following the sector last transferred, whichever occurred most recently. Sparing will occur at the start of any track if necessary and enabled.

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On data error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

READ WITH OFFSET



* 13037B Disc Controllers containing 13037-60028 Device Controller PCA's ignore these bits.

The controller first checks that the specified unit is available (if the hold bit is set, the controller will resume polling, leaving the command pending at the interface). The following description assumes the unit is available.

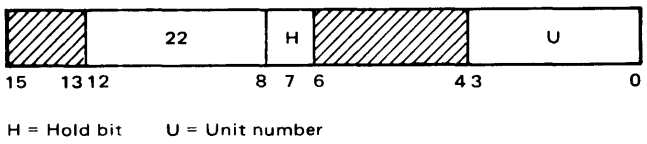
This command performs like a normal read (including termination sequences) except that the heads are moved off of track center by an amount proportional to an offset parameter word requested from the computer before data transfer begins. The controller requests this parameter by sending STDFL to the interface. Upon receipt, RQSRV is sent. Direct memory access (DMA) should not be activated for the data transfer portion of the command until one or both of these signals are received on the interface.

The controller transmits the cylinder offset to the selected disc drive, and may (for 13037 Disc Controllers having serial prefixes before 1815) also advance or delay the separator clock 10 nanoseconds with respect to the data. A cylinder offset of zero is on the track center. Offset parameters in the range of +63 to −63 move the heads off of track center by incremental amounts characteristic of the unit specified. (A negative parameter is in sign magnitude form.) All offsets are removed after normal command completion or error terminations.

This command is usually used only in error recovery situations when normal re-reads and REQUEST SYNDROME commands have failed. Since each offset operation requires a minimum of 1.5 milliseconds to complete, the target sector will have passed under the heads by the time the offset is complete, thus requiring an extra rotation of the disc. A similar amount of time is required at the end of the command to restore the heads to track center.

Spare tracks cannot be read with offset. The process of seeking to the spare track causes the disc drive to cancel the offset, and the controller cannot restore it. A similar situation occurs if a transfer requires an automatic incremental or decremental seek at the end of a logical cylinder.

READ WITHOUT VERIFY



The controller first checks that the specified unit is available (if the hold bit is set, the controller will resume polling, leaving the command pending at the interface). The following description assumes the unit is available.

After waiting for seek completion (without sparing), the controller begins reading from (1) the cylinder, head and sector last addressed by a SEEK command, (2) the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command, or (3) the sector following the last sector transferred, whichever occurred most recently.

This command performs like a normal read, but does not verify the preceding sector. Therefore, no address checking or sparing operations occur unless a track boundary is crossed during the operation. This command is provided for error recovery or, in conjunction with the REQUEST DISC ADDRESS command, wraparound read operations (the latter is discouraged unless extremely fast CPU's are being used).

WRITE COMMANDS

Write commands transfer information from the computer to the controller for subsequent writing onto the disc. Except for the WRITE FULL SECTOR command, the controller will append the preamble and postamble to the data field (the computer must supply 138 words of information — the preamble, 128 data words, and the postamble — during WRITE FULL SECTOR commands; the 12 word zero sync field, however, is supplied by the controller).

128 words per sector (138 words per sector for WRITE FULL SECTOR commands) are transferred until the interface sets EOD or until the controller is unable to continue the transfer due to a drive error, interface error, or condition set in the file mask. Because the controller always processes complete sectors, normal completion or any errors that occur will be reported at the end of the current sector. In the event that EOD is asserted prior to the end of a sector, the controller repeatedly will write the last transmitted word into the remainder of the sector data field (and through the postamble during WRITE FULL SECTOR commands).

STDFL and RQSRV are sent to the interface on normal completion of write commands. Overrun errors cause DVEND and RQSRV to be sent. Other errors will cause STINT to be sent. In all cases, the controller waits for a subsequent command or a timeout to occur.

WRITE



H = Hold bit U = Unit number

The controller accepts data from the computer and writes the addressed sector (preamble, data, and postamble) after verifying the previous sector. The command will not be executed if the surface is protected. If the P-bit is set, the Format switch must also be on.

The controller first checks that the specified unit is available. If the hold bit is set, the command is left pending on the interface and the controller resumes polling. The following description assumes the unit is available.

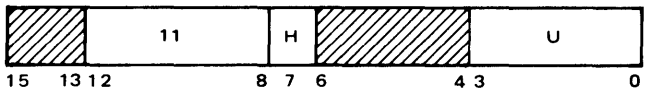
After sparing (if necessary and enabled) and waiting for seek completion, the controller begins writing on (1) the sector last addressed by a SEEK command; (2) the sector last addressed by an ADDRESS RECORD command; or (3) the sector following the last sector transferred, whichever occurred most recently.

On all data transfers out of the computer, the controller will request 128 words of data. If the computer transfers less, the controller will repeatedly write the last transmitted word into the remainder of the sector data field. If the controller fills the sector in this manner and then finds that the computer has more data available, it will flag an overrun error and terminate the operation. (Overrun is detected by the controller.) Normally, the controller continues to transfer 128 data words per sector until the interface sets End of Data (EOD). At the end of each sector, a check is made for overrun or a drive error. If an error is detected, the operation will be aborted regardless of End of Data (EOD). Sparing will occur at the end of any track if necessary and enabled.

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

The operation will be aborted whenever a track is encountered which has been flagged protected (unless the Format switch is on), or if the surface is protected by the disc drive PROTECT (READ ONLY) switch(es).

WRITE FULL SECTOR



H = Hold bit U = Unit number

This command is like a write except that the computer must pass the sync word, address words, and postamble to the controller in addition to the data field.

The controller first checks that the specified unit is available. If the hold bit is set, the command is left pending at the interface and the controller resumes polling. The following description assumes the unit is available.

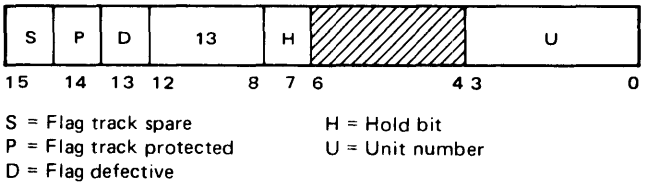
After waiting for seek completion (without sparing), the controller begins writing on (1) the cylinder, head and sector last addressed by a SEEK command; (2) the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command; or (3) the sector following the last sector transferred, whichever occurred most recently.

The controller will request 138 words per sector (sync word, cylinder address, head-sector address, 128 data words, CRC word, and 6 ECC words). If the computer transfers less, the controller will repeatedly write the last transmitted word into the remainder of the sector. If the controller fills the sector in this manner and then finds that the computer has more data available, it will flag an overrun error and terminate the operation. (Overrun is detected by the controller.) Normally, the controller continues to transfer 138 words per sector until the interface sets End of Data (EOD). At the end of each sector, a check is made for overrun or a drive error. If an error is detected, the operation will be aborted regardless of End of Data (EOD).

On normal completion, set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

The operation will be aborted if the FORMAT switch on the disc drive is off, or if the surface is protected by the disc drive PROTECT (READ ONLY) switch(es).

This command is intended only as a diagnostic tool. In any case, it is strongly recommended that any multiple sector transfers not cross a track boundary since all address verification and track status checks are off.



On receipt of the command word, the controller checks that the surface is not protected by the disc drive PROTECT (READ ONLY) switch(es) and that the FORMAT switch on the drive is set to ON before executing the command. The controller then begins requesting data from the computer and writes 128 data words on the addressed sector without verifying the preceding sector. Data transfer continues until the interface sets End of Data (EOD).

The controller first checks that the specified unit is available. If the hold bit is set, the command is left pending at the interface and the controller resumes polling. The following description assumes the unit is available.

After waiting for seek completion (without sparing), the controller begins writing on (1) the cylinder, head and sector last addressed by a SEEK command; (2) the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command; or (3) the sector following the last sector transferred, whichever occurred most recently.

On all data transfers out of the computer, the controller will request 128 words of data. If the computer transfers less, the controller will repeatedly write the last transmitted word into the remainder of the sector data field. If the controller fills the sector in this manner and then finds that the computer has more data available, it will flag an overrun error and terminate the operation. (Overrun is detected by the controller.) Normally, the controller continues to transfer 128 data words per sector until the interface sets End of Data (EOD). At the end of each sector, a check is made for overrun or a drive error. If an error is detected, the operation will be aborted regardless of End of Data (EOD).

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

Bits 13, 14, and 15 of the command word are used to flag the track defective, protected, or spare. Subsequently, when a data transfer (or VERIFY) operation is attempted on a track so marked, the status of the track last accessed by that operation will appear in bits 13-15 of STATUS-1 word. It is the responsibility of the system to ensure that all sectors on a track have the same status.

If the D bit is set, the track is considered defective and sparing will occur if required and enabled. The only drive operations allowed on a track so marked are READ FULL SECTOR, READ WITHOUT VERIFY, INITIALIZE, and WRITE FULL SECTOR. The latter two will not preserve track status unless specifically directed to do so.

If the P bit is set, a write operation will only be allowed on that track if the FORMAT switch is on; track status is preserved. INITIALIZE or WRITE FULL SECTOR will also be allowed if the FORMAT switch is on, but will not preserve track status unless specifically directed to do so.

If the S bit is set on a track, a spare track is in active use. Data operations including VERIFY but excepting INITIALIZE, WRITE FULL SECTOR, READ FULL SECTOR, and READ WITHOUT VERIFY will not be allowed on a track so marked unless access is made through its corresponding defective track. INITIALIZE and WRITE FULL SECTOR will not preserve track status unless directed to do so.

It is strongly recommended that any multiple sector transfers using the INITIALIZE command not cross a track boundary, since all address verification and status checks are off. In addition, a track boundary *must* not be crossed during a multiple sector transfer whenever tracks are being flagged spare or defective since the automatic track sparing algorithm may not work.

CONTENTS

Section 11

1.0	Scope	4
2.0	Theory of Operation	4
3.0	HP-IB Module	8
4.0	Buffer Module	29
5.0	Write Module	41
6.0	Read Module	50
7.0	13037 Port	59

HEWLETT-PACKARD CO.

ER	48	22	46	60	63
Sect A					

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	As Issued	4-18-78	lk/
B	Add Model No. 12745D C0480248	10-08-84	PK/

Model No.	12745 A/D	Stock No.	
Title	IMS		
Description	HP-IB/13037 I/F	Date	4-18-78
By		Sheet No.	1 of 68
Supersedes		Drawing No.	A-12745-90004-1

M0353

HEWLETT-PACKARD CO.

12745A/D INTERNAL MAINTENANCE SPECIFICATION

LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL 12745A/D	STK NO
HP-IB/13037 I/F	
BY	DATE 4-18-78
APPD	SHEET NO 2 OF 68
SUPERSEDES	DWG NO A-12745-90004-1

CONTENTS

(1) Scope

(2) Overview

(3) HPIB Module

(4) Buffer Module

(5) Write Module

(6) Read Module

(7) 13037 Port

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 3 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

1.0 SCOPE

This document includes a detailed gate level description of the 12745. Its intent is to provide an understanding of the 12745 that is sufficient for troubleshooting or any future design changes. Included is an overview of the product. For a more complete overview and description of the command set, the reader is referred to the 12745 External Reference Specification which can be found in the 12745-90901 Installation & Service Manual. Description of the 13037 operation is beyond the scope of this document. It is described only to the extent necessary to provide a complete hardware view of the 12745.

2.0 THEORY OF OPERATION

The 12745 Interface provides two main functions. These are the ability to transfer the 13037 controller commands, status, and data information via the HPIB and to provide a full sector data buffer that may be used in a burst transfer mode.

To perform these functions, five distinct logic modules are used (See Figure 0). Each module provides a specific portion of the total function. In general, intermodule communication occurs using asynchronous handshake. The internal operation of each module is either asynchronous, synchronous or both, depending upon the particular function involved. The following will give an overview of each module's operation.

2.1 HPIB MODULE:

The HPIB module consists of two major sections. One provides the proper handshake for data or commands coming to or from the 12745 over the HPIB. The other section interprets commands coming over the bus and translates them into control lines that govern the

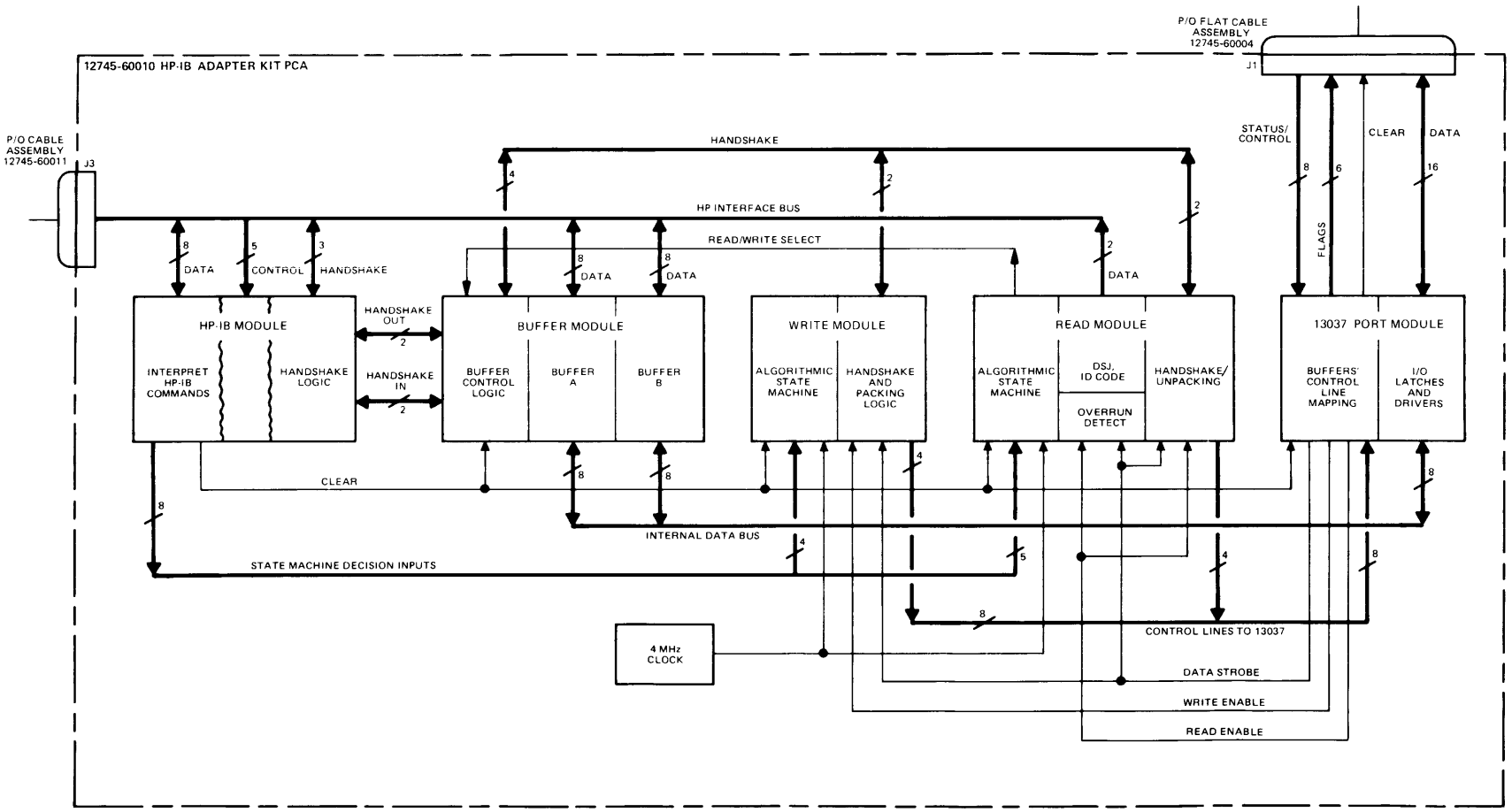


FIGURE 0 BLOCK DIAGRAM

HEWLETT PACKARD

operation of the other modules.

The HPIB module conforms to a subset of IEEE Standard 488-1975. In addition, the interface conforms to the Amigo HPIB protocol. for further information consult references 1, 2 or 3.

2.2 BUFFER MODULE:

The purpose of the buffer is two fold. It provides operation in a high speed data transfer mode at less than the controller's 937 KBYTE Rate, and also allows slow speed transfers on a sector at a time basis. The buffer itself consists of two 256 by 9 bit arrays called buffers A and B. The buffering scheme is bi-directional, i.e., it handles both HPIB to controller and controller to HPIB transfers.

The buffers are structured so that one is available for accepting data while the other can be sourcing any data it might contain. This process is termed "double buffering". When the accepting side is full and the sourcing side has been depleted, the buffers change roles and the transfer continues. The buffers are organized in bytes, requiring packing and unpacking on the controller side but compatible with the byte oriented HPIB. The ninth bit in each buffer is used to tag the last byte in a data transfer.

The actual read and write buffer operations are performed by asynchronous handshake and timing circuits. The three wire handshake of the HPIB is converted into a two wire handshake going to the buffer. A similar handshake is derived from the controller signals.

2.3 WRITE MODULE:

The write module contains logic that sets up data transfers to the controller. Also, upon receipt of a strobe signal from the controller,

it handshakes data out of the buffer.

The module is comprised of two primary divisions. The first is the algorithmic state machine. Using a set of input command signals, it cycles through a series of states, branching as appropriate for the inputs. The decision inputs are based mainly on the state of the HPIB module as determined by the previous HPIB primary and secondary commands. The result of these branching decisions is a series of output control lines. These control lines direct the remainder of the write module and provide flags that are sent to the 13037 port. The balance of the write module handshakes data (or commands) out of the buffer and packs it into the 16 bit output latch at the 13037 port.

2.4 READ MODULE:

Like the write module the read module contains an algorithmic state machine. Its input control lines are also derived mainly from the primary and secondary commands of the HPIB module. Besides sending flags to the 13037 port, the output control lines govern three groups of logic within the module. The first handles the unpacking of controller data and the handshaking of it into the buffer. The second is used to detect if the buffering is fast enough to stay ahead of the controller. If not, an error condition will be signaled to the 13037. The other set of logic within the read module handles the sourcing and handshake of information other than data or status onto the HPIB. This information, identity code and device specified jump, will be explained in Section 7.

2.5 13037 PORT:

The 13037 port is the final interconnect between the other modules and the edge connector going to the controller. The data output consists of a 16 bit bi-directional bus. Latches are used to hold data while packing or unpacking the 16 bit words. There is a group

of eight control and status lines coming from the controller. These are decoded to provide control lines within the module. In the idle mode only the "select" control line is monitored. When not busy, the controller polls through the possible eight CPU numbers. Upon matching numbers with the interface in question, a "select" occurs. At this time the internal input control lines are examined to determine if the controller wishes to perform a function. Also after "selection" the output control lines are enabled so the controller can examine any pending requests or information from the interface. When finished the CPU is "deselected" and all port activity is curtailed (except for polling).

The 13037 transmits data at a rate of 468 K words/sec. and control signals can switch much more rapidly. Because of transmission lines effects, it is necessary to provide proper impedence termination. (Refer to Section 6.2 for termination requirements of mutli CPU systems.)

3.0 HPIB MODULE:

This and each of the following sections will describe the various modules by looking at subsections of the associated schematic page.

3.1 HPIB DATA BUS:

Figure 1 shows the HPIB data bus. The transceivers U161 and U151 isolate the external data bus from the internal. The "S" inputs determine for each bit whether it is in send (S=1) or receive (S=0) mode. The "H" input selects passive (open collector) or active pullup when sending data. Active pullup is selected in each instance of data sourcing. The pullup resistors are provided because the bus is used alternately by three tri-stating sources.

NOTE: Be aware that the entire data bus is inverted!

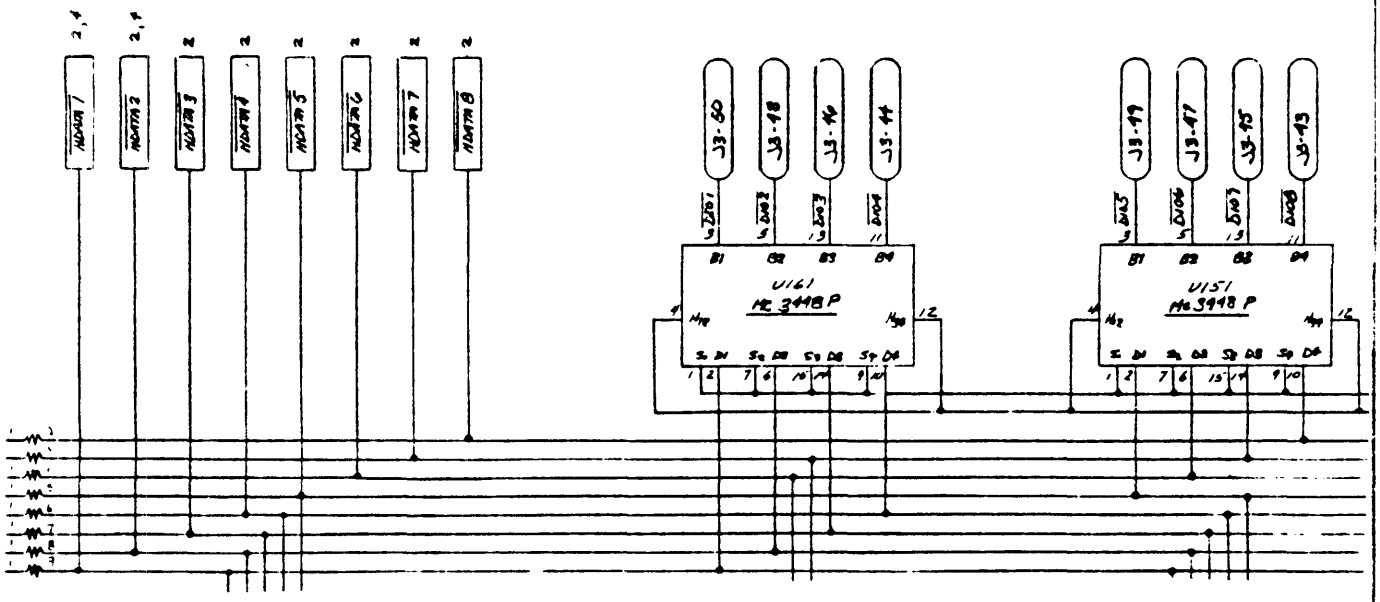


FIGURE 1

3.2 HPIB CONTROL LINES:

Figure 2 shows the HPIB control lines. "SRQ" and "REN" have no effect on the 12745A. "IFC" stands for interface clear. Its effect is to reset the primary state register (See Section 3.5). "ATN" (attention) and "EOI" (end or identify) work in conjunction as follows:

ATN	EOI	
0	0	Data is on the bus.
0	1	The last data byte is on the bus.
1	0	An HPIB command is on the bus.
1	1	The controller is requesting a parallel poll response.

The interface never controls the "ATN" line. When sourcing data it will, however, direct the "EOI" line to signal the end of a transfer. This is done by the "HTEOI" line (HT meaning "HPIB Transfer").

DAV (data valid), RFD (ready for data), and DAC (data accept) form a handshake for data and commands going over the bus. DAV is controlled by the source while RFD and DAC are controlled by the receiver. The

4 tristate inverters of U142 together with the S inputs of U162 allow this handshake to be bi-directional. The actual handshake sequence and timing are discussed in Section 3.9 (a).

The "random logic" in the lower left of figure 2 decodes "ATN" and "EOI" plus "SOURCE". "SOURCE" active indicates the device is in a state that sends data. The outputs of this logic array control the direction of HPIB data ("send data" line) and the direction of "Receiver Handshake" and "Source Handshake". In addition, parallel poll requests are decoded into "Request PP".

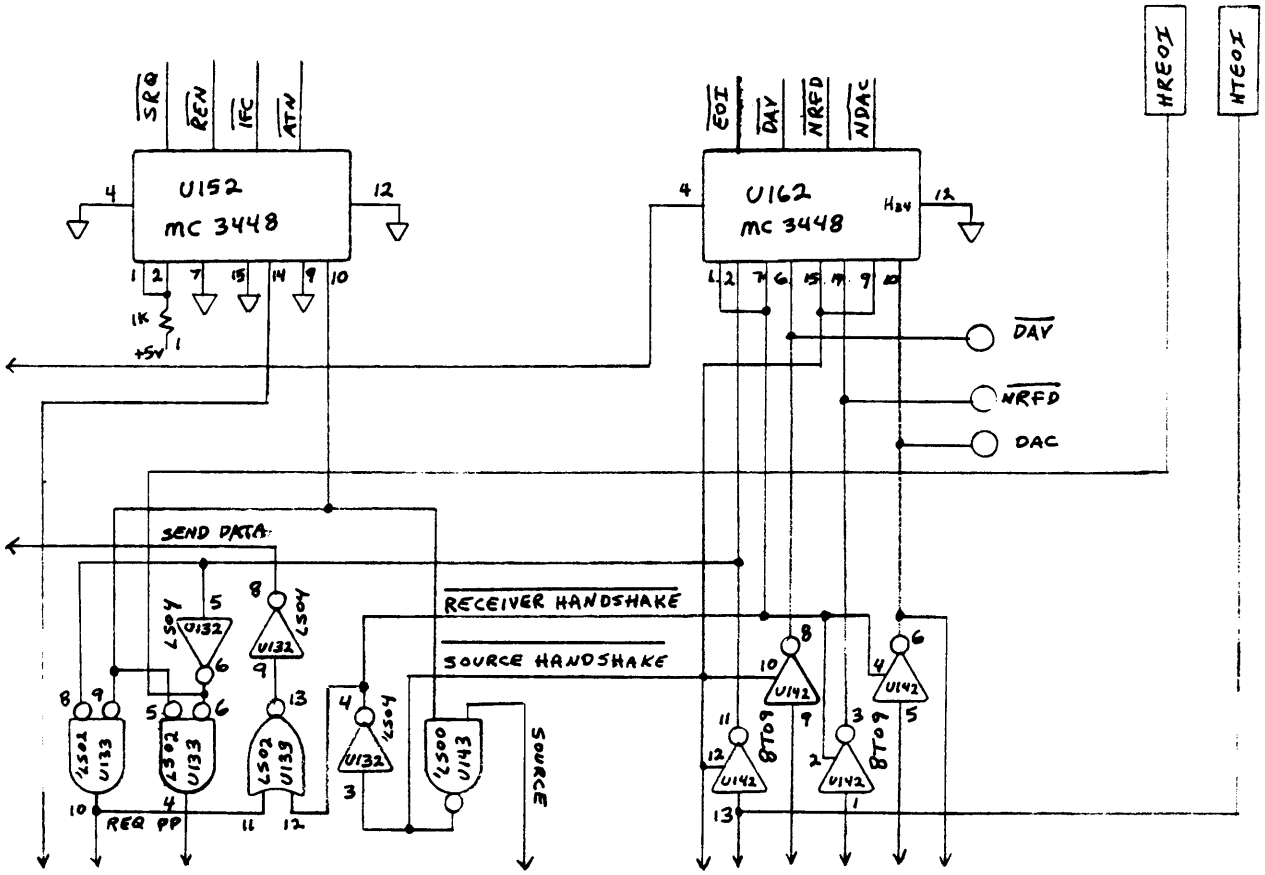


FIGURE 2

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 10 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

3.3 HPIB ADDRESS SELECT:

Figure 3B shows the thumbswitch S2 used to select the HPIB address. The three output lines go to U141 and U131 (figure 3A). U131 is the Parallel Poll Response mapping PROM. When a parallel poll is requested (See Section 3.2) PIN 5 of U143 is active. The actual response (PPoll) goes to U143 Pin 4. When the request and the response are active, U131 is taken out of the tristate mode and one of the eight lines is pulled low, indicating the response to the CPU. The parallel poll response line depends on the HPIB address. The mapping PROM selects the correct line for the given HPIB address.

U141 is an address comparitor. It is used to compare the address portion of an HPIB command with the address selected on the thumb-switch.

NOTE: Because A5, B5, B4, and B3 are tied to +5V, only HPIB address 0-7 are allowed. This is in keeping with the Amigo HPIB convention. When an address compare occurs, the open collector output Z allows the pullup resistor to take the line high. When a miscompare occurs, Z is pulled low.

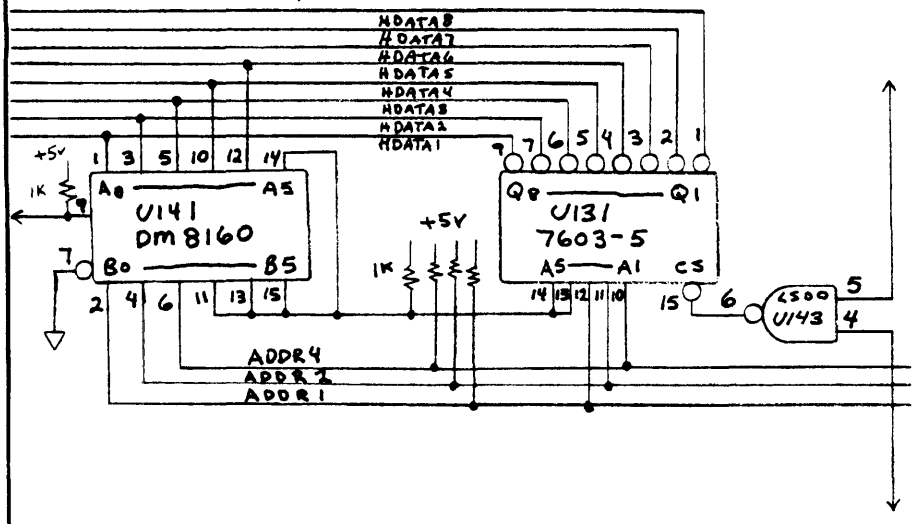


FIGURE 3A

FIGURE 3B

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 11 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

3.4 HPIB COMMAND DECODE:

Figure 4 shows the two mapping PROMS used in HPIB command decoding. U171 decodes the opcode portion of the command. U181 decodes the two bits that specify the command type (A3 and A4). The additional input to the two PROM combination (U181 A5) is the address compare result. (See Section 3.3) The HPIB Command parity is not decoded. U181 decodes command types as follows:

A4	A3	TYPE
0	0	SECONDARY COMMAND
0	1	PRIMARY TALK
1	0	PRIMARY LISTEN
1	1	UNIVERSAL COMMAND

(Remember that these lines are inverted when comparing to uninverted HPIB protocol.)

The additional two inputs to U181 not yet described are active when:

A2: (a) The HPIB primary command address field = 31, corresponding to UNTALK* or UNLISTEN (Table 2 address 00).

(b) A UNIVERSAL CLEAR or SELECTED DEVICE CLEAR is received (Table 2 addresses 0BH and 1BH).

A1: During various clear commands:

(a) UNIVERSAL CLEAR (Table 2 address 0BH)

(b) SELECTED DEVICE CLEAR (Table 2 address 0FH)

The outputs of U181 are all active low. When U181 is not selected, all lines are pulled up by Resistors R19. The chip is selected by "ACDS" (Accept Command Data State, See Section 3.10). When selected the outputs act as follows:

(A) $\overline{\text{"DCLR"}}$ (Device Clear) resets the entire subsystem when certain other conditions are met (See Section 3.7). $\overline{\text{"DCLR"}}$ is activated with a "UNIVERSAL CLEAR" (Table 1 address 0CH), "SELECTED DEVICE CLEAR" (Table 1 addresses 0CH and 1CH).

* Commands and command sequences are described in detail in the 12745A ERS.

(B) $\overline{\text{"MSA"}}$ (My Secondary Address) decodes an address compare on a secondary command. This is used for the Amigo Identify Command. (Table 1 addresses 10H-13H.)

(C) $\overline{\text{"SCG"}}$ (Secondary Command Gate). This signal is active whenever a secondary command is present. On the rising edge of $\overline{\text{SCG}}$, the secondary state register is latched (See Section 3.6).

(D) $\overline{\text{"PCG"}}$ (Primary Command Gate). This signal is active whenever a primary command is present. On the rising edge of $\overline{\text{PCG}}$, the primary state register is latched (See Section 3.5).

(E) $\overline{\text{"UNLTN"}}$ (Unlisten) decodes any unlisten commands (Table 1 address 0AH) and is also active when $\overline{\text{"MTA"}}$ is active (Table 1 addresses 14H and 17H).

(F) $\overline{\text{"MLA"}}$ (My Listen Address). Active upon receipt of an HPIB primary listen (Table 1 addresses 1BH and 18H).

(G) $\overline{\text{"OTA"}}$ (Other Talk Address). Active when another device is addressed to talk (Table 1 addresses 05H or 07H), or when an UNTALK is received (Table 1 addresses 04H or 06H) or when a LISTEN is received (Table 1 addresses 18H and 1BH).

(H) $\overline{\text{"MTA"}}$ (My Talk Address). Active upon receipt of a primary TALK (Table 1 addresses 14H and 17H).

12745 INTERFACE PROM PATTERN HARRIS 7603-5

FUNCTION: PRIMARY COMMAND MAP LOCATION: U181

REVISION: PILOT RUN DATE: 2/8/78

ADDRESS		CONTENTS								CONTENTS		BASE 16		
BASE 10	BASE 16	$\overline{MTA}$	$\overline{OTA}$	$\overline{MLA}$	$\overline{UNLTN}$	$\overline{PCG}$	$\overline{SCG}$	$\overline{MSA}$	$\overline{DCLR}$					
00	00	1	1	1	1	1	0	1	1			F	B	ILLEGAL
01	01	1	1	1	1	1	0	1	1			F	B	ILLEGAL
02	02	1	1	1	1	1	0	1	1			F	B	SELF TEST
03	03	1	1	1	1	1	0	1	1			F	B	NORMAL SECONDARY
04	04	1	0	1	1	0	1	1	1			B	7	OTHER TALK
05	05	1	0	1	1	0	1	1	1			B	7	OTHER TALK
06	06	1	0	1	1	0	1	1	1			B	7	UNTALK
07	07	1	0	1	1	0	1	1	1			B	7	OTHER TALK
08	08	1	1	1	1	0	1	1	1			F	7	OTHER LISTEN
09	09	1	1	1	1	0	1	1	1			F	7	OTHER LISTEN
10	0A	1	1	1	0	0	1	1	1			E	7	UNLISTEN
11	0B	1	1	1	1	0	1	1	1			F	7	OTHER LISTEN
12	0C	1	1	1	1	0	1	1	0			F	6	UNV CLEAR
13	0D	1	1	1	1	0	1	1	0			F	6	SEL DEV CLR
14	0E	1	1	1	1	0	1	1	1			F	7	ILLEGAL
15	0F	1	1	1	1	0	1	1	1			F	7	ILLEGAL
16	10	1	1	1	1	1	0	0	1			F	9	POSSIBLE IDENTIFY
17	11	1	1	1	1	1	0	0	1			F	9	POSSIBLE IDENTIFY
18	12	1	1	1	1	1	0	0	1			F	9	IMPOSSIBLE
19	13	1	1	1	1	1	0	0	1			F	9	POSSIBLE IDENTIFY
20	14	0	1	1	0	0	1	1	1			6	7	IMPOSSIBLE
21	15	0	1	1	0	0	1	1	1			6	7	TALK (ADDR=4)
22	16	0	1	1	0	0	1	1	1			6	7	IMPOSSIBLE
23	17	0	1	1	0	0	1	1	1			6	7	TALK (ADDR.#4)
24	18	1	0	0	1	0	1	1	1			9	7	IMPOSSIBLE
25	19	1	0	0	1	0	1	1	1			9	7	LISTEN (ADDR=4)
26	1A	1	0	0	1	0	1	1	1			9	7	IMPOSSIBLE
27	1B	1	0	0	1	0	1	1	1			9	7	LISTEN (ADDR.#4)
28	1C	1	1	1	1	0	1	1	1			F	7	IMPOSSIBLE
29	1D	1	1	1	1	0	1	1	0			F	6	SEL DEV CLR (ADDR=4)
30	1E	1	1	1	1	0	1	1	1			F	7	IMPOSSIBLE
31	1F	1	1	1	1	0	1	1	1			F	7	ILLEGAL

TABLE 1

LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL 12745A/D STK NO

HP-IB/13037 I/F

BY DATE 4-18-78

APPD SHEET NO 14 OF 68

SUPERSEDES DWG NO A-12745-90004-1

12745 INTERFACE PROM PATTERN HARRIS 7603-5

FUNCTION: SECONDARY COMMAND MAP LOCATION: U171

REVISION: PILOT RUN DATE: 2-8-78

ADDRESS		CONTENTS								CONTENTS BASE 16		
BASE 10	BASE 16	$\overline{CLR}$	$\overline{31}$ + UNV	$\overline{CCLR}$	R2	R1	W3	W2	W1			
00	00	1	0	1	1	1	0	0	0		B	8	SELF TEST/$\overline{31}$
01	01	1	1	1	0	0	0	1	1		E	3	LOOP BACK
02	02	1	1	1	1	1	0	0	0		F	8	ILLEGAL
03	03	1	1	1	1	1	0	0	0		F	8	ILLEGAL
04	04	1	1	1	1	1	0	0	0		F	8	ILLEGAL
05	05	1	1	1	1	1	0	0	0		F	8	ILLEGAL
06	06	1	1	1	1	1	0	0	0		F	8	ILLEGAL
07	07	1	1	1	1	1	0	0	0		F	8	ILLEGAL
08	08	1	1	1	1	1	0	0	0		F	8	ILLEGAL
09	09	1	1	1	1	1	0	0	0		F	8	ILLEGAL
10	0A	1	1	1	1	1	0	0	0		F	8	ILLEGAL
11	0B	0	0	1	1	1	0	0	0		3	8	UNV CLR
12	0C	1	1	1	1	1	0	0	0		F	8	ILLEGAL
13	0D	1	1	1	1	1	0	0	0		F	8	ILLEGAL
14	0E	1	1	1	1	1	0	0	0		F	8	ILLEGAL
15	0F	1	1	0	1	0	0	0	0		D	0	DSJ/SECONDARY CLR
16	10	1	1	1	1	1	0	0	0		F	8	ILLEGAL
17	11	1	1	1	1	1	0	0	0		F	8	ILLEGAL
18	12	1	1	1	1	1	0	0	0		F	8	ILLEGAL
19	13	1	1	1	1	1	0	0	0		F	8	ILLEGAL
20	14	1	1	1	1	1	0	0	0		F	8	ILLEGAL
21	15	1	1	0	0	1	1	1	0		C	E	BUFFERED READ
22	16	1	1	0	0	0	1	1	1		C	7	BUFFERED WRITE
23	17	1	1	0	0	0	1	0	1		C	5	STATUS/COMMAND
24	18	1	1	1	1	1	0	0	0		F	8	ILLEGAL
25	19	1	1	1	1	1	0	0	0		F	8	ILLEGAL
26	1A	1	1	1	1	1	0	0	0		F	8	ILLEGAL
27	1B	0	1	1	1	1	0	0	0		7	8	SELECTED CLEAR
28	1C	1	1	1	1	1	0	0	0		F	8	ILLEGAL
29	1D	1	1	1	1	1	0	0	0		F	8	ILLEGAL
30	1E	1	1	1	1	1	0	0	0		F	8	ILLEGAL
31	1F	1	1	1	0	0	0	1	0		E	2	SEND DATA

LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL 12745A/D STK NO

HP-IB/13037 I/F

BY DATE 4-18-78

APPD SHEET NO 15 OF 68

SUPERSEDES DWG NO A-12745-90004-1

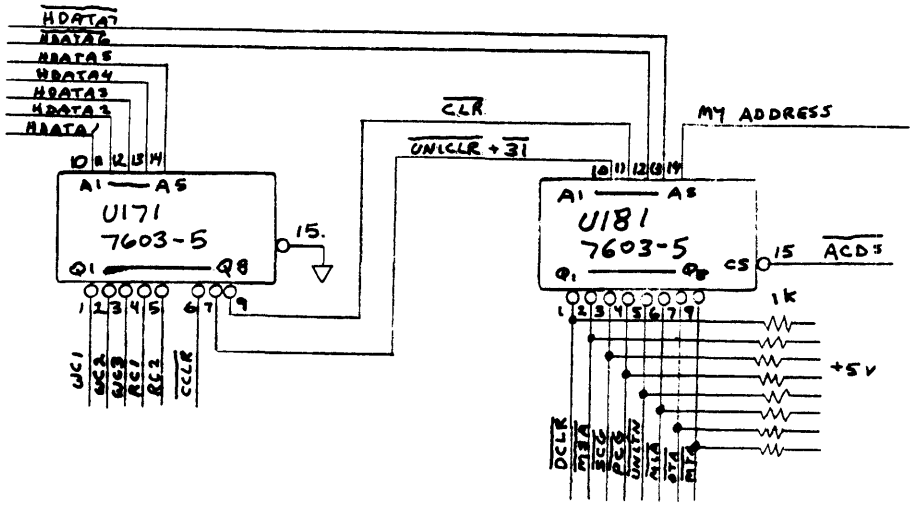


FIGURE 4

The five outputs from U171 not yet described are used as branching information for the state machines. WC1, WC2, WC3 go to the Write State Machine while RC1 and RC2 go to the Read State Machine. Refer to Sections 5 and 6 for their specific effects.

3.5 PRIMARY STATE REGISTER:

Figure 5 shows the primary state register. It is a 4 bit latch whose operation will be described. "MR" input when active will set all outputs to zero. This is caused by:

(a) $\overline{\text{IFC}}$ command line (Section 3.2)

or

(b) PON (Power On) which is generated by the power supply whenever it powers up.

The four data latches are independent S/R type latches when E (Enable) is low. Whichever input was last low (D or S) will cause: 0 for D Low, 1 for S Low. If both are low D overrides and the output is low. When E goes high the inputs are disabled and the outputs remain at

their current state. Inputs $\overline{MTA}$, $\overline{OTA}$, $\overline{MLA}$ and $\overline{UNLTN}$ act on TALK (Q4) and LISTEN (Q3) as described in Section 3.4.

D2 goes active whenever the current command is a TALK (U155 Pin 4) or LISTEN (U155 Pin 5). The output Q2 (MPA) is described in Section 3.6.

D1 goes active when an UNTALK is received. Pin 6 of U184 corresponds to the primary TALK and pin 5 of U184 to receipt of address 31 indicating untalk.

U173 pin 3 is active when a primary command is available ($\overline{PCG}$ and $\overline{ACDS}$ active).

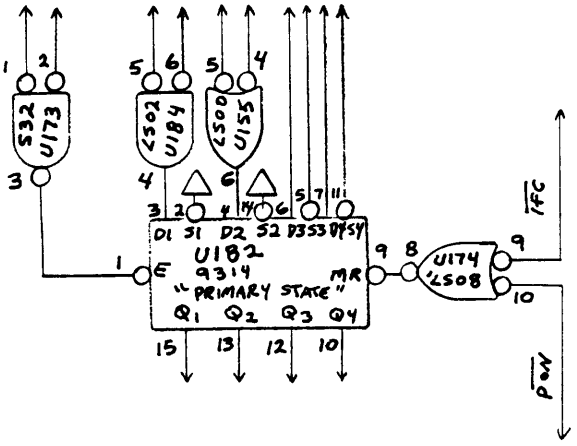


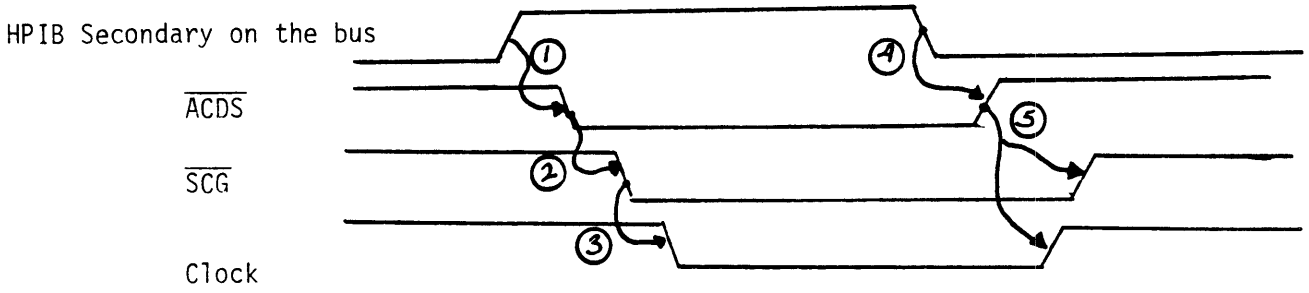
FIGURE 5

3.6 SECONDARY STATE REGISTER:

Figure 6 shows the "secondary state register" and corresponding inputs and outputs. Inputs D2 thru D6 are outputs from the opcode mapping PROM (Section 3.4). They are latched each time a secondary is received. D7 ("MSA") is used when an address match occurs during a secondary command. If following an "UNTALK" this corresponds to an identify request. D8 determines if the last primary command was a "TALK" or

"LISTEN" (MPA = my primary address U173 pin 9) or "UNTALK". A valid secondary can only follow these. If the clock input is activated and D8 is not high, the "second" line does not go high and the secondary state register is in effect invalidated (See Sections 8 and 9).

The clock input acts as shown in Timing Diagram 1.



TIMING DIAGRAM 1

The reset input to the register is activated by "WACK" (Write Acknowledge) and "RACK" (Read Acknowledge). These come from the read and write machines when they are finished with the current secondary command.

WC1, WC2, and WC3, as mentioned, are inputs to the write state machine. However they are qualified by some "random logic" prior to actually getting there. If "Listen" = 0 then WCODE 3, WCODE 2, and WCODE 1 are forced to 0, 0, and 1 respectively. This makes the write machine go down a "nop" path. $\overline{\text{PN DSJ}}$ (Power on DSJ) forces the write codes to 0, 0 and 0. This forces the state machine down the "DSJ Holdoff" path (See Section 8). $\overline{\text{PN DSJ}}$ overrides LISTEN. If PN DSJ = 1 and LISTEN = 1, WCODEm = WCm. RC1 and 2 go directly to the state machine as RCODE 1 and RCODE 2.

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 18 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

U184 pin 10 is the identify input to the state machine (RCODE 4). The identify state occurs if the last secondary matched with the device HPIB address ("MSA") (U184 pin 8) and the board was UNTALKED in the previous primary ("ISS" = identify standby state). "SOURCE" becomes active if (1) the board is "talked" or (2) an "identify" is received (U173 pin 11).

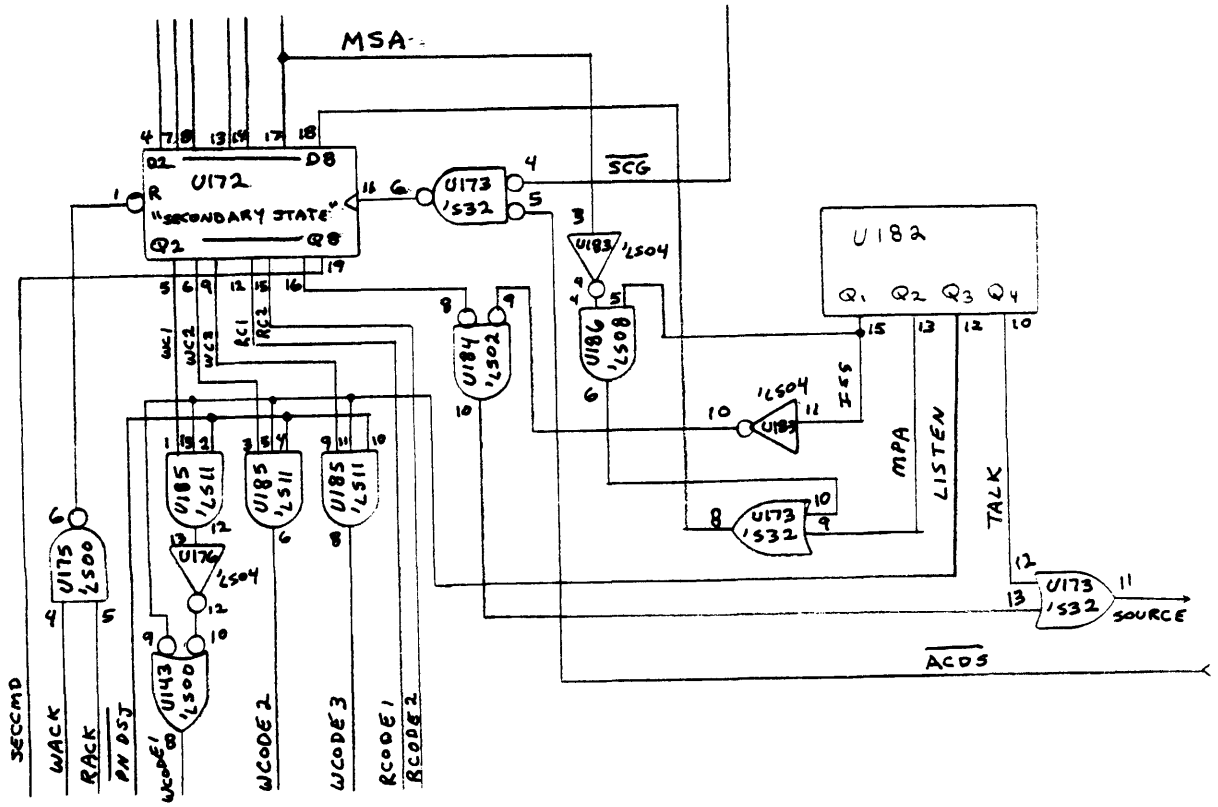


FIGURE 6

3.7 CLEAR LOGIC DECODE:

Figure 7 shows a set of random logic used in decoding two types of clear commands. "CMD CLEAR" is used to reset the Buffer Control

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 19 OF 68
LTR	P.C. NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

logic and clear the Service Flip Flop (Section 7). It is decided initially as "CCLR" (Command Clear, Table 2), U184 pin 3. This occurs upon receipt of a secondary command that:

(1) indicates a 13037 command follows
(2) indicates a status request
(3) indicates a buffered read or write (See Table 2)

In order for "CCLR" to be valid additional conditions must be met:

(a) the board must be in the listen mode (U184 pin 2 checks this)
(b) the "Accept Command Data State" must also occur to indicate a command is actually being processed, U184 pin 11
(c) the previous secondary must already have been processed and hence cleared by $\overline{\text{WACK·RACK}}$. This implies "SECCMD" must be low (U184 pin 12).

When all these conditions are met, "CMD CLEAR" becomes active. $\overline{\text{DEV CLEAR}}$ (U186 pin 11) is a signal that resets the HPIB/CONTROLLER sub-system. The initial decode for this command is "DCLR" (U184 pin 2) (See Section 3.4). However, "DCLR" is qualified by U148 pin 1 in the following manner before becoming $\overline{\text{DEV CLEAR}}$:

(a) the board must be "LISTENED" (U133 pin 3). This is a requirement for selected device clear (Table 2 address 1BH) or
(b) $\overline{\text{UNV CLR}}$ is active (U133 pin 2) which, in conjunction with DCLR, indicates a Universal Clear.

$\overline{\text{DEV CLEAR}}$ can also result from a "power on" (U186 pin 12). RCODE 3 simply corresponds to "TALK" state. $\overline{\text{DCLRO}}$ is the decode of $\overline{\text{DEV CLEAR}}$ that excludes the power on condition.
The four diodes can be found on the board's front. They indicate the states labeled, active when lit.

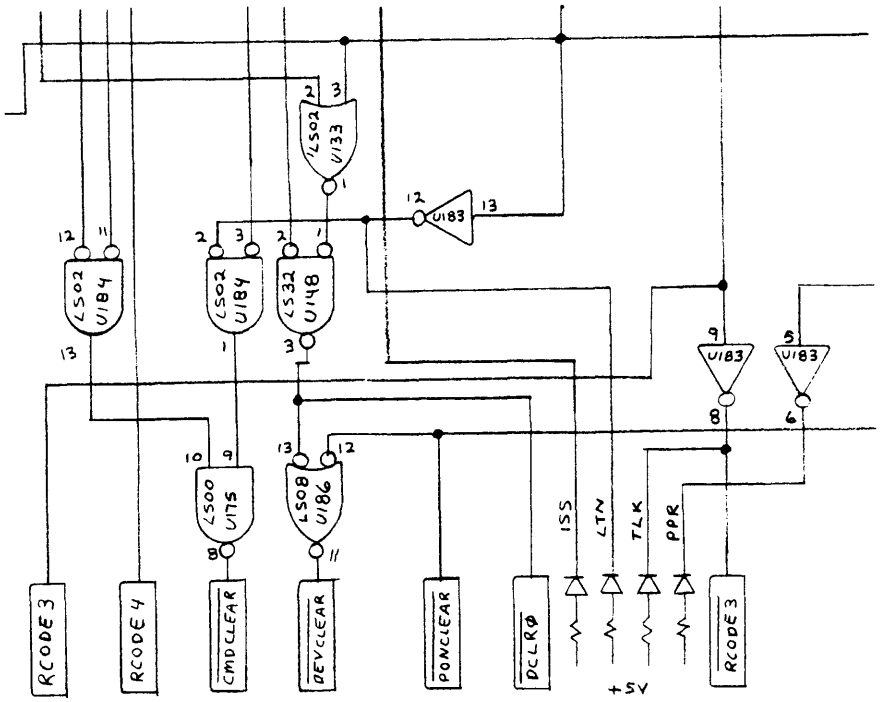
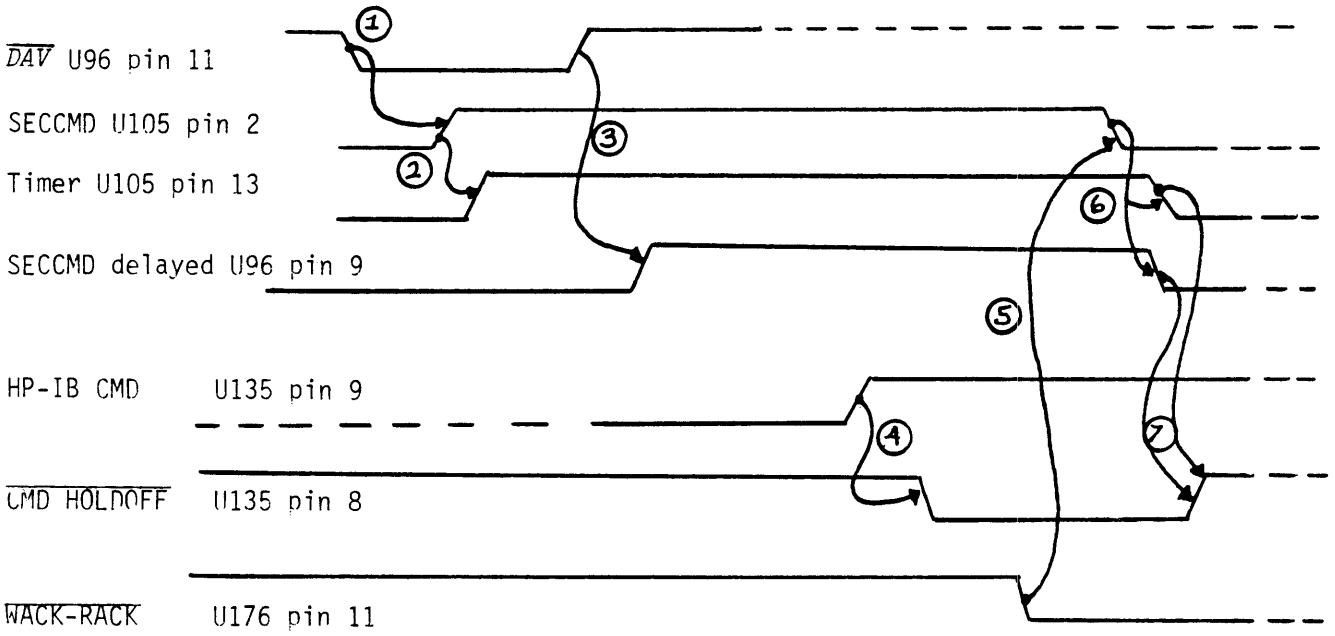


FIGURE 7

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 21 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				



TIMING DIAGRAM 2

A new secondary command is accepted into the secondary state register (Section 3.6), which happens sometimes after DAV is asserted:

(1) after the secondary is accepted SECCMD goes high causing the Timer to fire
(2) when DAV goes away the current secondary command is no longer available. This causes SECCMD delayed to be active
(3) The holdoff state is now achieved.

No further commands can be processed until:

(a) the current command has completed execution (SECCMD delayed goes low from WACK·RACK) or
(b) the timer times out

Without the holdoff circuit, the host CPU could issue a new secondary command while the state machines are in the middle of a branching sequence. The new WCODES and RCODES might cause erroneous branching. The timer is there so that in the event the board "hangs up" it can

3.9 HPIB SOURCE HANDSHAKE:

3.9a Figure 9 shows the set of logic used to implement the HPIB handshake when the 12745A is sending data.

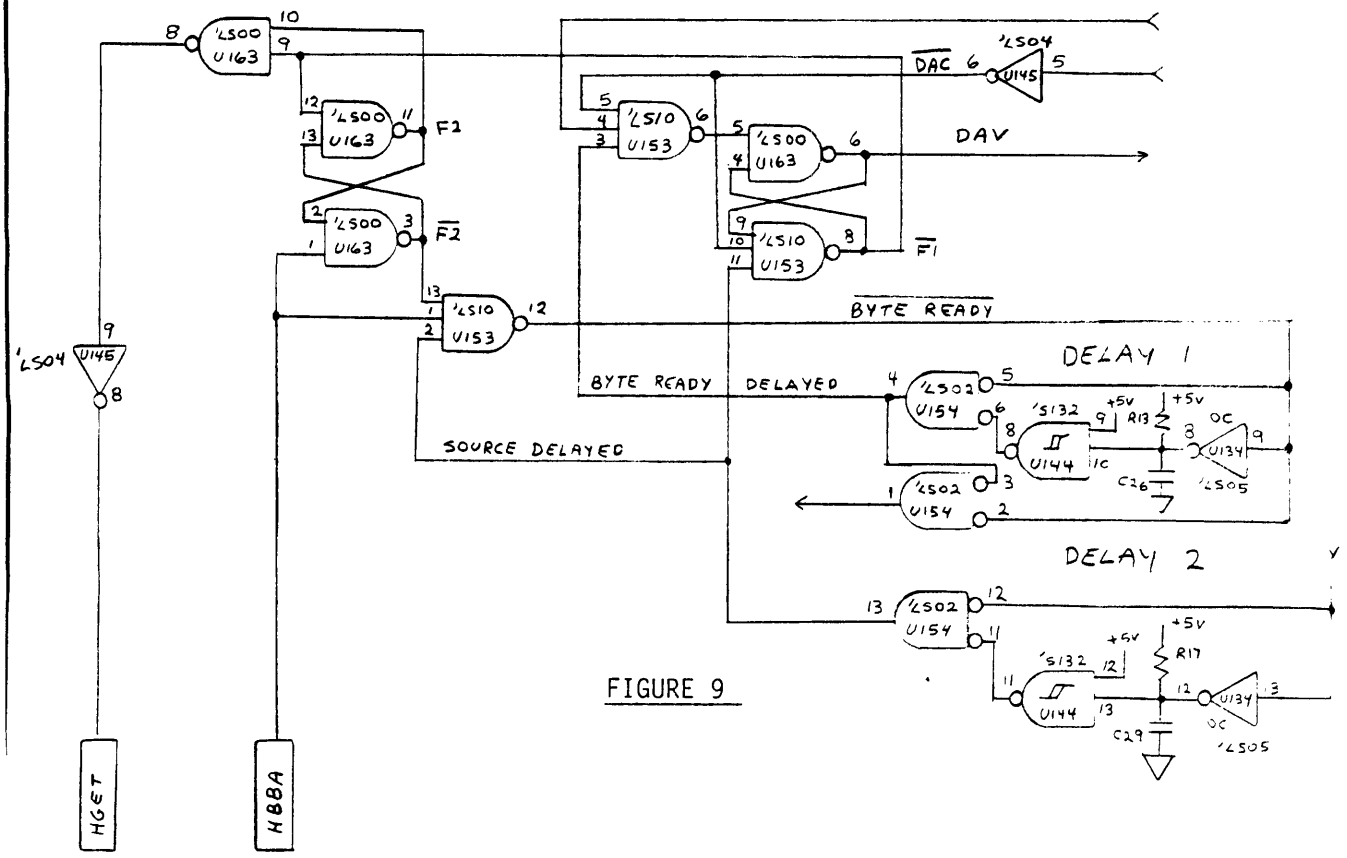
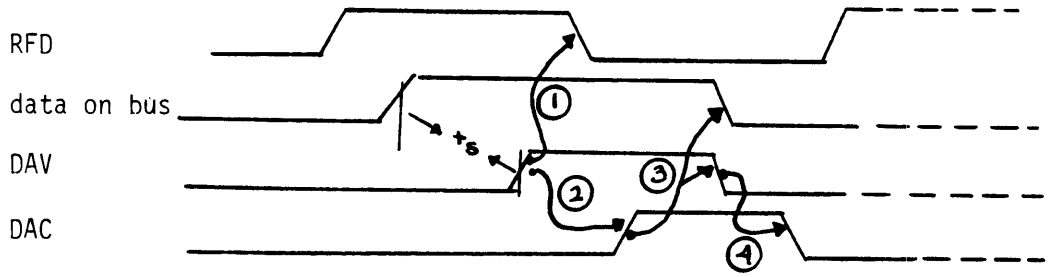


FIGURE 9

				MODEL 12745A /D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 23 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

The basic HPIB handshake is shown in Timing Diagram 3.



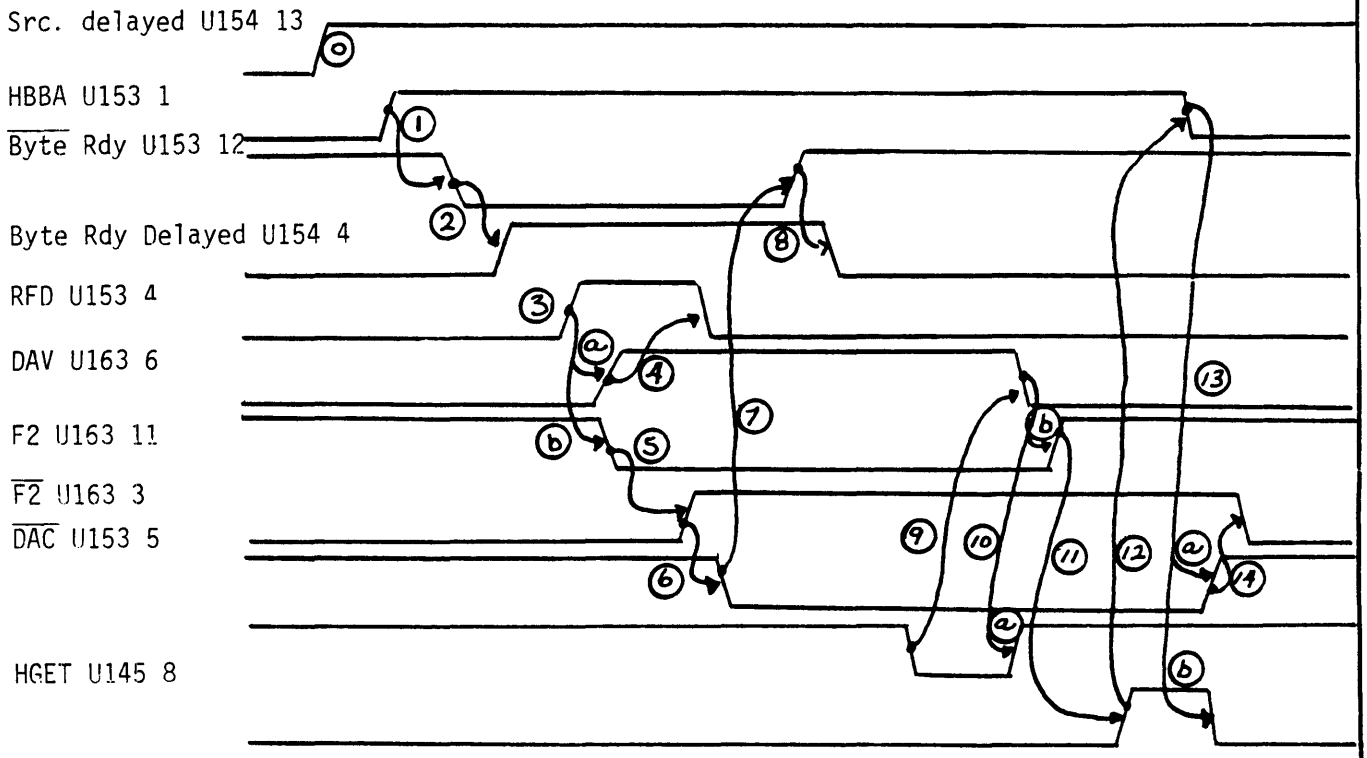
Timing Diagram 3

RFD (Ready for Data) signals that the receiver is ready. Either before or after RFD the sender puts the data on the bus. It is required to settle for 350 ns (ts) at which time DAV (data available) is asserted. When the receiver has processed the data he activates DAC (data accepted) which resets DAV (3). When DAV goes away, it takes DAC with it (4) completing the handshake. When the receiver is ready for the next byte RFD goes high.

3.9b The source handshake proper will be discussed. When the controller of the bus signals the interface to source data, SOURCE HANDSHAKE ENABLE (Section 3.2) goes active (U145 pin 13). When a source on the bus changes from one device to another, the HPIB protocol requires a 300 ns settling time before the new "talker" takes over. Delay 2 provides this requirement. The delay works as follows: initially the input (U134 pin 13 and U154 pin 12) is high. This means that U134 pin 12 is low and the charge is depleted off the capacitor. When the input goes active

(low), U134 goes into its open collector mode. The capacitor is then charged up from current through the resistor. When the capacitor voltage reaches the trigger voltage of U144 (Schmidt trigger input) the output (U144 pin 11) goes low. But the original input (U155 pin 12) was low, thus "source delay" (U154 pin 13) goes active (high).

Timing Diagram 4 shows the remainder of the internal transitions of the handshake.



Timing Diagram 4

HBBA goes high when the interface has valid data to source. Transition (1) is caused directly by the initial conditions of the logic and HBBA going high. Transition (2) is delayed from transition (1) by a network similar to that described above. The delay is to allow the data on the HPIB to set up 350 ns before DAV is asserted.

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 25 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

NOTE: Not all of the delay is accounted for here, some is taken up in buffer controls to be described.

(3) occurs when all listeners are "Ready for Date". This causes DAV to go high (a) and sets the other half of the DAV flip flot $\overline{F2}$ (b). DAV going high will reset the user's RFD signal (See Section 3.9a). $\overline{F1}$ going low sets the other internal flip flop $\overline{F2}$ (5) which in turn sets the other flip flop half $\overline{F2}$ (6). Byte Ready is then reset (7) followed by Byte Ready Delayed (8). Some time later the listeners have taken the data ($\overline{DAC}$). This causes DAV to go inactive (See Section 3.9a) which in turn resets the DAV flip flop (10 (a) and 10 (b)). $\overline{F1}$ going high caused HGET to go high. This ia a signal to either the buffers or the state machine that the HBBA signal has been acknowledged. The buffer control or the state machine will then de-assert HBBA (12), which in turn will deactivate the HGET signal (13 (b)). The secondary internal flip flop is then reset (13 (a) and 14) to bring the handshake logic back to its initial conditions awaiting the next HBBA.

3.10 ACCEPTOR HANDSHAKE LOGIC:

Figure 10 shows the logic used for accepting bytes (either data or commands) over the HPIB. A detailed description of the HPIB handshake is given in Section 3.9a. The acceptor logic is only enabled when the interface is in the LISTEN state (U164 pin 9) or an HPIB command is present (U164 pin 4). If neither is the case, $\overline{\text{ENABLE}}$ will go high causing both NDAC (U143 pin 11) and NRFD (U164 pin 13) to go low. This allows other devices on the bus to complete their data transfers.

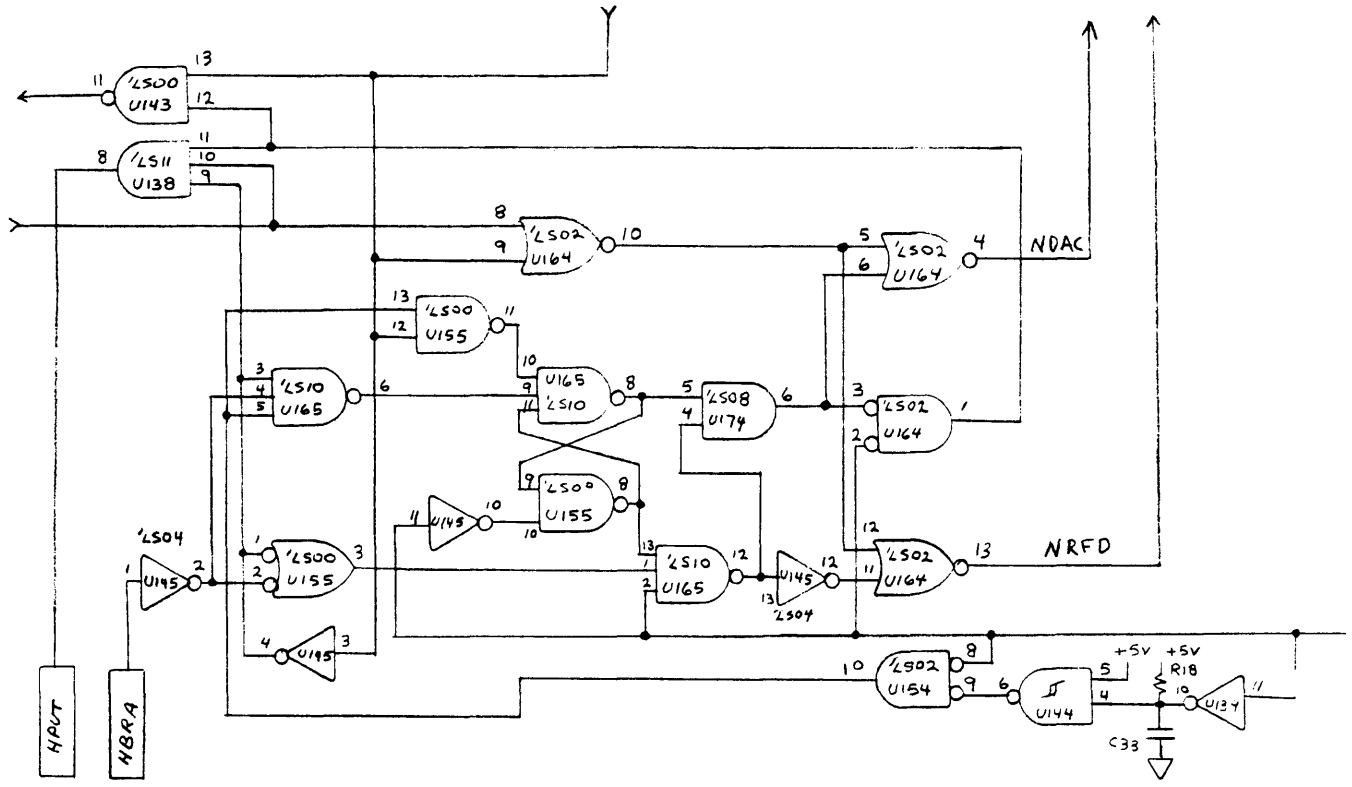
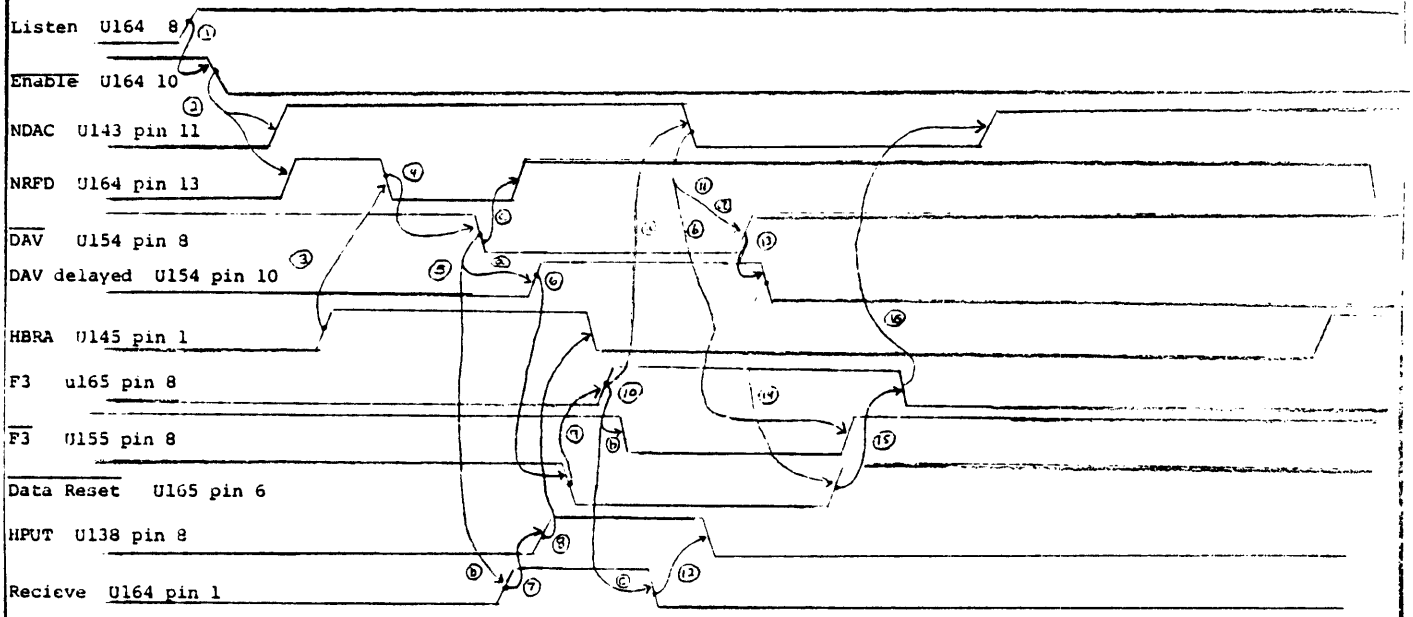


FIGURE 10

LTR	P C NO	APPROVED	DATE	REVISIONS

MODEL 12745A/B	STK NO
HP-IB/13037 I/F	
BY	DATE 4-18-78
APPD	SHEET NO 27 OF 68
SUPERSEDES	DWG NO A-12745-90004-1

HEWLETT-PACKARD CO.



Timing Diagram 5

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO. 28 OF 68
	REVISIONS			SUPERSEDES	DWG. NO. A-12745-90004-1

Timing Diagram 5 shows the important internal transitions of the acceptor logic. The example used is a data transfer, though a similar sequence occurs for commands. (1) is caused by LISTEN going high and enabling the acceptor. This in turn puts NDAC nad NRFD in their initial high state (2). When the buffers have room for more data HBRA does high. This indicates the interface is prepared so NRFD goes low (3). NRFD will eventually cause the sender to assert DAV (4). DAV is put through a 60 ns delay line that guarantees the data set up time and allows the preset on F3 to go high (5a). Transition (5c) resets NRFD, following HPIB protocol. (5b) activates the "Receive" line. This is a signal for both commands and data. If it were a command we were processing "HPIB CMD" would be high causing $\overline{\text{ACDS}}$ (accept command data state) to go low. This would result in a command being processed (See Section 3.4). However, since the example is a data transfer HPIB = Low, which results in HPUT to go active (7). HPUT will send a write pulse to the data buffers. HPUT also resets HBRA (8) to signal the buffer is not ready for the next byte until it has processed this one. Meanwhile, "DAV Delayed" has caused "Data Reset" to go low. This resets the discrete flip flop (F3) to F3 = HIGH (9). F3 going high causes NDAC to go low, signaling that the data has been taken (10a). F3 also causes "Receive" (and hence HPUT) to go low, setting up for the next transfer (10c). In line with HPIB protocol, NDAC will cause DAV to go low (11a) which of course deactivates DAV Delayed also (13). The "Data Reset" line then goes high (14). 11(b) sets one-half of the flip flop to its preset state, while the other half must await "data reset" to go high (14) and (15). The "idle state" is then reached by removing NDAV (16). The acceptor logic then awaits another HBRA and DAV before repeating the entire process.

4 BUFFER MODULE

4.0 Section 4 describes the buffer module of the 12745. Page 2 of

of the schematic which contains the buffer module is described part by part in the sections that follow.

4.1 IN/OUT HANDSHAKE SELECT

Figure 4.1 shows the two IC's that select the direction of the buffer handshake. When the select line is high (U124 pin 1) 1B, 2B, and 3B are selected on U124. Similarly U127 has 2Y1, 2Y2 and 2Y3 active. This allows (a) handshake into the buffers from the controller via RPUT and RBRA (See Section 6) and (b) handshake out of the buffers from the HPIB side via HBBA and HGET (See Section 3). When the select line is low, the direction of the handshake is reversed. The "EOI" tag is also multiplexed from and to the correct side at the handshake.

U127 has tristate outputs. To allow for this and because all signals are active high, pull down resistors R15 are necessary.

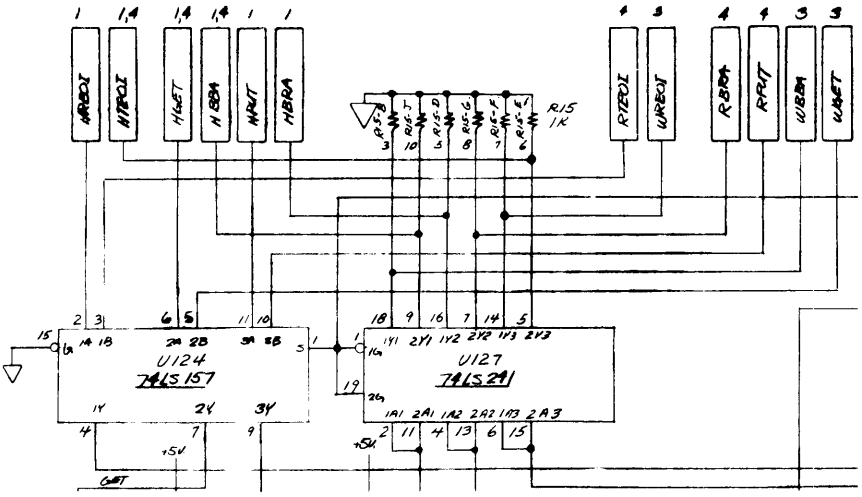


FIGURE 4.1

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 30 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

4.2 BUFFER INPUT CONTROL

Figure 4.2 shows the logic that handshakes data into the buffers. Its major function is to signal when it can accept data (BRA = Buffer Room Available) and generates control lines going to the buffer. A detailed operation sequence is shown in Timing Diagram 4.1.

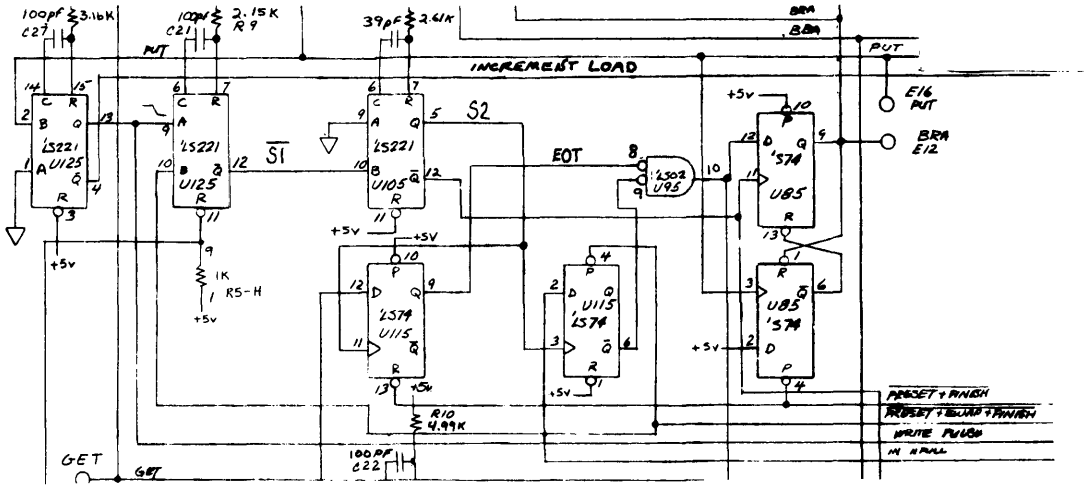
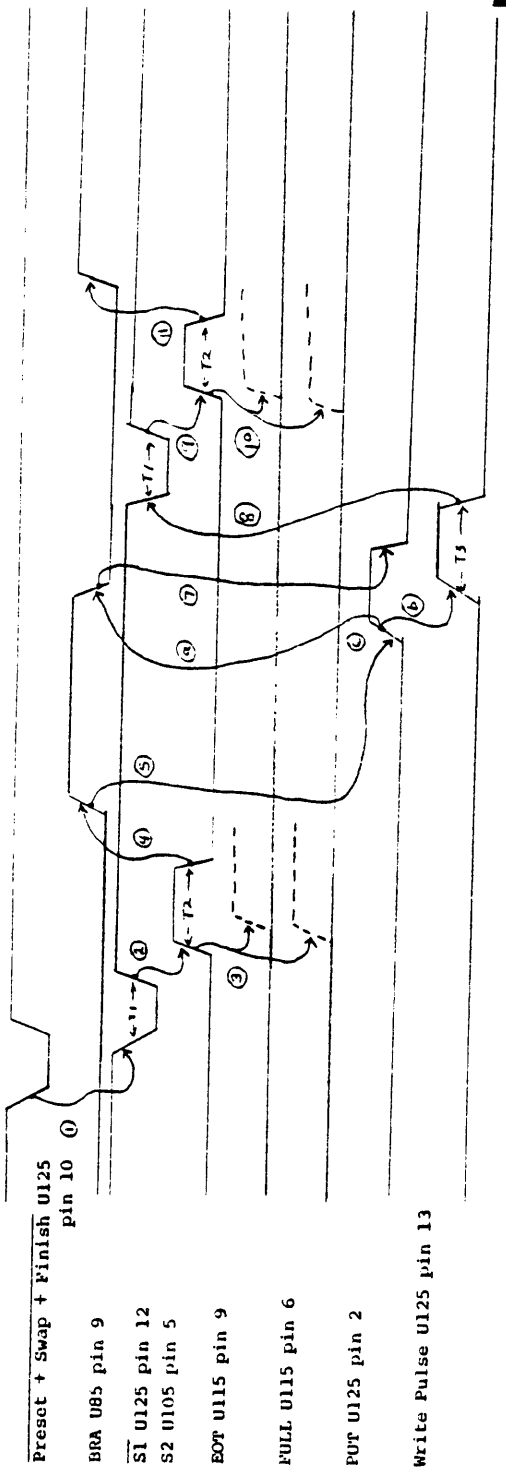


FIGURE 4.2

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 31 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				



Timing Diagram 4.1

				MODEL 12745A/D	STK NO
				HB-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 32 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

Transition (1) initializes the process. This pulse will result from a command being accepted, a power on, or the buffers swapping roles. (1) causes a one shot to fire. The one shot duration is not important at this time. (2) triggers the next one shot. Again the length of this one shot is not important at this stage. (4) completes the initialization by setting BRA high (Buffer Room Available). A data transfer then occurs as follows: When the data source is ready to stuff the buffer and sees BRA high it asserts PUT (5). PUT in turn resets BRA, indicating that the buffers are now no longer ready for another byte (6a). PUT also generates the write pulse that goes to the buffer (6b). The duration of the write pulse (T3) was chosen to satisfy the data settling time in the buffer's rams (180 ns). Transition (7) occurs out of the read module. When BRA goes low, the PUT signal is reset to allow set up of the next PUT sequence. Transition (8) causes the next one shot to fire. Its purpose is to allow the address pointers (Section 4.6) to settle and to allow the EOT and full lines to settle. This takes an additional 190 ns (T1). At the end of T1, the next 1 shot fires (9). Its purpose is two-fold. On the leading edge it samples the inputs to the "full" and "EOT" flip flops (U115). If either the buffer is full or an "EOT" has been received, BRA should not go high again. On the trailing edge of this one shot BRA is set if the above conditions are not satisfied. The logic is then ready to write another byte when the next PUT comes. The duration of T2 was chosen to allow propagation delay through U115 and set up time at U85 pin 12. This is satisfied by T2 = 90 ns.

4.3 BUFFER OUTPUT CONTROL LOGIC

Figure 4.3 shows the control logic used in extracting bytes from the buffer. Timing Diagram 4.2 shows the sequence of transitions that occur in typical operation.

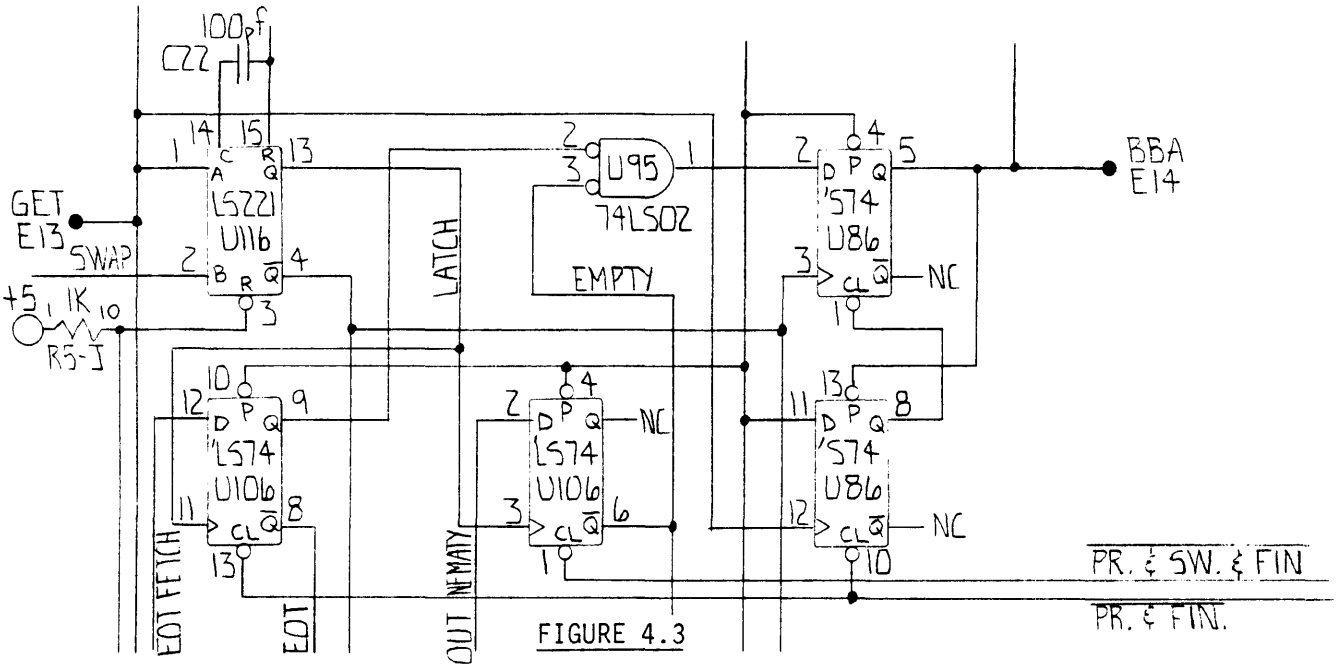
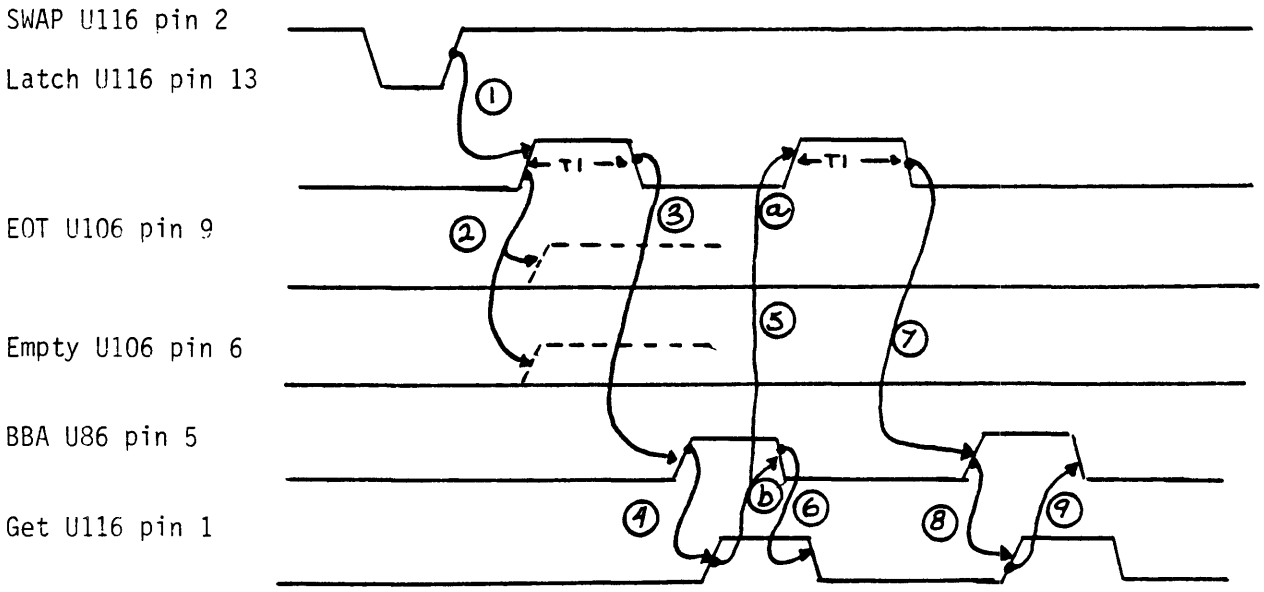


FIGURE 4.3



Timing Diagram 4.2

LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL 12745A/D	STK NO
HP-IB/13037 I/F	
BY	DATE 4-18-78
APPD	SHEET NO 34 OF 68
SUPERSEDES	DWG NO A-12745-90004-1

The process starts by a "SWAP" pulse (1). This is generated when the buffer being written into becomes full and the buffers flip roles. The first valid byte is latched into the buffer output latches (See Section 4.5) on the rising edge of "LATCH". Also on this edge (2), the "end of transfer" (EOT) and "empty" latches are sampled. The handshake out of the buffer will ease, i.e. BBA will not go high if either condition is met. This edge also starts incrementing the address pointer to point to the next byte. The length of the one shot pulse (T1) is such that the address lines are settled and the data is valid out of the buffer before the next "LATCH" pulse comes along. T1 equals approximately 350 ns. The total cycle time from "LATCH" to "LATCH" should be greater than 380 ns. The extra time needed is gotten from propagation delays. The falling edge of "LATCH" sets BBA (3), except in the instances cited above. BBA going high will induce the receiving logic to generate GET (4) which in turn resets BBA. The receipt of GET also starts the next byte fetch (5a). The rising edge of "LATCH" then repeats the process.

4.4 BUFFER RESET AND SWAP

Figure 4.4 shows the logic that is involved in "swapping" the buffers and also in resetting all the buffer logic. $\overline{\text{DEVCLEAR}}$ and $\overline{\text{CMD CLEAR}}$ both control U118 pin 11, the reset line for the buffer logic. $\overline{\text{DEVCLEAR}}$ resets when the rest of the board is reset. $\overline{\text{CMD CLEAR}}$ is used to reset the logic just prior to any data or commands going through. Also causing the reset line (U118 pin 11) to go active is the one shot at the lower left of figure 4.4. Its purpose is to reset the control logic after a data transfer is complete (EOTF=EOT fetched). The "sync" line guarantees that this occurs at the correct time.

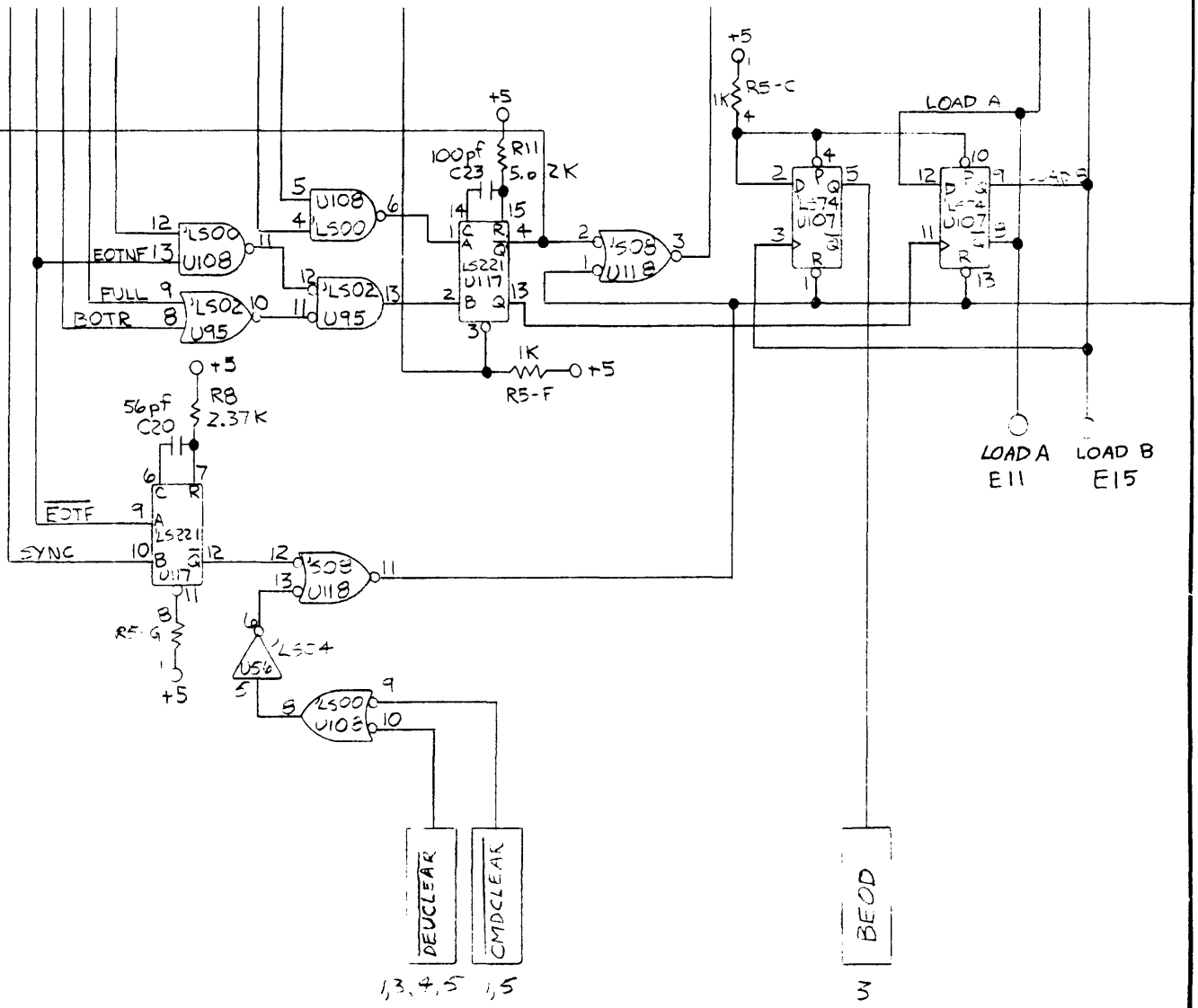


FIGURE 4.4

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 36 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

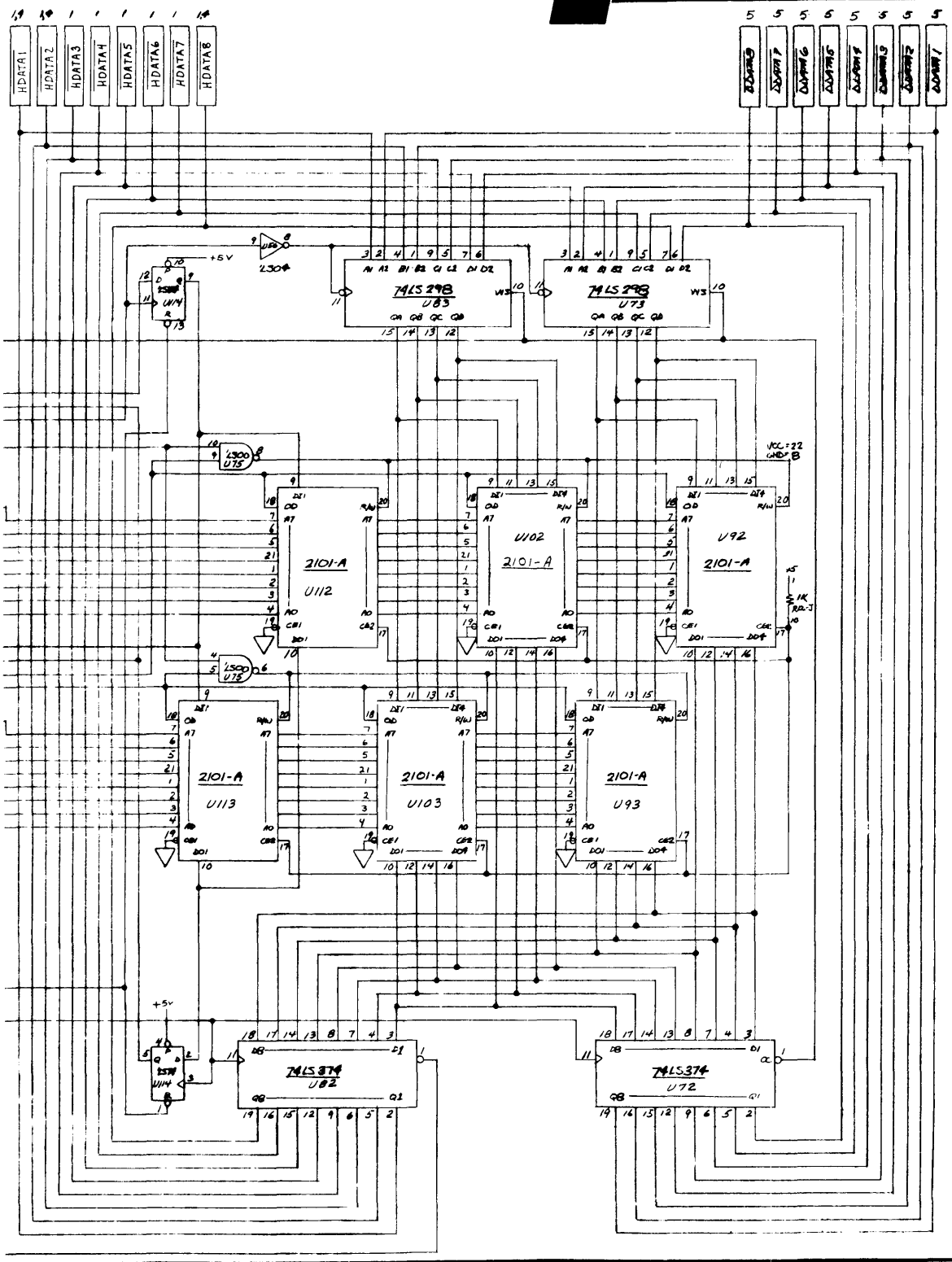
The one shot toward the middle of Figure 4.4 is used to "swap" the buffers. When the buffer that is sourcing data is empty, but has not seen an EOT, it is ready for a new full buffer (U108 pin 11 = Low). When the buffer accepting data is full or has received the last byte, it is ready to have the data read at (U95 pin 10 = Low). When both of the above conditions are met, U95 pin 13 goes high signaling a swap is ready. A sync pulse then comes (U108 pin 6) that activates the "SWAP" one shot. The logic that must be reset by the pulse is connected to U117 pin 4 (those not reset by a clear command) or U118 pin 3 (those reset by the "SWAP" or a clear command). The "SWAP" also clocks the A/B Select latch U107. "LOAD A" high indicates that data is going into buffer A and coming out of buffer B. When "LOAD B" is high, the opposite is true. The "SWAP" pulse causes the role of the buffers to change by causing the "LOAD A/B" line currently high to go low.

BEOD is a control line used to sense when the first swap has occurred.

4.5 BUFFERS

So far there has been considerable discussion about the buffers. Their operation will be explained here. Figure 4.5 shows the memory and associated circuitry that makes up the two full sector buffers. At the top, two multiplexer latches make up the input. "SELECT" determines whether the input shall be from the HPIB Side ("SELECT" = 0) or the controller side ("SELECT" = 1). These two groups of data lines are labeled "HDATA" and "DDATA" respectively. Also included as an input is the D Latch U114. It is used to latch incoming EOT tags. When the input data and EOT bit are ready, "PUT" (See Section 4.2) comes along and latches the information. The latched data is then seen at the input of both the A and B buffers. A short time later a write pulse occurs (See Section 4.2) that secures the data in the latches. The write pulse is however gated with nand gates U75. This allows the pulse only to go to buffer with half the

HEWLETT-PACKARD CO.



				MODEL 12745 A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE
				APPD	SHEET NO 38 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

9320-2789 (FORMERLY 0-700024)

load line high (e.g. Load A = high means the pulse goes to A and not B). The address which is being written to has already stabilized by this time. This process will continue as dictated by the control logic.

As mentioned, while data is being written into the buffer, it can also be read out. The two octal and 1 "D" latches are used for this purpose. The outputs of buffers A and B are connected. However, only one set of outputs is selected at a time.

The "LOAD A/B" lines go to the "OD" (output disable) input of each RAM. The purpose is disable the output lines of the buffer not being read from. When the data is stable, the control logic will latch the data and EOT tag in the latches. The "select" line will then determine whether the data will go to the controller (enabling U72) or the HPIB side (enabling U82).

4.6 BUFFER POINTERS

Figure 4.6 shows the logic used to correctly address the two buffers. U122 and U123 are 2 eight bit counters used for this purpose (they are actually each dual quad counters tied together). As the data is read from or written to the buffers, they are incremented from 0 to 255. The clock input on each (pin 1) comes from U121, a multiplexer. The mux's outputs Y1 and Y2 are selected so that the increment pulse from the write control logic goes to the pointer currently being written into, similarly for the read logic. The multiplexer select line switches with a buffer "SWAP".

The two "D" latches at the top of figure 4.6 detect when the buffers are full. When the counter goes from 255 to 0 the MSB changes high to low. This transition is then detected by the "D" latch and channeled through the multiplexer to the correct set of control logic. There is a "Buffer Full" detector dedicated to each pointer.

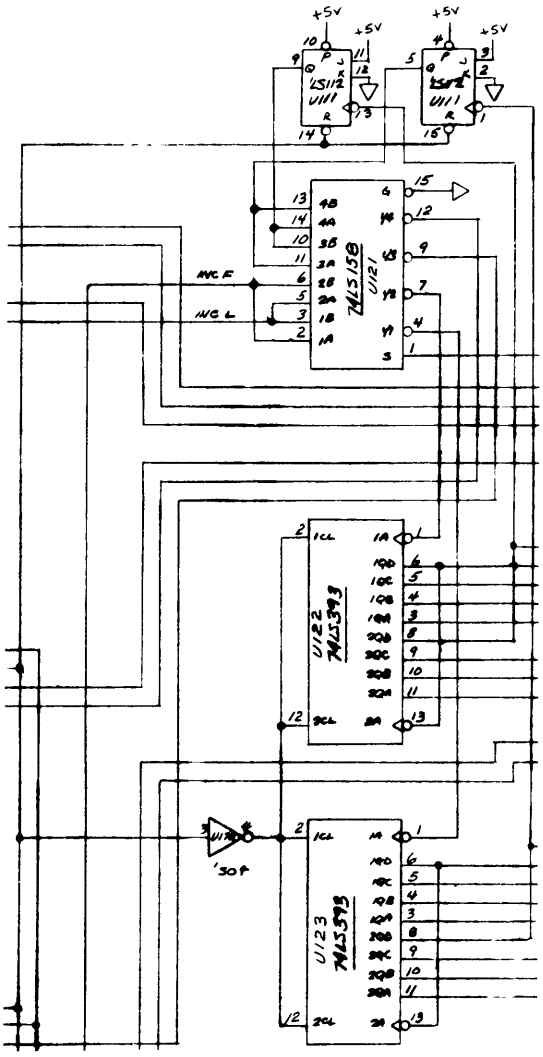


FIGURE 4.6

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 40 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

5.0 WRITE MODULE

5.1 STATE MACHINE

Figure 5.1 shows the write state machine. Because the Read and Write state machines are identical, one description will suffice.

A "state" starts when a new address is latched into the "address" register (U187). This occurs on the clock's rising edge. How that address gets there will be described later.

The new address goes into the mapping PROMS. PROM U168 is the "select prom". It is responsible for selecting input and output control lines. When the input address is stable, U168 has the address of the current output control line at Q3-Q1. It also has the new value of that control at Q4. These go into U167, an eight bit addressable latch. It allows one of its latches (the one addressed) to change at a time. On the low half of the clock cycle, the addressed latch's output reflects the value seen at "D". It is a transparent latch at this point. However, no glitches should occur because "D" is stable. On the clock's next rising edge, the contents are saved. The output lines are used for controlling various module operations to be described in Sections 5 and 6.

Outputs Q5-Q7 of U168 are used to select one of eight input lines at multiplexer U158. The selected input (Y) will be used to determine the next state as described below. To avoid improper operation, the inputs are latched at the beginning of each cycle (U157). Besides going into U168, the current state address goes into prom U178. Its output consists of two four bit address portions used in determining the next address. The ability to determine which of these two four bits to choose is what gives the state machine its "smarts".

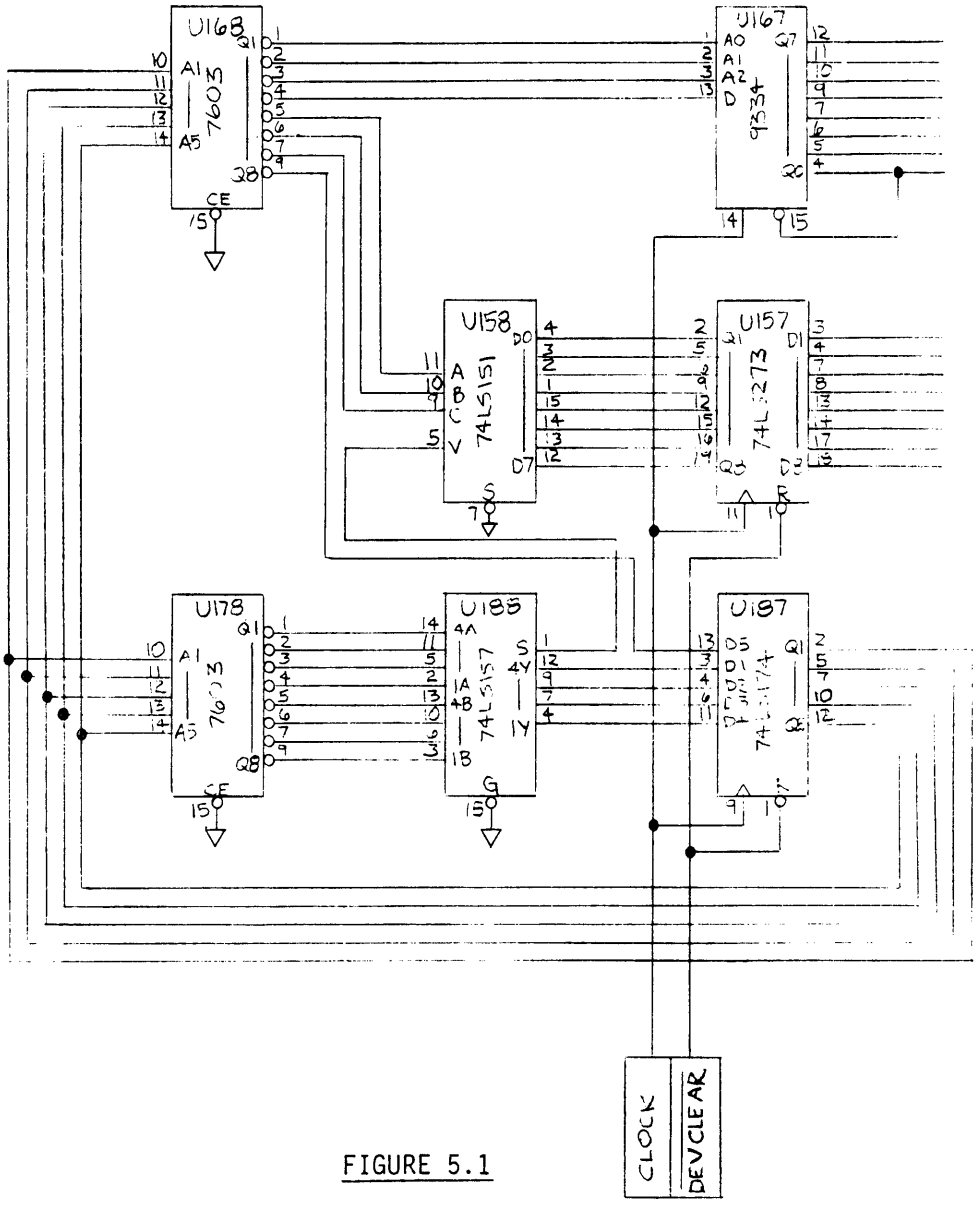


FIGURE 5.1

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 42 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG. NO A-12745-90004-1
	REVISIONS				

This decision is made by using the selected input described above (U158 pin 5). A 0 or 1 will select one or the other four bit sets through the multiplexer (U188). This determines four of the five next address bits. The fifth bit (page bit) comes from mapping Prom U168. When branching, the two next states must have the same page bit! For example, it is not possible to branch to OCH on a 0 input and 1DH on a 1 input. The new five bit address now appears on the address register with the next rising clock edge. The entire process starts again.

$\overline{\text{DEV CLR}}$ resets the address register to 00H and also the input control latch. The output control lines clear by arriving at a state that sets U167 pin 4 low.

5.2 PACKING LOGIC

Figure 5.2 shows the logic that takes bytes from the buffer and packs them into 16 bit words at the controller output latches (See Section 7).

The purpose of the three flip flops in Figure 5.2 is as follows: U146 is used as a byte pointer. It determines whether the most significant byte (MSB) or the least significant byte (LSB) is currently going out. U126 (lower flop) is used to clock the MSB into the output latch (pin 9) and to signal to the buffer control that the byte has been taken (pin 8). The other flip flop half has analogous operation for the LSB.

The remainder of the logic determines when the flip flops should be clocked or reset. Initially a clear pulse is received to U146 pin 15 setting Q = 0. This same clear will

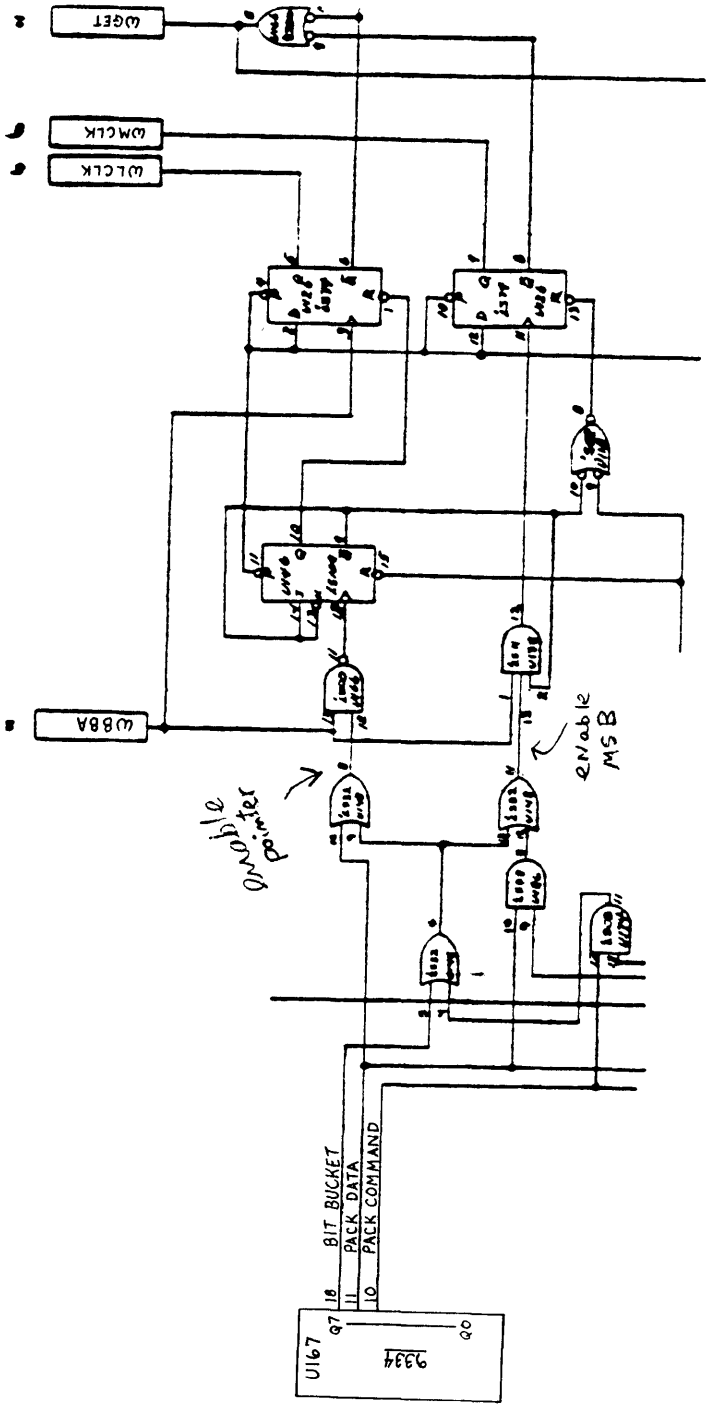
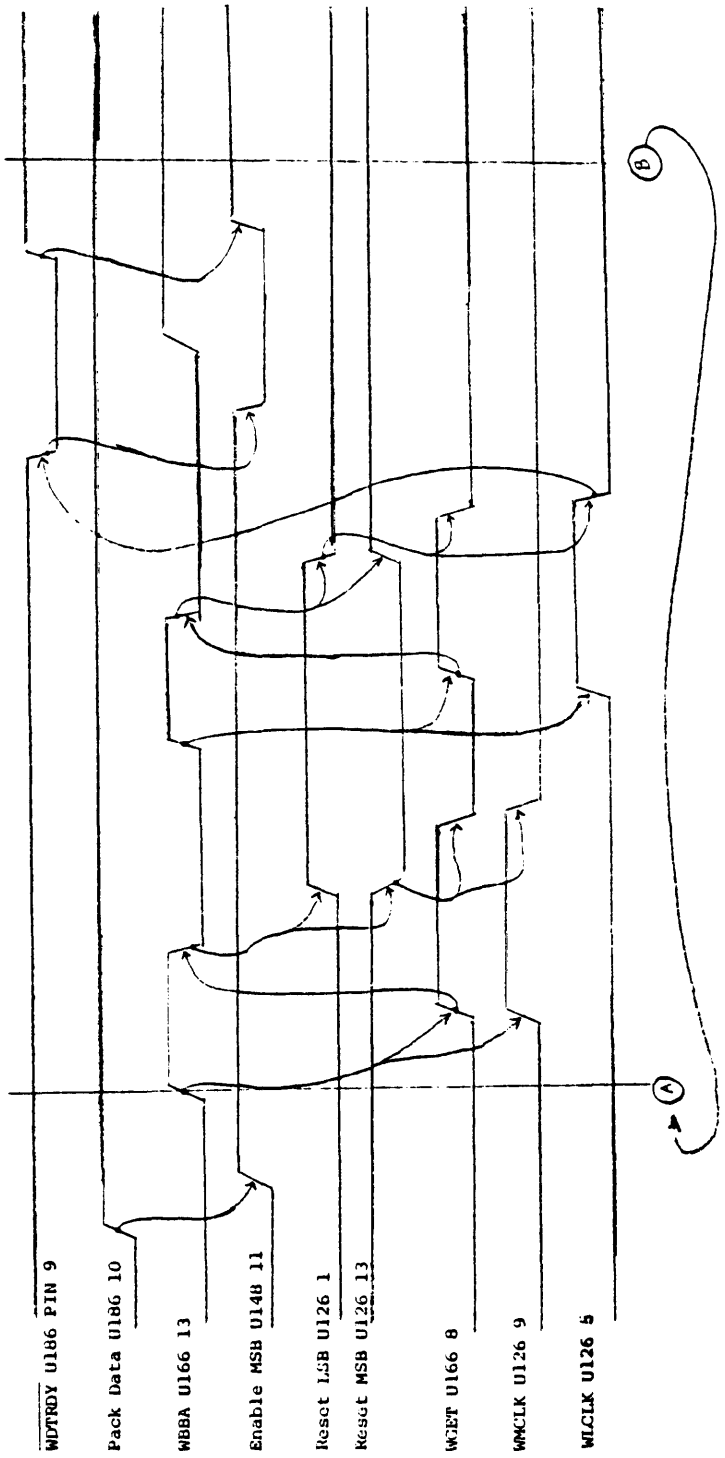


FIGURE 5.2

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 44 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG. NO A-12745-90004-1
	REVISIONS				



Timing Diagram 5.2

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 45 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

cause WLCLK and WMCLK to go low. Following this no data can be taken from the buffers until WBBA goes high (U166 pin 13). This signals that valid information is ready from the buffer. Also the state machine must signal for the write operation to begin. This involves setting "Bit Bucket", "Pack Data", or "Pack Command" high. "Pack Command" is a signal indicating that the first two bytes of a 13037 command are being packed. "Pack Data" indicates that actual data is being packed, or that bytes of a command beyond the first two are being packed. "Bit Bucket" is a line activated when erroneous operation occurs. It allows the buffers to be emptied without sending the data to the disc.

The clock input to the byte pointer (U146 pin 12) will be enabled (U166 pin 12) when any of "Pack Data", "Pack Command", or "Bit Bucket" are active. The "enable MSB" line (U148 pin 11) is activated directly by bit bucket. For it to be activated by "Pack Command" U174 pin 13 must also be high. This line corresponds to a counter. Initially it comes up high, but goes low when the first two command words have been accepted (See Section 5.4). "Pack Data" is qualified by U186 pin 9 (WTDRY). This line is low whenever data is in the output registers and has not been accepted. When the controller accepts the current data work, $\overline{\text{WTDRY}}$ goes high indicating that the output latches are ready for the next word.

Timing Diagram 5.2 shows the actual chain of events.

5.3 WRITE DATA HANDSHAKE

Figure 5.3 shows the circuit used in handshaking the packed work to the controller. Together the two "D" latches of U136 form an edge triggered set-reset flip flop. This SR flop is only

enabled when Pack Data = High (U136 pin 11). Typical operation of the circuit is illustrated in Timing Diagram 5.3. The events start with the set clock going high (1) latching the high "Pack Data" line. This causes WDTRDY to go low (1a), signalling to the controller that valid data is ready. Also the "Reset Bottom" line does high (1b), in effect enabling the clock input to the bottom half. Some time later the clock signal comes from the controller(2). (The derivation of this signal (IFCLK and IFOUT) is explained in Section 7). The effect is to reset the upper half (2) which in turn goes back and resets the lower half (3). It is required by the controller that $\overline{\text{WDTRDY}}$ stay low throughout the duration of IFCCK*IFOUT. This requirement is satisfied by the inverter (U176) during the period (3) to (6). If the controller clock signal is generated prior to $\overline{\text{WDTRDY}}$ being active, an "over run" is detected within the controller.

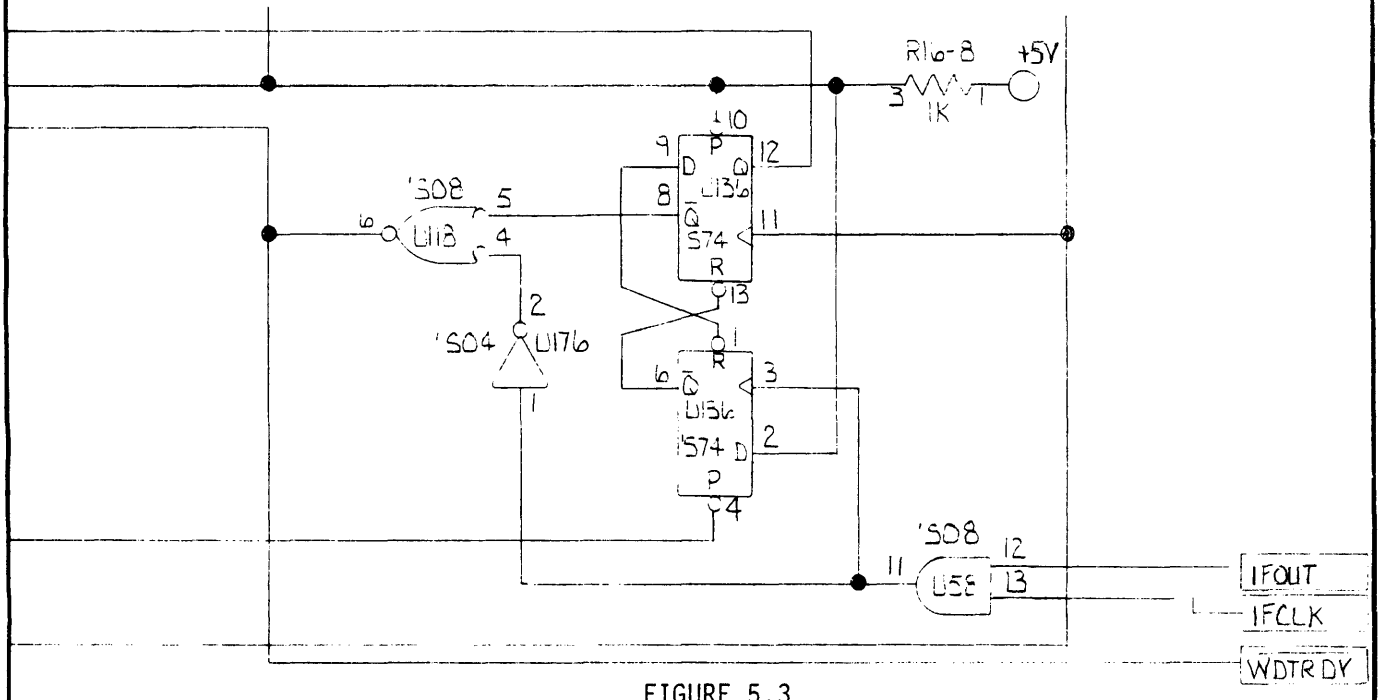
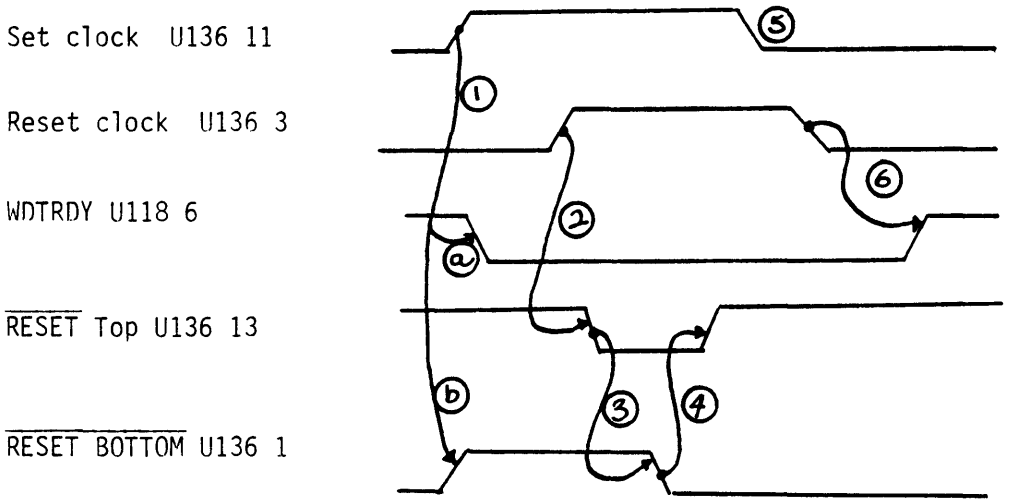


FIGURE 5.3

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 47 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				



Timing Diagram 5.3

5.4 COMMAND PACKING LOGIC

Figure 5.4 shows the set of logic that handles the command packing and handshake of the command to the controller. The right JK flip flop is used as a 1 bit counter during the command packing sequence. First, the Pack Command line goes high (U156 pin 14). Two command bytes are then packed into the 13037 port output latches as described in Section 5.2. At the end of this packing sequence U156 pin 12 goes high, latching the J input. This ends the command packing sequence, since the $\overline{Q}$ output now disables the command portion of the logic described in 5.2. The fact that the packing is complete is signaled through U147 pin 3 (which is low) and then through U147 pin 8, the FINISH input to the state machine. This will eventually cause the state machine to set Pack Command low

(See Section 8). At this time CMDY and $\overline{\text{IFGTC}}$ are low and high respectively. This causes the discrete flip flop of U166 to set G1 initially high as shown in Timing Diagram 5.4. The state machine then sets CMRDY CONTROL high (transition 0). This causes the gated CMRDY (U174 pin 3) to also go high (transition 1). This is a signal to the controller that a command is on its bus. When the controller has accepted the command it causes $\overline{\text{IFGTC}}$ to go low (transition 2), setting G1 = 0 and $\overline{\text{G1}}$ = 1 (3 and 4a). This causes U174 pin 3 to go low (transition 5), taking away the command signal to the controller. U147 pin 11 is also activated at this point, which sets the finish signal to the state machine (transition 4b). When it sees the finish signal, the state machine resets CMRDY control (6) which sets the flip flop to its initial state (7) and (8).

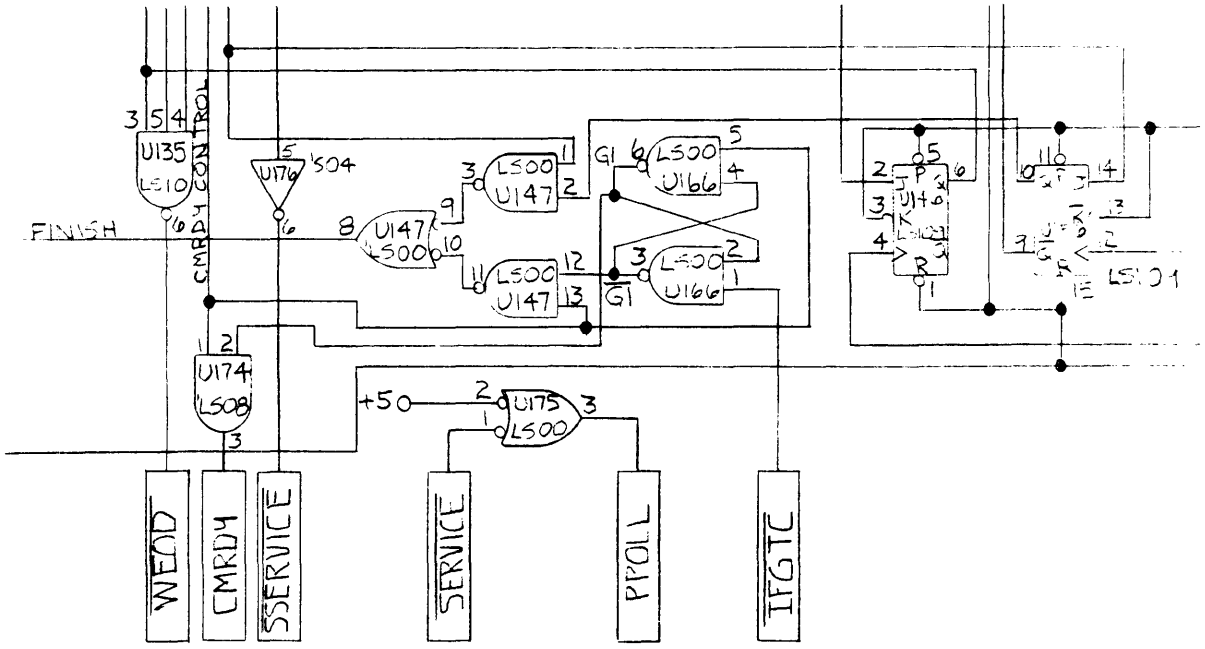
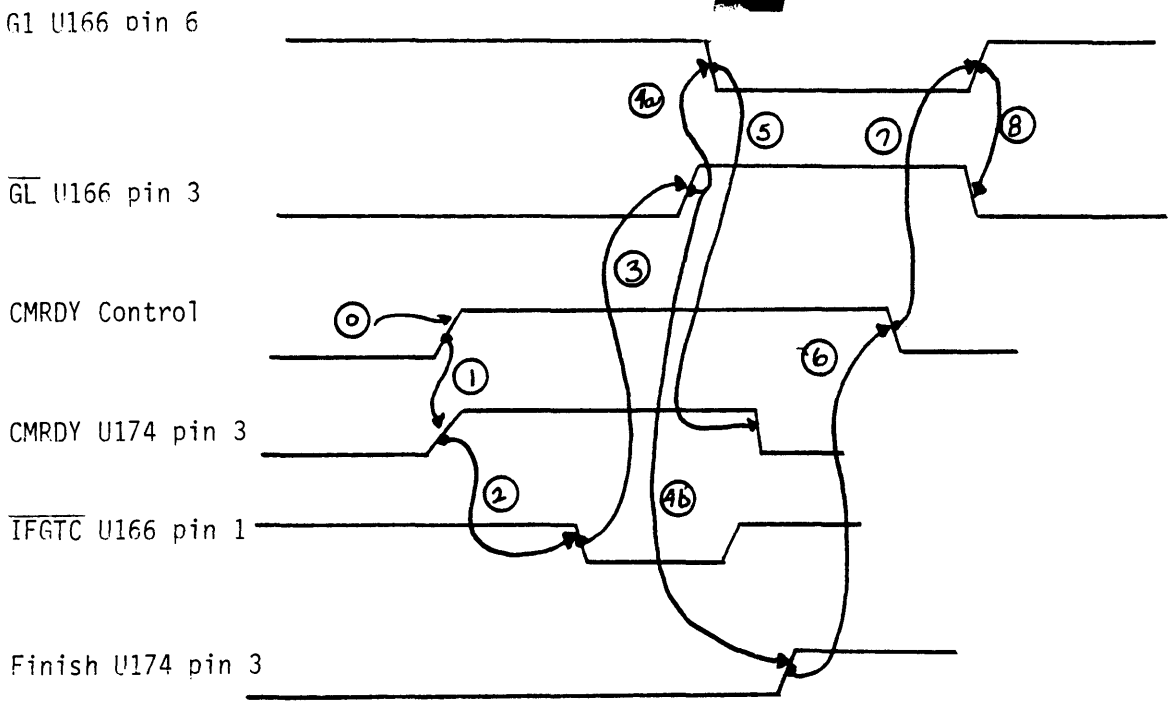


FIGURE 5.4

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 49 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				



Timing Diagram 5.4

6 READ LOGIC

6.0 This section describes the logic on page four of the schematic.

6.1 State Machine

The design of the Read State Machine is identical to that of the Write Machine. Refer to Section 5.1 for a detailed description.

6.2 Unpacking Logic

Figure 6.2 shows the logic used in unpacking the 16 bit words into bytes that are sent to the buffers. The operation of this logic is similar to that described in Section 5.2, though it will be described here in detail.

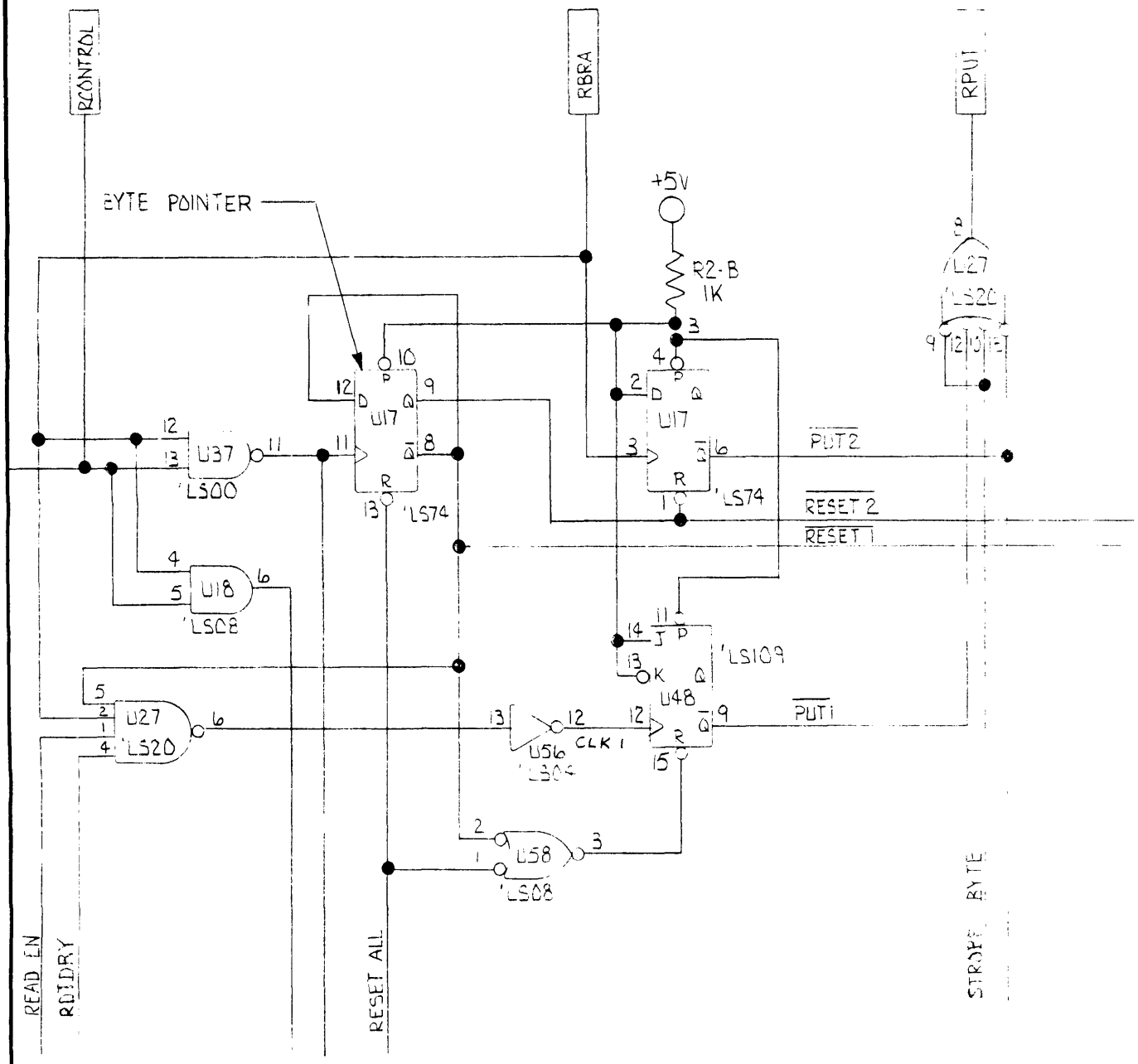
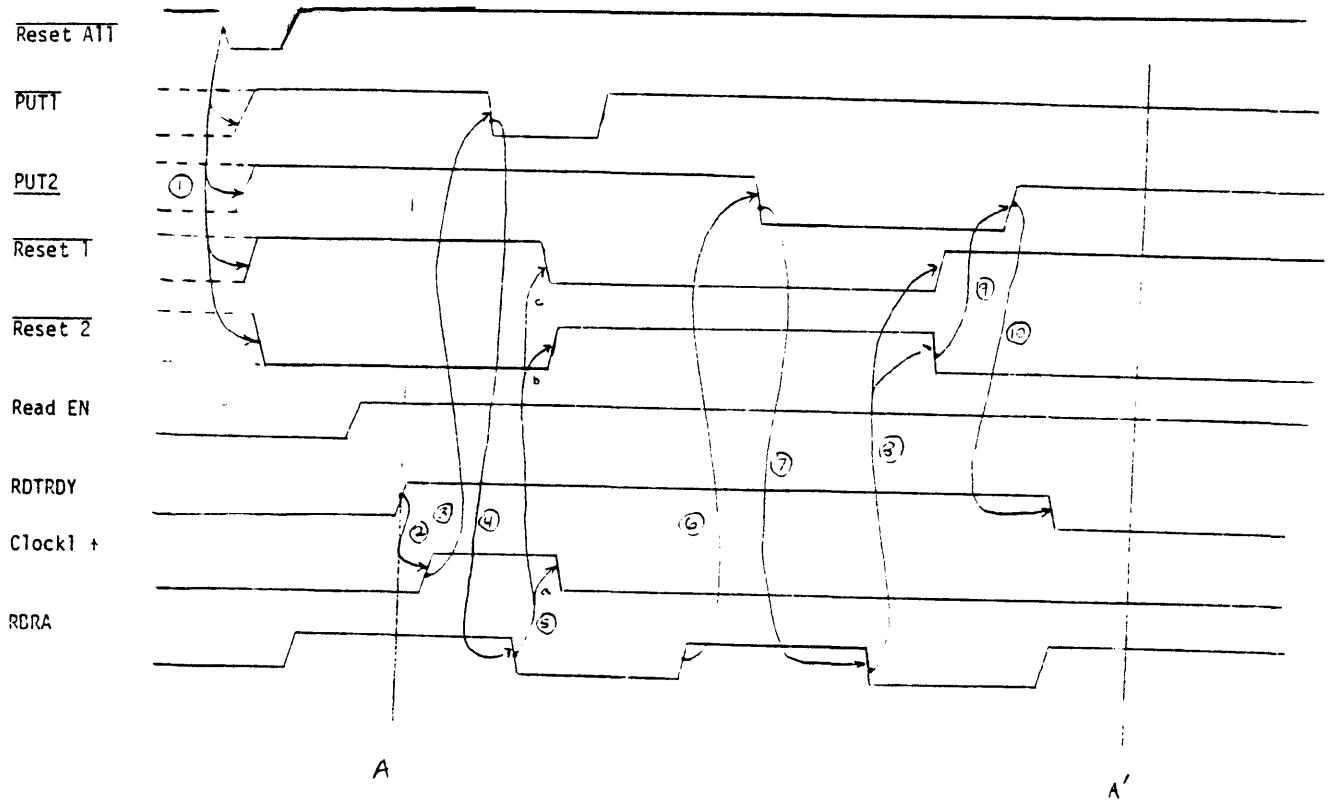


FIGURE 6.2

				MODEL 12745 A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 51 OF 68
	REVISIONS			SUPERSEDES	DWG NO



Timing Diagram 6.2

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 52 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

Timing Diagram 6.2 illustrates a typical sequence of transitions. Transition 1 is the reset pulse to this logic group that is generated by the state machine. Between (1) and (2) RBRA goes high (or was high) and the state machine has set Read EN high. Transition 2 occurs when the controller strobes a word of data into the 13037 PORT, thus setting RDTRDY. When this occurs the logic starts packing the first byte (transition 3). (4) causes RBRA to go low while the address lines into the buffers settle. RBRA will come back high when the address and other data has settled (See Section 4.2). (5) causes the byte pointer to point to byte 2 after its initial point to byte 1. RBRA comes high signaling the second byte can be stuffed into the buffer. This causes the second PUT pulse (6), which in turn resets RBRA (7). RBRA going low causes the byte pointer to point back to byte 1 (8). The $\overline{\text{PUT2}}$ pulse is then taken away (9) which causes the "Read data Ready" (RDTRDY) to go high. The logic state is now the same at A as at A'. The sequence will be started again at A when a new word is received from the controller.

6.3 READ LOGIC/CONTROLLER HANDSHAKE:

Figure 6.3 shows the logic used in handshaking the bytes out of the 13037 port receiver latches. Its operation is similar to the logic described in Section 5.3. The sequence of events starts by a clock pulse being received at U18 pin 3. This is inverted and transmitted to the clock input of U28 pin 11, latching the high input. The clock pulse (1FCLK-1F1N) is caused by the 13037 and

happens only when it has valid data ready to be placed in the buffers. This causes RDTRDY to go active and enables the unpacking logic described in the previous section. When the byte pointer described in Section 6.2 is pointing to the first byte, U37 pin 10 is high. U37 pins 9 and 2 were previously set high by the state machine. This causes $\overline{\text{RMOC}}$ (Read MSB Output Control) to go low, gating the first byte onto the DDATA bus described in Section 4.5 and Section 7. The byte pointer of Section 6.2 then points to the second byte and RLOC becomes active gating the second byte onto the bus. When the logic in section 6.2 has finished writing the second byte, a clock pulse will appear at U28 pin 3. This will reset RDTRDY, indicating that the data in the receiver latches is no longer needed. For an understanding of the operation of the dual D latch used here, refer to Section 5.3 which describes an identical circuit.

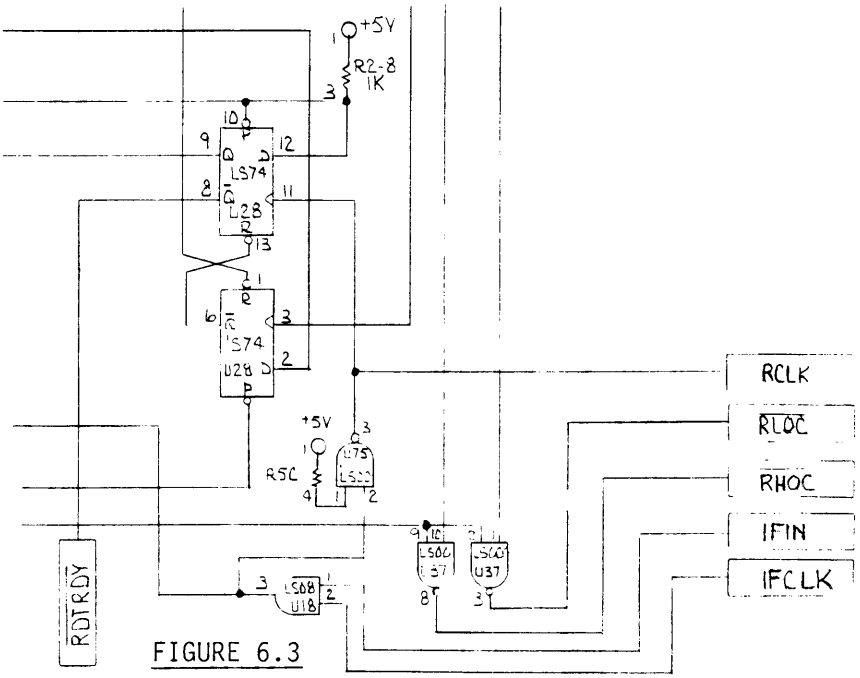


FIGURE 6.3

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 54 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

6.4 OVER-RUN DETECTOR

Figure 6.4 shows the logic used in detecting an overrun. An overrun occurs if the controller writes new data into the 13037 port receiver latches before the old data is taken out, and at some time later the listener requests that byte that has been lost.

The first condition that must occur for an overrun to occur is that RDTRDY (U38 pin 3) is high when a clock signal comes from the controller (U38 pin 1). When this occurs, U38 pin 5, goes high signaling a possible overrun. When the next RBRA signal goes high, signaling the next byte will be taken, U38 pin 13 is clocked and the $\overline{Q}$ output of this latch goes low. This tags the next byte put into the buffer with EOT which, when received, stops any further handshake of controller bytes into the buffer. In the meantime, the listener on the bus continues to accept data from the buffers, causing HGET to pulse (U48, pin 4). When the listener gets to that byte tagged with EOT (the spot where the data was lost), U66 pin 4 goes high (HTEOI). But because it was a read operation, U66 pin 5 was already high, thus U66 pin 6 and U58 pin 9 are high. But when the conditional overrun occurred, U58 pin 10 was high. All these conditions being satisfied means U58 pin 8 is high. Now when the listener accepts this byte where the lost data was, the input to U48 pin 2 will be latched by the resultant HGET. This, in turn, causes the $\overline{Q}$ output (U48 pin 7) to go low, sending a signal to the 13037 port that an overrun has occurred.

The nand gate connected to the reset of this overrun latch allows it to be cleared when a device clear is issued (U53 pin 4) or when a new 13037 command is accepted by the

controller (signalled by $\overline{\text{IFGTC}}$).

The 3 input nand gate (U45) is used to signal the controller to stop sending data (Read end of Data = REOD). The conditions for this signal are that the device controlling the bus UNTALK the 12745 ($\overline{\text{READ CODE 3}}$ = HIGH), that it be in a read sequence (READ EN = HIGH), and that the conditional overrun has occurred (U45 pin 3). In a typical operation the bus supervisor issues a read to the disc, which will keep sending data until it reaches the last track. In the meantime the bus supervisor is counting the data. When it has enough, it stops accepting data and issures the untalk. Back at the disc, the controller has no idea that the transfer has been stopped. The interface keeps accepting the data until the buffer is full and at this time the conditioned overrun occurs, satisfying the condition for $\overline{\text{REOD}}$ described above.

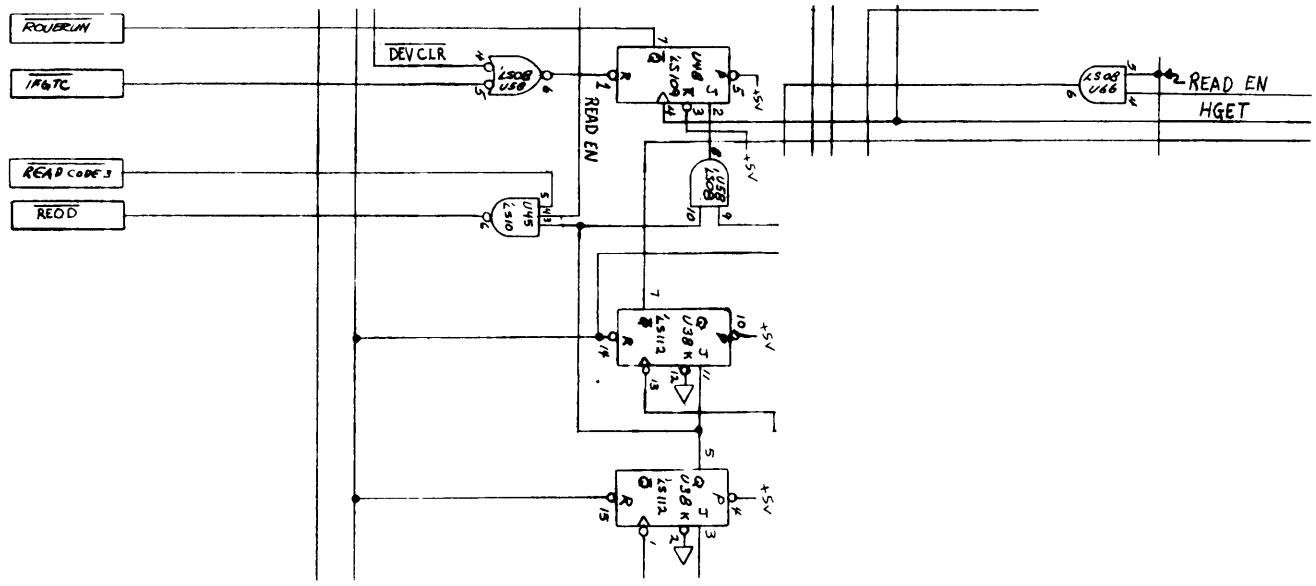


FIGURE 6.4

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 56 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

6.5 OTHER READ LOGIC

Figure 6.5 shows a collection of random logic that performs a number of sourcing functions. The D latch to the left is a power-on detect latch. When a power up occurs, the preset line sets the Q output high. While the latch is in this state, read and write operations will be locked out (See Sections 8 and 9). To clear the latch from this condition either a device clear is issured ($\overline{\text{DCLRO}}$) that pulls on the reset line, or a DSJ request is received which clocks the Q output into the low state.

DSJ is a one bit status. It takes on the values 0, 1, 2 under appropriate circumstances. When the state machine recognizes that it has received a DSJ request, it sets DSJ EN high. When the controller of the bus has set the interface in the TALK state and has relinquished control of the bus, Trans EN goes high. With both TRANS EN and DST EN high, the drivers of the DSJ code are enabled, (U57 pin 6 and U76 pin 6). If the power-on condition occurs, U76 pin 6 pulls the $\overline{\text{HDATA}}$ 2 line low (note U76 is open collector). But the $\overline{\text{HDATA}}$ 1 line will be high in this example because U15 pin 6 is high. The remainder of the HDATA lines have been pulled high (See Section 3.1). Thus the byte is 11111101 which when inverted corresponds to the DSJ power up code 02H. When the power on condition does not occur, $\overline{\text{HDATA}}$ 1 equals DSJ bit meaning the DSJ code can either be 00H or 01H.

The Amigo protocol provides for an "identify" sequence. This allows a particular device to send a unique 2 byte code when an identify sequence is received. In the case of the 12745 /13037 combination that code is 0002H. The

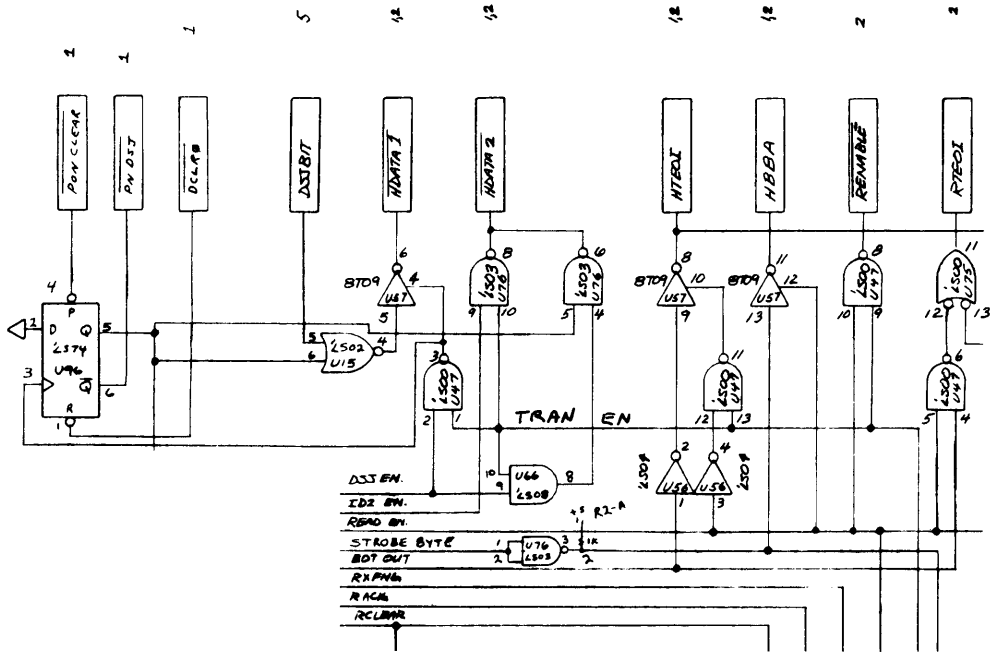


FIGURE 6.5

first byte is sent with all lines on the $\overline{\text{HDATA}}$ bus pulled up (thus = 00H). For the second byte ID2 (identify second byte) is set high. Coupled with TRAN EN going high (signalling that the interface is allowed to talk on the bus). The $\overline{\text{HDATA}}$ 2 line is pulled low by U76 pin 8. This gives 11111101 on the bus (the remaining lines are pulled high) which inverts to 02H.

The group of logic converging on HTEOI is used to send EOT directly to the HPIB when the DSJ and second Identify go out. This can only happen when TRANS EN is high and when a read operation is not being performed (Read EN = LOW). When these two conditions are satisfied, U47 pin 11 enables the tristate inverter U57 pin 8.

STROBE BYTE is a line used in handshaking data to the HPIB directly from the state machine. When STROBE BYTE goes

				MODEL 12745A /D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 58 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

high, HBBA is signalled to the source handshake logic (Section 3.9) by U57 pin 11, providing that Read En is low (U57 pin 12).

RTEOI is the "last byte" tag on sourcing operations going into the buffers. It can either be signalled from the state machine (U75 pin 12) or from the overrun logic (U75 pin 13).

7 13037 PORT

7.0

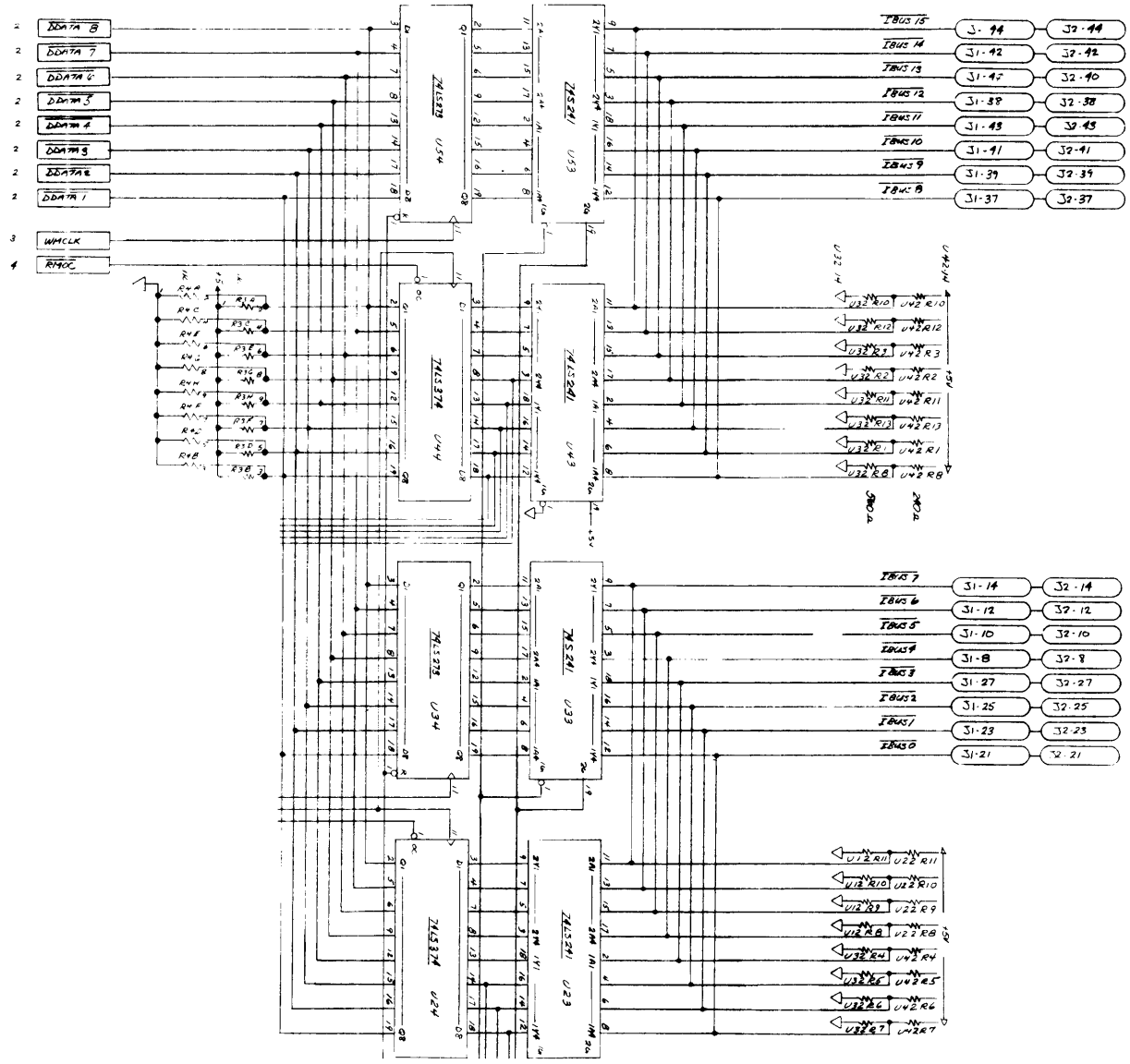
This section describes the logic on the 13037 side of the interface. This corresponds to page 5 of the schematic.

7.1 INPUT/OUTPUT LATCHES

Figure 7.1 shows the input and output latches that separate the interval DDATA 8 bit bus from the external sixteen bit IBUS that goes to the controller. In the output mode, a byte of data is placed on the DDATA bus and latched into U54 with WMCLK (See Section 5.2). The second byte is then placed on the DDATA bus and clocked into U34. The sixteen bit quantity then ripples thru buffers U53 and U33 to the output bus IBUS. The purpose of the drivers is to provide tristate capability going to the controller's data bus. The output drivers are enabled by the controller activating $\overline{\text{ENID}}$ (Enable Interface Drivers) and ENID at pins 1 and 19 of U53 and U33.

The input mode is controlled by the controller causing data to be clocked into U24 and U44. The data is then read from the latches as described in Section 6.3 by enabling the output drivers one at a time. The buffers U43 and U23 are used solely for their Schmitt trigger inputs which provide added noise rejection.

HEWLETT-PACKARD CO.



				MODEL 12745 A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 60 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

9320-2789 (FORMERLY 0-700024)

7.2 INTERFACE CLOCK

Figure 7.2 shows the clock used to cycle the state machines. It is set to operate at 4 MHZ, though could operate anywhere below 6MHZ. The additional random logic associated with the LS324 is used during production testing to control the clock output (the $\overline{\text{stop}}$ input freezes the Q output high allowing CLOCK to toggle as the external $\overline{\text{STEP}}$ toggles).

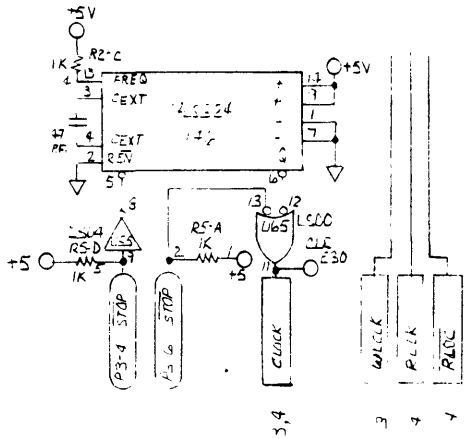


FIGURE 7.2

7.3 CPU NUMBER SELECT

Figure 7.3 shows the IC and thumb switch that determine the "CPU Number". During idle operation, the controller sequentially polls CPU numbers to determine if that CPU has a command for it. It does this by outputting 3 bits on the data bus (the lower 3). If a compare occurs, the Z output of U35 goes high. The interface selects the CPU

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 61 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

number by the setting on S1.

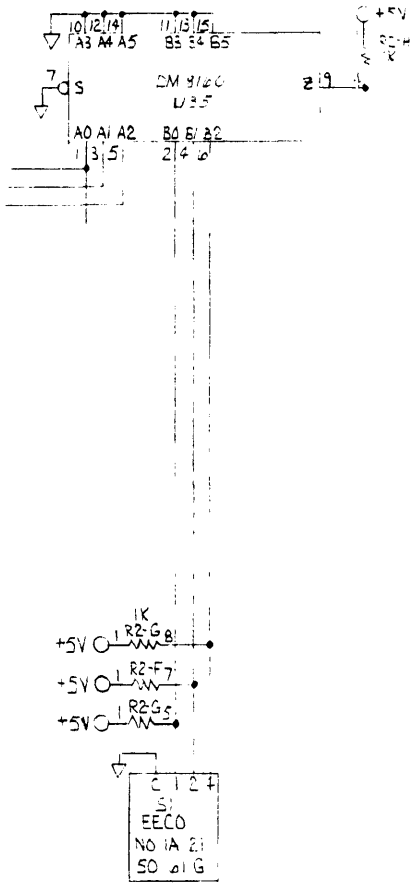


FIGURE 7.3

7.4 MISC CONTROL LOGIC

Figure 7.4 shows a group of random logic that performs a variety of functions. The flip flop U16 has input 12 which is the address compare described in 7.3. After sending out the CPU address, the controller sends a "select" pulse (U16 pin 11). If an address compared occurred (U16 pin 12 = high), the interface is selected. It remains selected until a DISCO (meaning disconnect) pulse comes (U16 pin 13).

HEWLETT-PACKARD CO.

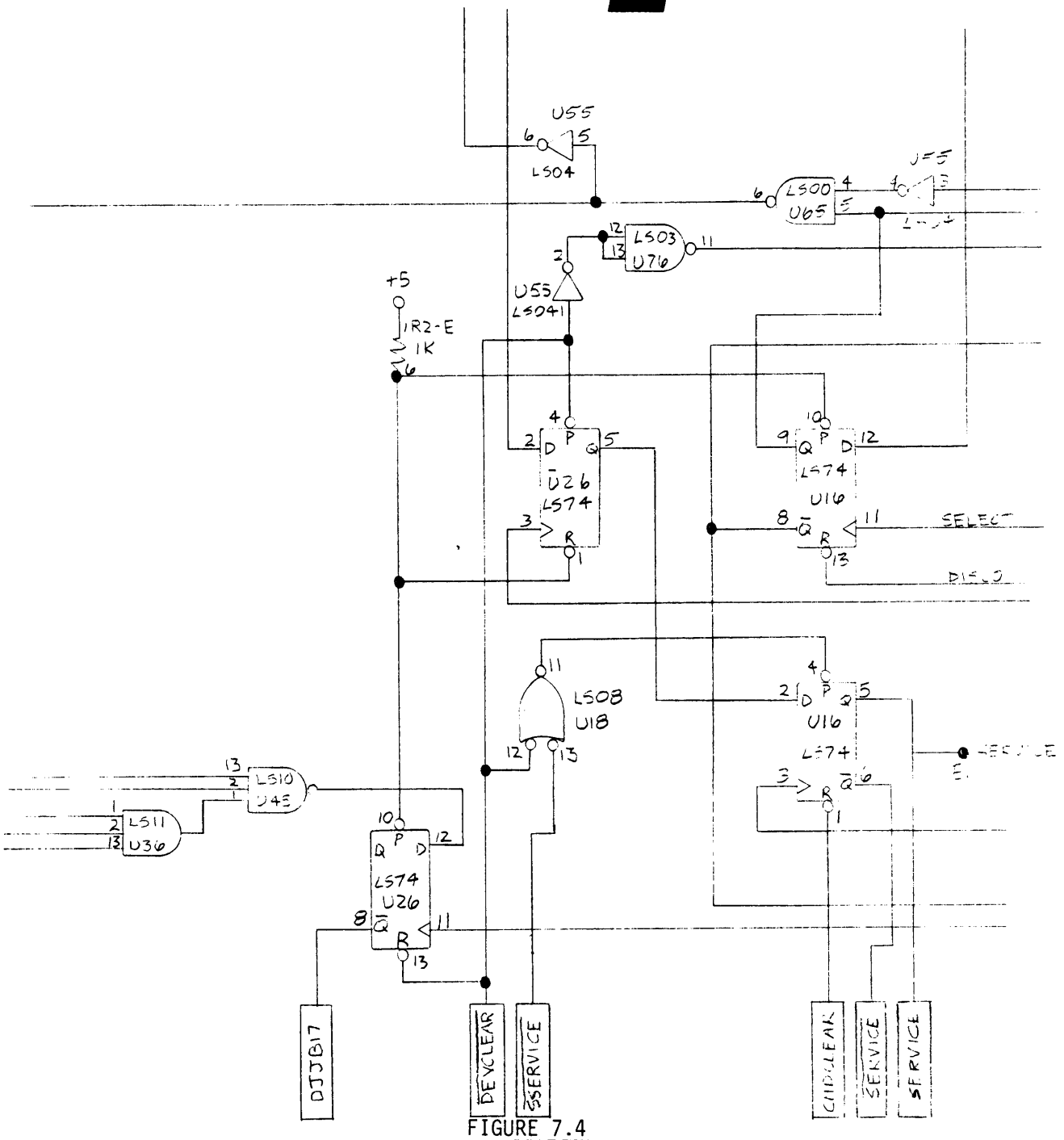


FIGURE 7.4

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 63 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

In Section 7.2 the $\overline{\text{ENID}}$ (enable interface drivers) line was mentioned (U55 pin 3 in Figure 7.4). This is a signal that allows the output drivers to become active. When $\overline{\text{ENID}}$ is active and the interface is selected, the drivers are enabled. (U65 pin 6 and U55 pin 6).

When the disc is performing an operation on the interface and following a selection, it sets $\overline{\text{Busy}}$ low (U26 pin 5). When the operation is complete, the service flip flop is clocked (U16 pin 3), latching the now reset $\overline{\text{Busy}}$ bit.

The DSJ flip flop (U26 pin 8) is used as a one bit status. The data input (U26 pin 12) is a combination of five inputs. These five bits (corresponding to the S1 field) check for S1 = 0 or S1 ≠ 0. If S1 = 0 then the DSJ bit is not set, otherwise it is.

The remaining logic (U18 and U76) is used during a clear to (a) set the service flip flop and (b) clear the 13037.

7.5 FUNCTION BUS

Figure 7.5 shows the logic used in decoding the control lines coming from the 13037. ENIR (enable interface receivers) is not used because the receivers are always enabled. ENID (enable interface drivers) is decided as described in Section 7.4. The four 1F1N lines are decodable control lines that indicate which particular control operation is being performed. The buffer U13 is used for its noise rejecting Schmitt triggered inputs. When the control operation to be done is stable on the 1F1N bus, $\overline{\text{IFVLD}}$ goes active (interface valid). This enables the mapping rom U14, which decodes the four 1F1N lines into eight useable control lines. The six low order outputs are only

enabled when the interface is selected (U25 pin 4). 1FCLK (interface clock) is the pulse used to validate date operations. "IFIN" is active when the interface is receiving data, "IFOUT" when sending.

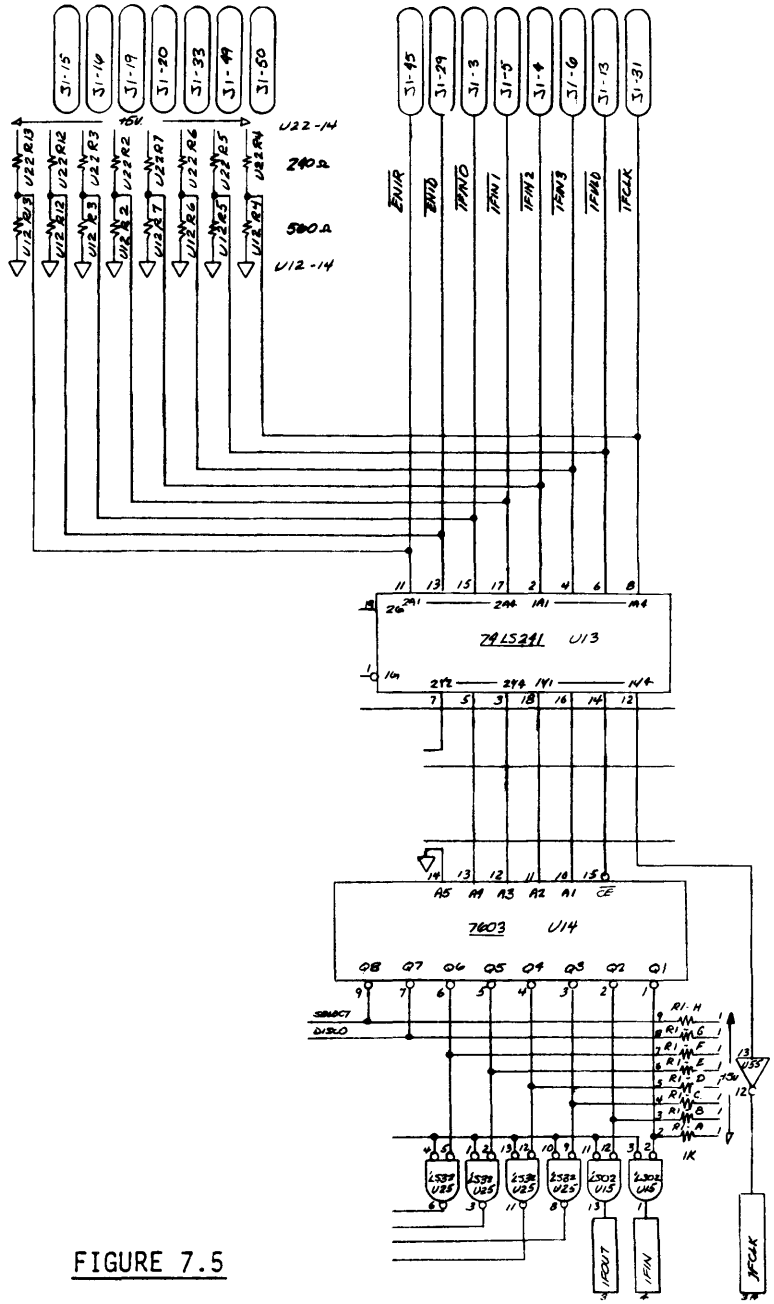


FIGURE 7.5

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 65 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

7.6 INTERFACE SIGNALS

Figure 7.6 shows the control lines going to the 13037B. The buffer U62 is enable only when the controller selects the interface (pins 19 and 1). When this selection occurs the SELECT LED is lit by U62 pin 7.

$\overline{\text{CMRDY}}$ is a signal to the controller that the interface has a command for it. $\overline{\text{DTRDY}}$ is a signal from the write logic that it has data for the controller or a signal that the read logic has not yet accepted data.

$\overline{\text{OVRUN}}$ (overrun) signals that the interface lost a word while doing a disc operation. $\overline{\text{EOD}}$ (end of data) signals to the controller that it should quit the current read or write operation following the current sector. $\overline{\text{XENG}}$ is a signal that is sent to the controller following receipt of an illegal secondary.

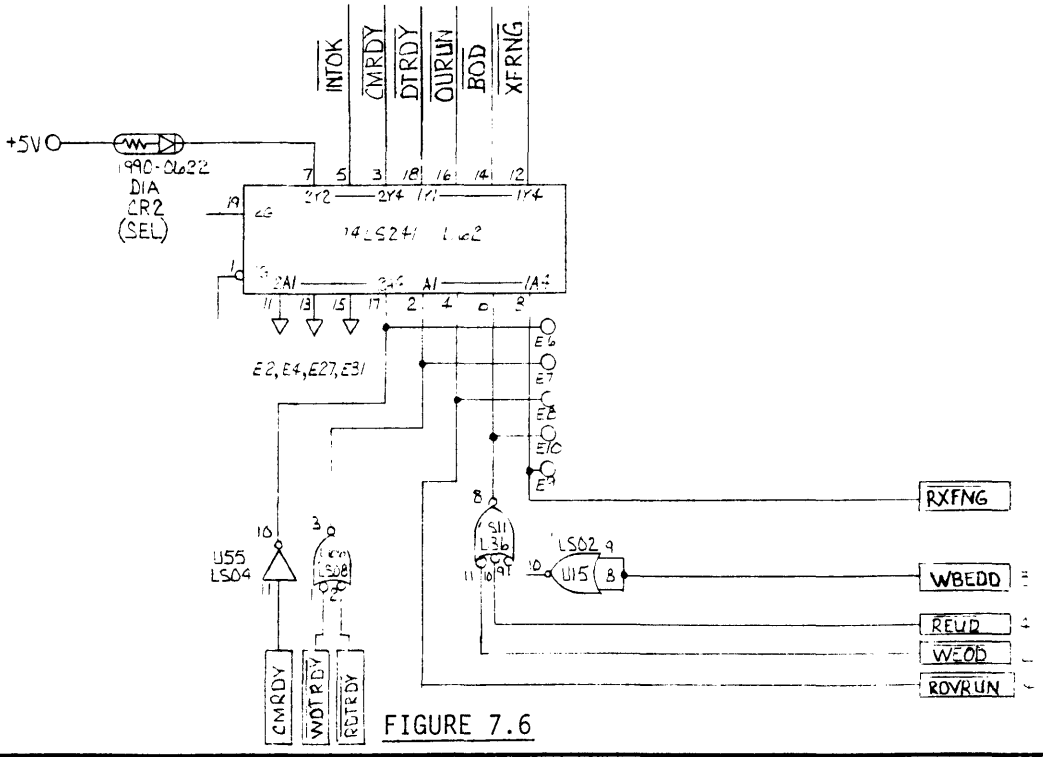


FIGURE 7.6

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 66 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

Figure 7.7 below is used to control the "clear" line going to the 13037. The "DEVCLEAR" pulse only lasts about 100µs, which is too short to go through a low pass filter that the 13037 has on that line for noise immunity. Consequently, the one shot, U116, is added to extend that pulse to about 100µs. The gate U18 disables the parallel poll response to the HPIB to prevent the controller from sending a command while the controller is being cleared. The gate U36 is used to allow only CPU #0 to clear the 13037. This allows for having a "master" CPU to have ultimate control over the 13037.

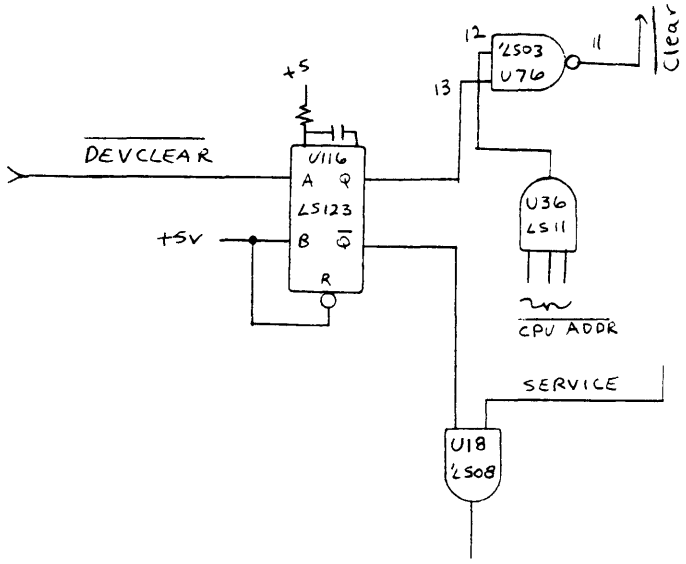


Figure 7.7

				MODEL 12745A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
				APPD	SHEET NO 67 OF 68
LTR	P C NO	APPROVED	DATE	SUPERSEDES	DWG NO A-12745-90004-1
	REVISIONS				

Figure 9B shows a "noise immunity" circuit for the DAV line. Under certain conditions when released, the DAV line will ring on the trailing edge. This can cause a ghost DAV pulse to occur which will lead to improper 12745 operation. The circuit in Figure 9B eliminates that.

It works as follows: before the beginning of a handshake cycle DAV is high. HPIB specs guarantee that this is the case for a minimum of 350 ms. This is sufficient time for the RC network to be charged to +5V (see 3.9b). This means "lock out" = 0. When DAV goes low, this causes U137 pin 4 to go high. U137 pin 5 is already high from "lock out", which means "DAV debounced" goes low. In the mean time, the L505 inverter is discharging the capacitor C19. When this completes, "lock out" will go high. When "Noisey DAV" goes high again, "DAV debounced" follows, but this time "lock out" = 1. This means that U137 pin 5 = 0 which forces "DAV debounced" to stay at 1 even if the "NOISEY DAV" rings. This will remain the case until the delay circuit times out and set "lock out" back to 0.

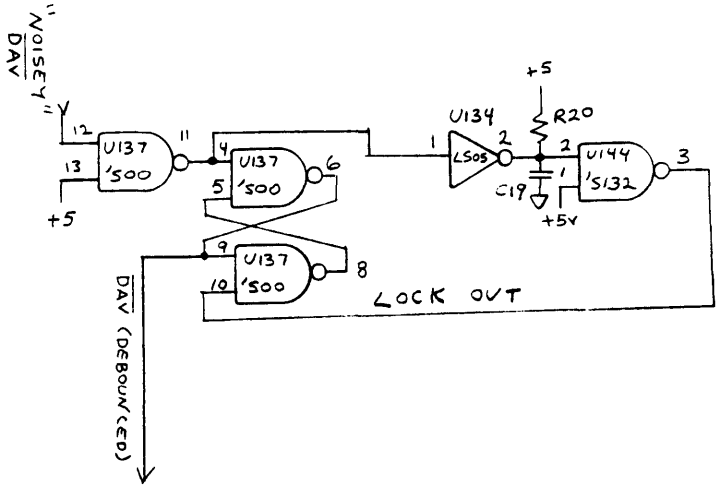


Figure 9B

				MODEL 12745 A/D	STK NO
				HP-IB/13037 I/F	
				BY	DATE 4-18-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 68 OF 68
	REVISIONS			SUPERSEDES	DWG NO A-12745-90004-1

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 12745-60010
12745-68010

DATE CODE : E-2228

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
C1	0160-2055	CAP .01UF-20+80%
C10	0160-2055	CAP .01UF-20+80%
C11	0160-2055	CAP .01UF-20+80%
C12	0160-2055	CAP .01UF-20+80%
C13	0160-2055	CAP .01UF-20+80%
C14	0160-2055	CAP .01UF-20+80%
C15	0160-2055	CAP .01UF-20+80%
C16	0160-2055	CAP .01UF-20+80%
C17	0160-2055	CAP .01UF-20+80%
C18	0140-0190	CAP 39PF 5%
C19	0140-0196	CAP 150PF 5%
C2	0160-2055	CAP .01UF-20+80%
C20	0140-0191	CAP 56PF 5%
C21	0160-0336	CAP 100PF 1%
C22	0160-0336	CAP 100PF 1%
C23	0160-0336	CAP 100PF 1%
C24	0160-2055	CAP .01UF-20+80%
C25	0160-2055	CAP .01UF-20+80%
C26	0160-0336	CAP 100PF 1%
C27	0160-0336	CAP 100PF 1%
C28	0160-2055	CAP .01UF-20+80%
C29	0140-0200	CAP 390PF 5%
C3	0160-2055	CAP .01UF-20+80%
C30	0160-2055	CAP .01UF-20+80%
C31	0160-2055	CAP .01UF-20+80%
C32	0160-2055	CAP .01UF-20+80%
C33	0140-0192	CAP 68PF
C34	0160-2055	CAP .01UF-20+80%
C35	0160-2055	CAP .01UF-20+80%
C36	0160-2055	CAP .01UF-20+80%
C37	0160-2055	CAP .01UF-20+80%
C38	0160-2055	CAP .01UF-20+80%
C39	0160-2055	CAP .01UF-20+80%
C4	0160-2055	CAP .01UF-20+80%
C40	0180-0374	CAP 10UF 10%
C41	0160-2055	CAP .01UF-20+80%
C42	0160-0945	CAP 910PF 5%
C5	0160-2055	CAP .01UF-20+80%
C6	0180-0374	CAP 10UF 10%
C7	0180-0374	CAP 10UF 10%
C8	0160-2055	CAP .01UF-20+80%
C9	0160-2208	CAP 330PF 5%
CR2	1990-0622	LED-VISIBLE
E1	0360-1682	TERM-PIN
E10	0360-1682	TERM-PIN
E11	0360-1682	TERM-PIN
E12	0360-1682	TERM-PIN

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 12745-60010
12745-68010

DATE CODE : E-2228

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
E13	0360-1682	TERM-PIN
E14	0360-1682	TERM-PIN
E15	0360-1682	TERM-PIN
E16	0360-1682	TERM-PIN
E17	0360-1682	TERM-PIN
E18	0360-1682	TERM-PIN
E19	0360-1682	TERM-PIN
E2	0360-1682	TERM-PIN
E20	0360-1682	TERM-PIN
E21	0360-1682	TERM-PIN
E22	0360-1682	TERM-PIN
E23	0360-1682	TERM-PIN
E24	0360-1682	TERM-PIN
E25	0360-1682	TERM-PIN
E26	0360-1682	TERM-PIN
E27	0360-1682	TERM-PIN
E28	0360-1682	TERM-PIN
E29	0360-1682	TERM-PIN
E3	0360-1682	TERM-PIN
E30	0360-1682	TERM-PIN
E31	0360-1682	TERM-PIN
E32	0360-1682	TERM-PIN
E4	0360-1682	TERM-PIN
E5	0360-1682	TERM-PIN
E6	0360-1682	TERM-PIN
E7	0360-1682	TERM-PIN
E8	0360-1682	TERM-PIN
E9	0360-1682	TERM-PIN
MP11	5040-6009	EXTRACTOR PC
MP13	7120-7185	LABEL-INFO
MP14	5020-7318	SPACER
MP9	5040-6058	BRACE-PC BOARD
R1	1810-0275	NTWK RES 9X1K
R10	0698-3279	RES 4.99K 1%.125
R11	0698-3155	RES 4.64K 1%.125
R12	1810-0275	NTWK RES 9X1K
R13	0698-0083	RES 1.96K 1%.125
R14	0757-0279	RES 3.16K 1%.125
R15	1810-0275	NTWK RES 9X1K
R16	1810-0275	NTWK RES 9X1K
R17	0698-3152	RES 3.48K 1%.125
R18	0698-3153	RES 3.83K 1%.125
R19	1810-0275	NTWK RES 9X1K
R2	1810-0275	NTWK RES 9X1K
R20	0698-3449	RES 28.7K 1%.125
R21	0698-3266	RES 237K 1%.125
R3	1810-0275	NTWK RES 9X1K

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 12745-60010
12745-68010

DATE CODE : E-2228

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
R4	1810-0275	NTWK RES 9X1K
R5	1810-0275	NTWK RES 9X1K
R6	0698-0085	RES 2.61K 1%.125
R8	0698-3150	RES 2.37K 1%.125
R9	0698-0084	RES 2.15K 1%.125
S1	3100-3395	SW-THWHL 8 POS
S2	3100-3395	SW-THWHL 8 POS
U102	1818-0343	IC-MEMORY
U103	1818-0343	IC-MEMORY
U105	1820-1437	IC SN74LS221N
U106	1820-1112	IC SN74LS74N
U107	1820-1112	IC SN74LS74N
U108	1820-1197	IC SN74LS00N
U111	1820-1212	IC SN74LS112N
U112	1818-0343	IC-MEMORY
U113	1818-0343	IC-MEMORY
U114	1820-1112	IC SN74LS74N
U115	1820-1112	IC SN74LS74N
U116	1820-1423	IC SN74LS123N
U117	1820-1437	IC SN74LS221N
U118	1820-1367	IC SN74S08N
U12	1810-0335	NETWORK-RES DIP
U121	1820-1428	SN74LS158N
U122	1820-2096	IC SN74LS393N
U123	1820-2096	IC SN74LS393N
U124	1820-1470	IC SN74LS157N
U125	1820-1437	IC SN74LS221N
U126	1820-1112	IC SN74LS74N
U127	1820-1918	IC SN74LS241N
U13	1820-1918	IC SN74LS241N
U132	1820-1199	IC SN74LS04N
U133	1820-1144	IC SN74LS02N
U134	1820-1200	IC SN74LS05
U135	1820-1202	IC SN74LS10N
U136	1820-0693	IC SN74S74N
U137	1820-0681	IC SN74S00N
U138	1820-1203	IC SN74LS11N
U141	1820-1131	IC DM8160N
U142	1820-1360	IC N8T09A
U143	1820-1197	IC SN74LS00N
U144	1820-1307	IC SN74S132N
U145	1820-1199	IC SN74LS04N
U146	1820-1282	IC SN74LS109N
U147	1820-1197	IC SN74LS00N
U148	1820-1208	IC SN74LS32N
U15	1820-1144	IC SN74LS02N
U151	1820-2058	IC MC3448AL

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 12745-60010
12745-68010

DATE CODE : E-2228

REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U152	1820-2058	IC MC3448AL
U153	1820-1202	IC SN74LS10N
U154	1820-1144	IC SN74LS02N
U155	1820-1197	IC SN74LS00N
U156	1820-1282	IC SN74LS109N
U157	1820-1730	IC SN74LS273N
U158	1820-1217	IC SN74LS151N
U16	1820-1112	IC SN74LS74N
U161	1820-2058	IC MC3448AL
U162	1820-2058	IC MC3448AL
U163	1820-1197	IC SN74LS00N
U164	1820-1144	IC SN74LS02N
U165	1820-1202	IC SN74LS10N
U166	1820-1197	IC SN74LS00N
U167	1820-0833	IC 9334PC
U17	1820-1112	IC SN74LS74N
U172	1820-1730	IC SN74LS273N
U173	1820-1449	IC SN74S32N
U174	1820-1201	IC SN74LS08N
U175	1820-1197	IC SN74LS00N
U176	1820-0683	IC SN74S04N
U18	1820-1201	IC SN74LS08N
U182	1820-0626	IC 9314PC
U183	1820-1199	IC SN74LS04N
U184	1820-1144	IC SN74LS02N
U185	1820-1203	IC SN74LS11N
U186	1820-1201	IC SN74LS08N
U187	1820-1076	IC SN74S174N
U188	1820-1470	IC SN74LS157N
U22	1810-0334	NETWORK-RES DIP
U23	1820-1918	IC SN74LS241N
U24	1820-2641	IC SN74LS374N
U25	1820-1208	IC SN74LS32N
U26	1820-1112	IC SN74LS74N
U27	1820-1204	IC SN74LS20N
U28	1820-0693	IC SN74S74N
U32	1810-0335	NETWORK-RES DIP
U33	1820-1624	IC SN74S241N
U34	1820-1730	IC SN74LS273N
U35	1820-1131	IC DM8160N
U36	1820-1203	IC SN74LS11N
U37	1820-1197	IC SN74LS00N
U38	1820-1212	IC SN74LS112N
U42	1810-0334	NETWORK-RES DIP
U43	1820-1918	IC SN74LS241N
U44	1820-2641	IC SN74LS374N
U45	1820-1202	IC SN74LS10N

MATERIAL LIST CONTINUES ON NEXT PAGE . . .

MATERIAL LIST FOR PC-BOARD COMPOSED OF MULTIPLE H-P PART NUMBERS

PART-NUMBER(S): 12745-60010
12745-68010

DATE CODE : E-2228

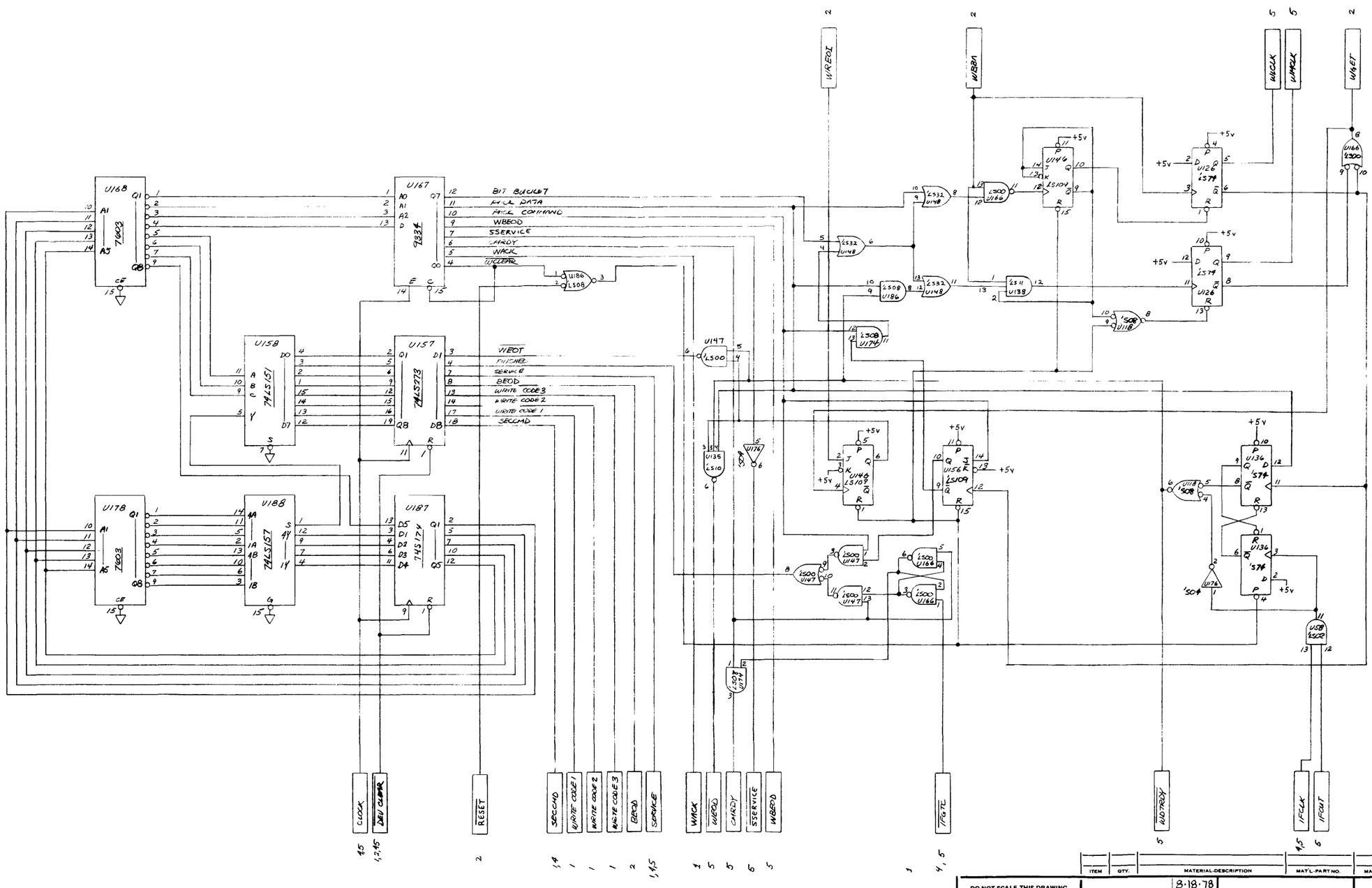
REFERENCE DESIGNATOR	COMPONENT PART	DESCRIPTION
U46	1820-2622	IC SN74LS624
U47	1820-1197	IC SN74LS00N
U48	1820-1282	IC SN74LS109N
U53	1820-1624	IC SN74S241N
U54	1820-1730	IC SN74LS273N
U55	1820-1199	IC SN74LS04N
U56	1820-1199	IC SN74LS04N
U57	1820-1360	IC N8T09A
U58	1820-1201	IC SN74LS08N
U62	1820-1624	IC SN74S241N
U65	1820-1197	IC SN74LS00N
U66	1820-1201	IC SN74LS08N
U67	1820-1730	IC SN74LS273N
U68	1820-1217	IC SN74LS151N
U72	1820-2641	IC SN74LS374N
U73	1820-1444	IC SN74LS298N
U75	1820-1197	IC SN74LS00N
U76	1820-1198	IC SN74LS03N
U77	1820-0833	IC 9334PC
U82	1820-2641	IC SN74LS374N
U83	1820-1444	IC SN74LS298N
U85	1820-0693	IC SN74S74N
U86	1820-0693	IC SN74S74N
U92	1818-0343	IC-MEMORY
U93	1818-0343	IC-MEMORY
U95	1820-1144	IC SN74LS02N
U96	1820-1112	IC SN74LS74N
U97	1820-1076	IC SN74S174N
U98	1820-1470	IC SN74LS157N
XU12	1200-0483	SOCKET 14 DIP LO
XU22	1200-0483	SOCKET 14 DIP LO
XU32	1200-0483	SOCKET 14 DIP LO
XU42	1200-0483	SOCKET 14 DIP LO

END OF MATERIAL LIST.

ENGINEERING RESPONSIBILITY																SEPIA
0	1	2	3	4		6	8	9		11	12	14	15			
16	17		19		21	22	23	25	29	30	32	33	38	43		
45	46	61	63				SCH A	SCH B	SCH C							

D-12745-60010-53

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0875	L.O./ EC	3.18.78
B	CURRENT DATE CODE E-2134 PC48-3558	[illegible]	10-14-81
C	CURRENT DATE CODE E-2228 PC48-3845/A	MAX I -CS	10-6-82



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

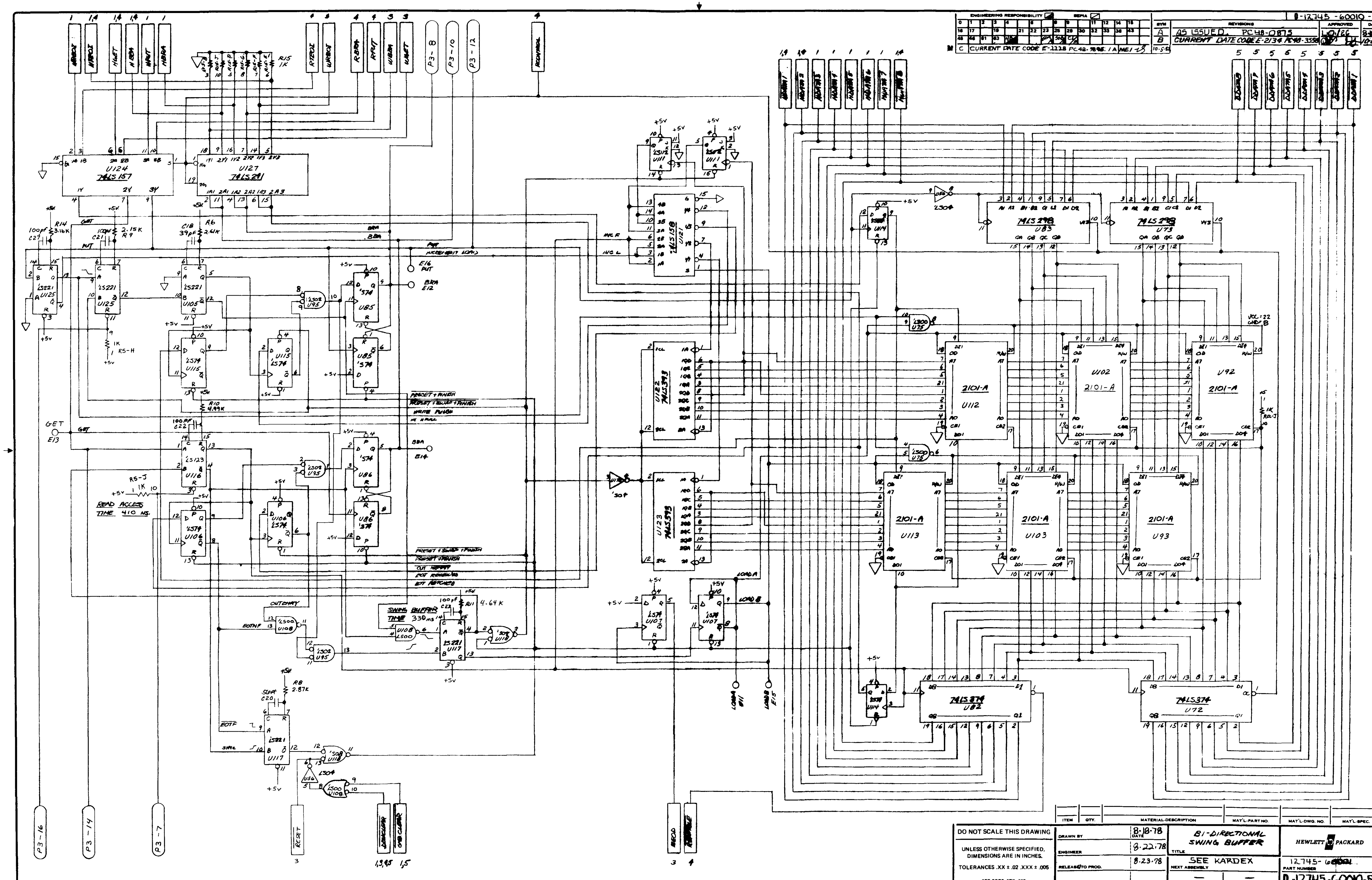
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY	8.18.78 DATE	WRITE LOGIC TITLE
ENGINEER	8.22.78	HEWLETT PACKARD
RELEASE TO PROD.	8.23.78	SEE KARDEX NEXT ASSEMBLY
SUPERSEDES DWG.		FINISH — SCALE —

12745-60010 PART NUMBER

D-12745-60010-53

SHEET 1 OF 1



STOCK NO 9280-0004 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT

ZONE	REVISIONS	APPROVED	DATE
A	AS ISSUED. PC48-0875	LOY/EC	8-12-81
B	C9 WAS 47 PF ; U45 WAS 74LS324 ;		
	ADDED NOTE ; PC 48-2894	LNT/JB	7.2.81
C	CHGE NOTE. DATE CODE WAS D-2134 PC-48-2894/REV.A	LNT/JB	8-12-81
D	CURRENT DATE CODE D-2134 PC 48-2894/REV.B	LNT/JB	8.26.81

E CURRENT DATE CODE E-2134 PC 48-3350 — 10-7-81
F CURRENT DATE CODE E-2134 PC 48-3350 — 10-5-82

ENGINEERING RESPONSIBILITY — DEPT.

D-12745-60010-35

(REV'S CONT.)

C6, C7, C40
10uF 20 VDC

+5V

P1-12,14 P1-16,20 P1-1,9 P1-29,30 P1-43,45 P1-47,50 P1-57,65 P1-1,2 P1-3,4

240Ω VAR C.T.S. P.N. 760-1-R240
680Ω USE C.T.S. P.N. 760-1-R680

J-44 J-42 J-40 J-38 J-45 J-41 J-39 J-37

J1-44 J1-42 J1-40 J1-38 J1-45 J1-41 J1-39 J1-37

J2-44 J2-42 J2-40 J2-38 J2-45 J2-41 J2-39 J2-37

J2-14 J2-12 J2-10 J2-8 J2-27 J2-25 J2-23 J2-21

J2-15 J2-16 J2-19 J2-20 J2-33 J2-49 J2-50

J2-45 J2-29 J2-3 J2-5 J2-4 J2-6 J2-13 J2-31

J2-28

J2-48 J2-9 J2-47 J2-46 J2-11 J2-7

DATA 8 DATA 7 DATA 6 DATA 5 DATA 4 DATA 3 DATA 2 DATA 1 WHCLK RHOC

RS-A RS-B RS-C RS-D RS-E RS-F RS-G RS-H RS-J RS-K RS-L RS-M RS-N RS-P RS-R

74LS241 U53 · 74LS241 U43 · 74S241 U33 · 74LS241 U23 · DM 8160 U35 · 74LS241 U13 · 74S244 U62

74LS279 U54 · 74LS374 U44 · 74LS279 U34 · 74LS374 U24 · 7603 U14

74LS624 U46 · 74LS08 U45 · 74LS04 U55 · 74LS00 U56 · 74LS11 U36 · 74LS10 U45 · 74LS74 U26 · 74LS123 U25 · 74LS08 U18 · 74LS04 U56 · 74LS00 U56 · 74LS08 U46 · 74LS38 U25 · 74LS38 U25 · 74LS38 U25 · 74LS03 U15 · 74LS04 U56 · 74LS11 U36 · 74LS08 U46 · 74LS02 U15

940 PF C.N.E. · C9 330 PF · R21 2.49K 1% · R2-H 1K · R2-N 1K · R2-O 1K · R1-H 1K · R2-A 1K · R2-B 1K

1990-0422 D1A CR2 (SEG.)

+5V

U42-14 U32-14 U22-14 U12-14

240Ω 680Ω

SELECT DISLO SERVICE E1

DISPLAY SERVICE CHG CLAMP 2 SERVICE

S1 EIRCO W1 1A 2I 3O 6I 6

E2,E4,E27,E31

E2 CHRDY E7 DTRDY E8 OVRUN E9 RDD E10 WRRQ E4

JACK CHRDY ROTARY ROTARY R.OVRUN R.RDD R.RCLK WRRQ R.WCLK

INTDK CHRDY DTRDY OVRUN RDD WRRQ

ENIR ENID INTD INT INT2 INT3 INTD ITCLK

CLEAR

JACK

ITEM | QTY. | MATERIAL-DESCRIPTION | MAT'L-PART NO. | MAT'L-DWG. NO. | MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY		8.18.78 DATE
ENGINEER		8.22.78
RELEASE TO PROD.		8.23.78
SUPERSEDES DWG.		

TITLE: REGISTER LOGIC
NEXT ASSEMBLY
FINISH — SCALE —

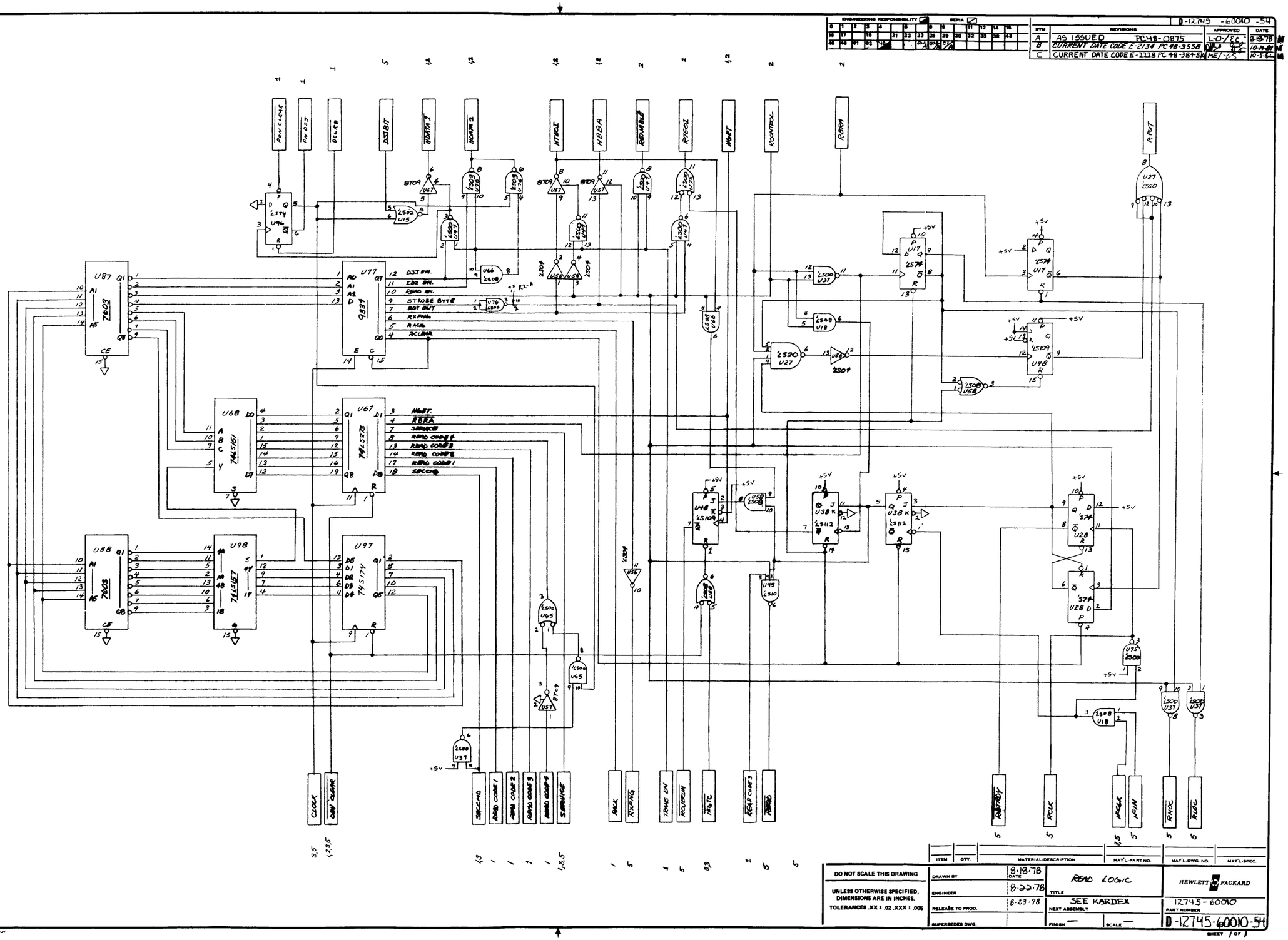
HEWLETT PACKARD
PART NUMBER 12475-60010
D-12745-60010-35
SHEET 1 OF 3

D-12745-60010-54

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0875	L.O./Ec.	9-15-78
B	CURRENT DATE CODE E-2134 PC 48-3558		10-11-78
C	CURRENT DATE CODE E-2128 PC 48-3845	ME/	10-5-78

ENGINEERING RESPONSIBILITY — SEPIA

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
48	49	81	82	113				254	255	256						



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005

DRAWN BY	8·18·78	
ENGINEER	8·22·78	
RELEASE TO PROD.	8·23·78	
SUPERSEDES DWG.		

TITLE: READ LOGIC

HEWLETT PACKARD

NEXT ASSEMBLY: SEE KARDEX

PART NUMBER: 12745-60010

FINISH — SCALE —

D-12745-60010-54

SHEET 1 OF 1

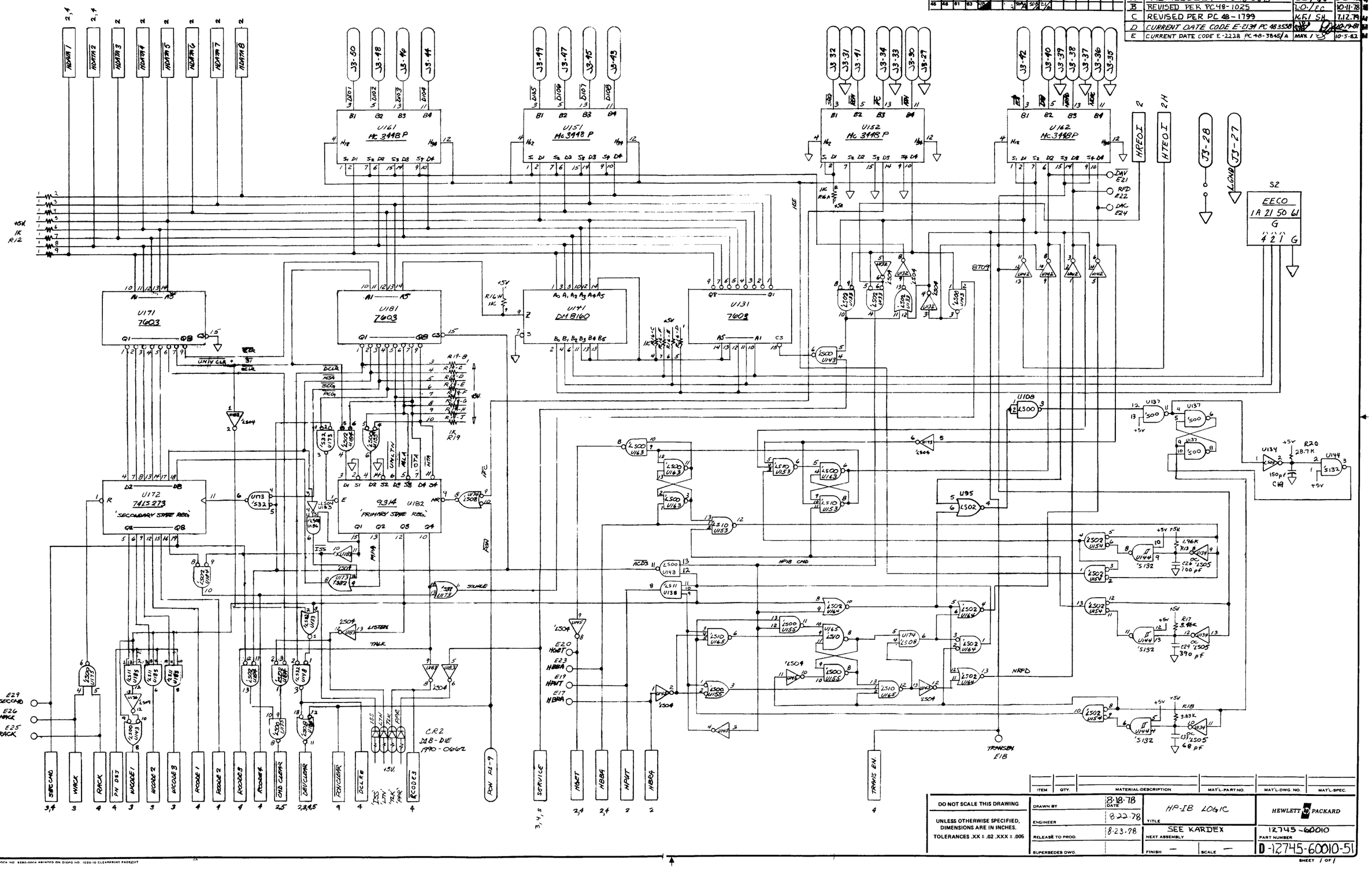
STOCK NO. 1280-1003 PRINTED ON DIEPO NO. 102010 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY															
0	1	2	3	4		6		8	9		11	12	13	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

SEPIA

D-12745-60010-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED. PC48-0875	LO./PC	5-18-78
B	REVISED PER PC48-1025	LO./PC	10-11-78
C	REVISED PER PC 48-1799	K.F.I SH	7.12.79
D	CURRENT DATE CODE E-2134 PC 483558		10-19-81
E	CURRENT DATE CODE E-2228 PC 48-3845/A	MAX /	10-5-82



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING	DRAWN BY	8.18.78 DATE	HP-IB LOGIC TITLE
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES .XX ± .02 .XXX ± .005	ENGINEER	8.22.78	SEE KARDEX NEXT ASSEMBLY
	RELEASE TO PROD.	8.23.78	FINISH — SCALE —
	SUPERSEDES DWG.		

HEWLETT PACKARD

12745-60010 PART NUMBER

D-12745-60010-51

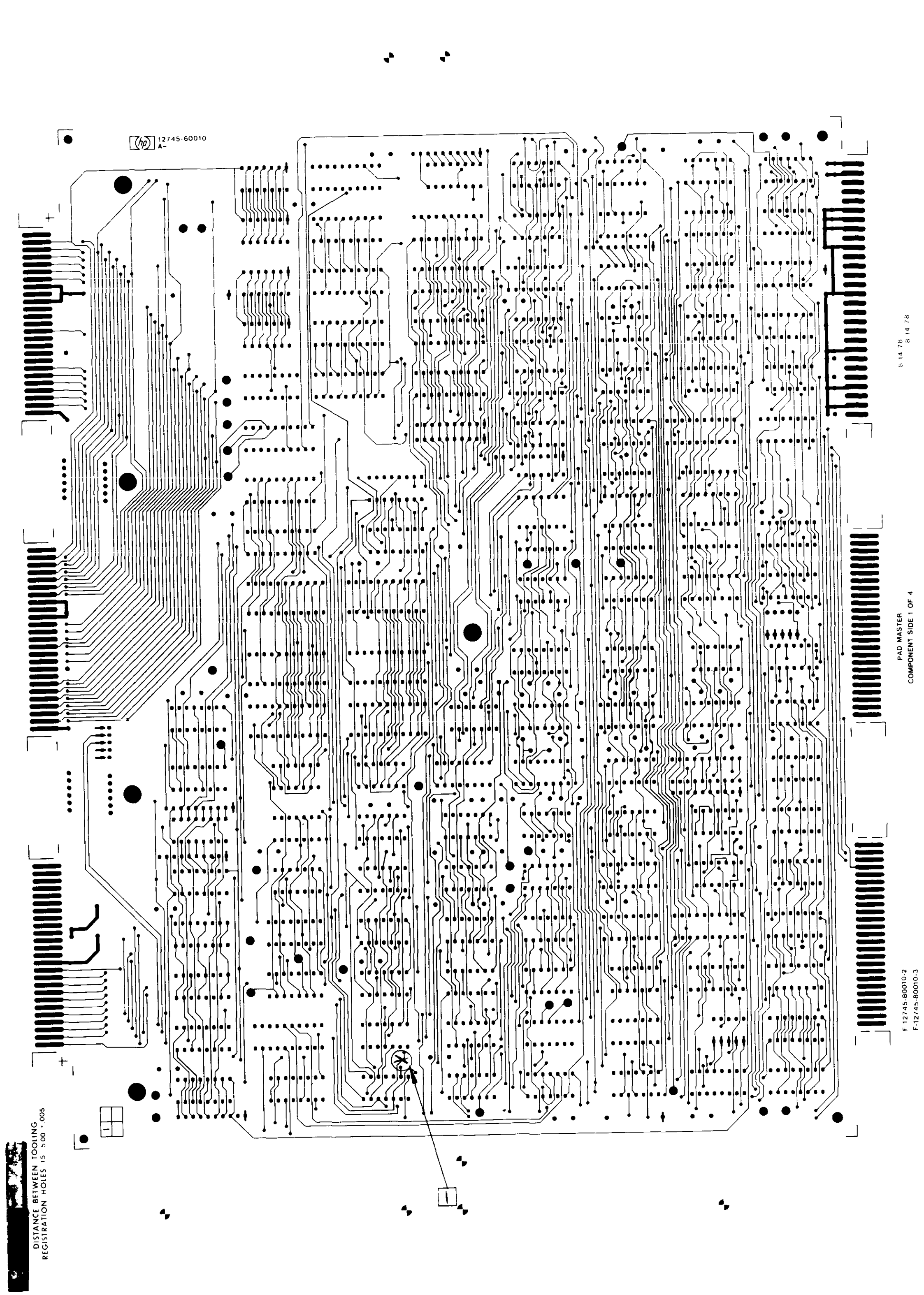
SHEET 1 OF 1

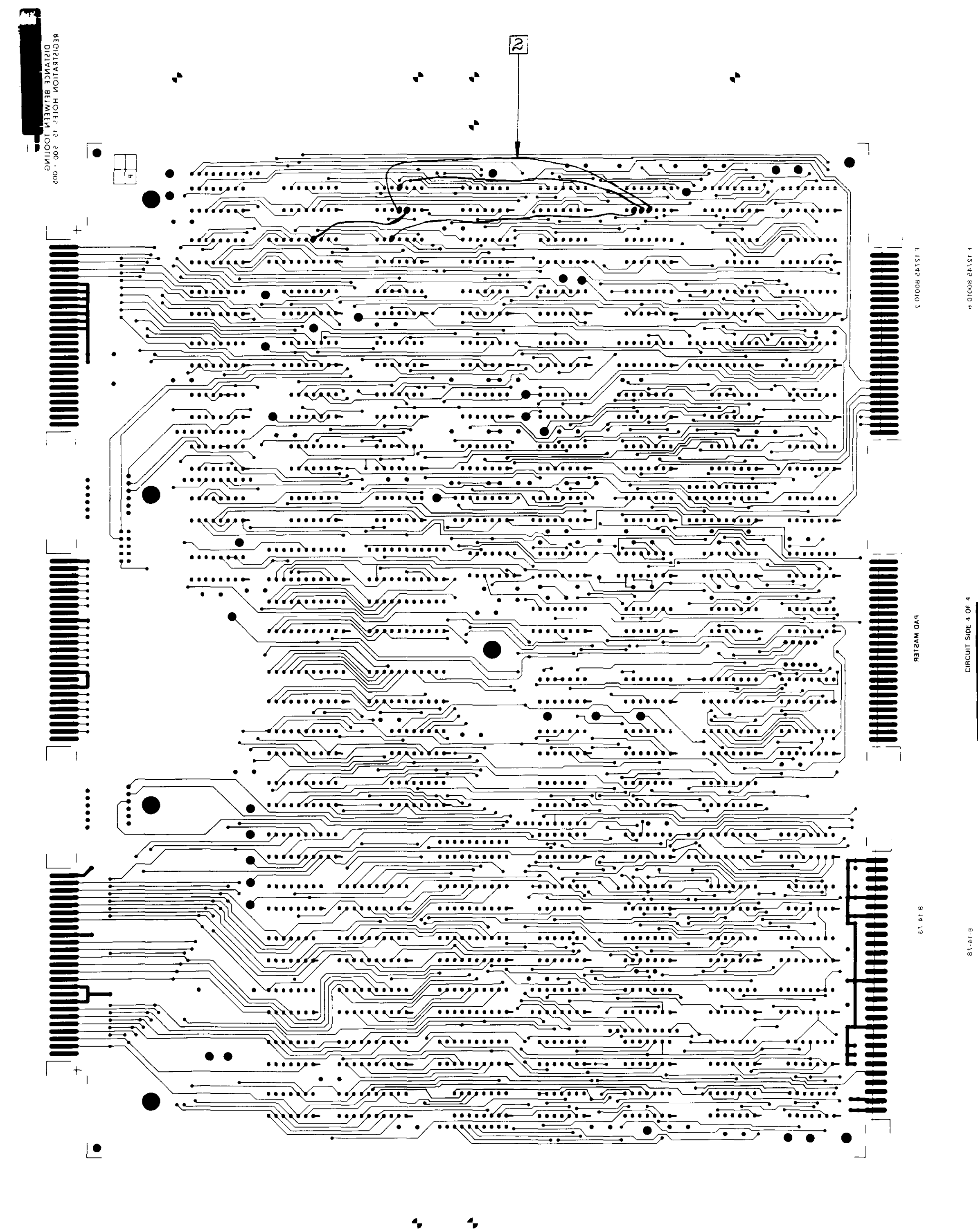
STOCK NO. 8280-0004 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY												SEPIA		
0	1	2	3	4		6		8	9		11	12	4	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	10	50	50A/A	C1/A							

D-12745 -60010 -20

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED. PCH8-1025	L.O./EG	10-11-78





NOTES:

1. CUT TRACE AS NOTED (1 PLACE.)
2. ADD JUMPERS AS NOTED (4 PLACES.)

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES XX ± .02 XXX ± .005

SEE CORP STD 608

DRAWN BY	DATE 10-11-78	TITLE MODIFICATION DRAWING
ENGINEER		
RELEASE TO PROD	10-11-78	NEXT ASSEMBLY SEE KARDEX
SUPERSEDES DWG		FINISH / SCALE

HEWLETT hp PACKARD

PART NUMBER 12745-60010

D-12745-60010-20

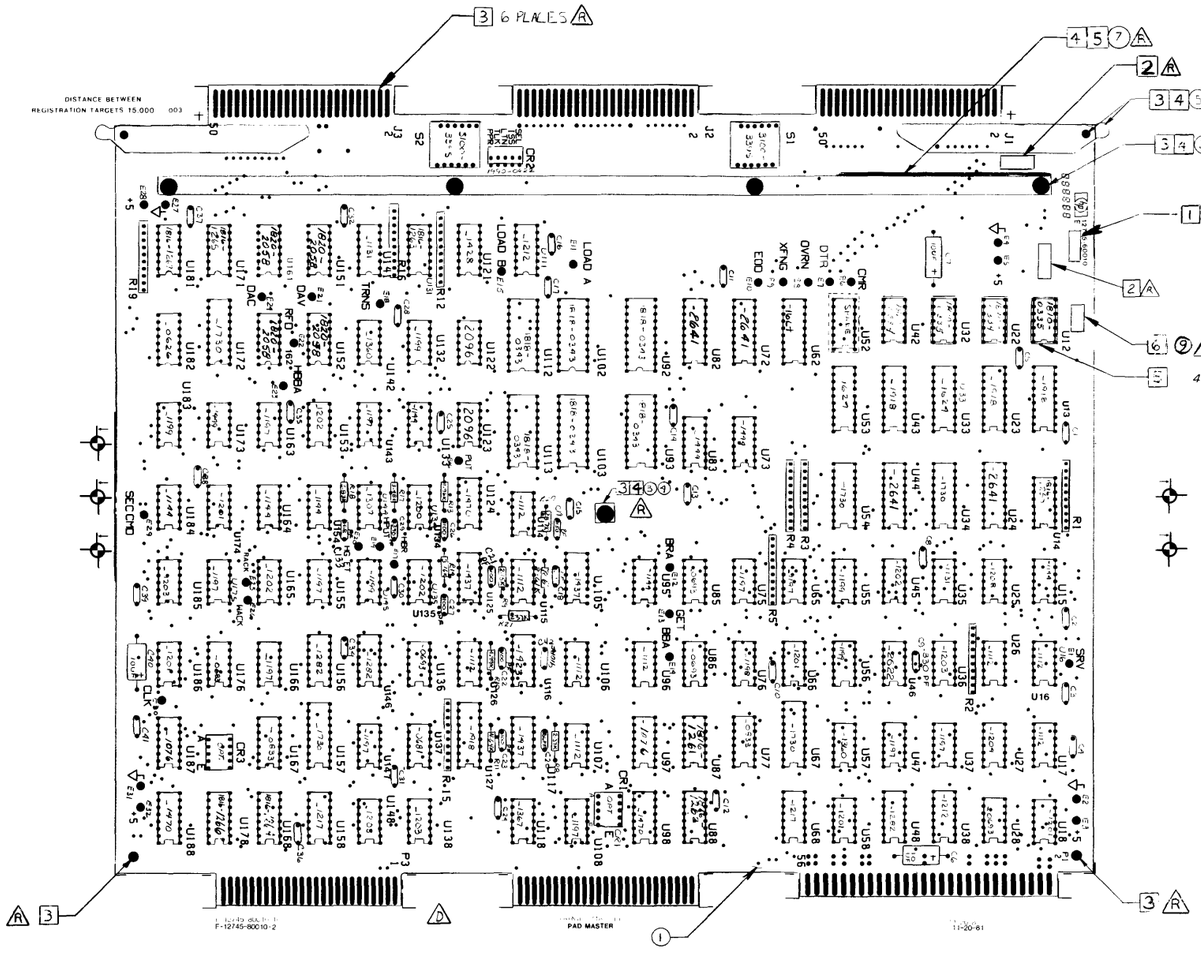
SHEET OF

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 6 8 9 11 12 14 16	
16 17 18 21 22 23 25 29 30 32 33 38 43	
45 46 81 83 A	

W	DATE CODE 2122B PC 48-3845/A	ME I	9-5-82
Y	CHG'D U122&U123 PER CC480863		7-26-84
Z	CORRECTED NOTE ON DRG. PER CC481280		2-25-85

D-12745-60010-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PC48-0875	LOT/ED	5-17-79
B	ADDED NOTE 7 DATE	ALE	
C	WAS 1.40 PC48-1[illegible]	L.T/E.D	
D	5060-0807 WAS 1326-0052 PC48-1140	TT/SH	10-30-79
E	CIRCUIT CHANGE PER PC48-1236	TT/SH	12-20-79
E	REVISED PER PC 48-1799	K.F./SH	7.12.79
F	DELETED ITEM 6 (7120-7348) AND NOTE 8 PC 48-1503	K.F./EC	8-20-79
G	[illegible]	[illegible]	[illegible]
M	[illegible]	[illegible]	[illegible]
J	BOARD REVISED; DELETE NOTE 7, ADD L REF PC 48-2162	[illegible]	2-[illegible]
K	ATTACHED CORRECT PAD MASTER PC 48-2463 REV. L	K.F./	11.16.80
L	REVD SW. FINAL [illegible]	[illegible]	3-6-81
M	C9 WAS 47 PF; U46 WAS -1642; DATE CODE WAS 7925. PC 48-2894	LNT/	7.2.81
N	DATE CODE WAS 2134. PC 48-2894/REV.A	LNT/	8.12.81
P	DATE CODE WAS D-2142 PC 48-2894/REV.B	LNT/	8.26.81
R	DATE CODE WAS D-2134 REVD PER PC 48-3553		10-19-81
S	CHGE DATA FOR NEW ARTWORK DATE PC 48-3558/B		11-25-81
T	CHANGED RAIT NO. ON U14, U87, U88, U131, U163, U171, U178 & U181 PCO 48-3745	K.F/	
V	REVISED PER PCO 48-5013	K.F./	2-22-82
U	REVISED PER PCO 48-5016	K.F./	7.30.82



REFERENCE DRAWINGS } **SCHEMATIC** D-12745-60010 **-51**,52,53,54,55

UNLESS NOTED OTHERWISE:

ALL RESISTANCE IN *OHMS*
ALL RESISTORS *1/8 W 1%*
ALL CAPACITANCE IN *MICROFARADS*
ALL CAPACITORS *.01 CERAMIC DISC*
ALL IC's *ARE 1820-XXXX*
ALL DIODES —
ALL TRANSISTORS —
ALL RESISTOR PACKS ARE 1810-0275

NOTES:

A A A A 1 DLR 266. MARK ASSEMBLY DATE CODE 2128.
A 2 DLR 266. MARK PART NUMBER, DATE CODE, COMPONENT SIDE.
A 3 DLR [illegible] MASK PRIOR TO LOADING
A 4 DLR 265. TOUCH UP. INSTALL ITEMS 3 3 9 9 0 x 1
A 5 DLR [illegible] INSTALL ITEM [illegible]
ALSO INSTALL ITEM (7) [illegible]
A 6 IN SAME [illegible]

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
9	1	LABEL "ORIGIN"	7120-8330		
8		DELETED			
7	1	LABEL	7120-7185		
6	2	EXTRACTOR	5040-6009		
5	2	PIN	1480-0116		
4	1	SPACER	5020-7318		
3	2	SCREW	0624-0077		
2	1	BRACE	5040-6058		
1	1	BOARD-ETCHED	12745-80010		

DO NOT SCALE THIS DRAWING	DRAWN BY	DATE 8-17-78	HP-IB INTERFACE ASSEMBLY DWG.
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.	ENGINEER		TITLE
TOLERANCES .XX ± .02 .XXX ± .005	RELEASE TO PROD.	8-17-78	NEXT ASSEMBLY SEE WHERE USED
SEE CORP. STD. 608	SUPERSEDES DWG.		FINISH SCALE 1:1

HEWLETT PACKARD

PART NUMBER 12745-60010

D-12745-60010-1

SHEET 1 OF 1